TEXAS INSTRUMENTS

**HD3SS213**

SLAS901B –SEPTEMBER 2013–REVISED DECEMBER 2016

# HD3SS213 5.4-Gbps DisplayPort 1.2a 2:1 and 1:2 Differential Switch

## 1 Features

- Compatible with DisplayPort 1.2 Electrical Standard
- 2:1 and 1:2 Switching Supporting Data Rates up to 5.4 Gbps
- Supports HPD Switching
- Supports AUX and DDC Switching
- Wide –3-dB Differential BW of over 5.4 GHz
- Excellent Dynamic Characteristics (at 2.7 GHz):
  - Crosstalk = –50 dB
  - Isolation = –25 dB
  - Insertion Loss = –1.5 dB
  - Return Loss = –13 dB
  - Maximum Bit-Bit Skew = 5 ps
- $V_{DD}$ Operating Range: 3.3 V ±10%
- Package Options:
  - 5 mm × 5 mm, 50-Pin BGA Microstar Junior
- Output Enable (OE) Pin Disables Switch to Save Power
- HD3SS213 < 10 mW (Standby < 30 μW when OE = L)

## 2 Applications

- Motherboard Applications Needing DP and PCI Express
- Desktop and Notebook Applications:
  - DP Switching
  - PCI Express Switching
- Docking

## 3 Description

The HD3SS213 device is a high-speed passive switch capable of switching two full DisplayPort 4 lane ports from one of two sources to one target location in an application. It also switches one source to one of two sinks. For DisplayPort applications, the HD3SS213 supports switching of the Auxiliary (AUX), Display Data Channel (DDC), and Hot Plug Detect (HPD) signals in the ZEQ package.
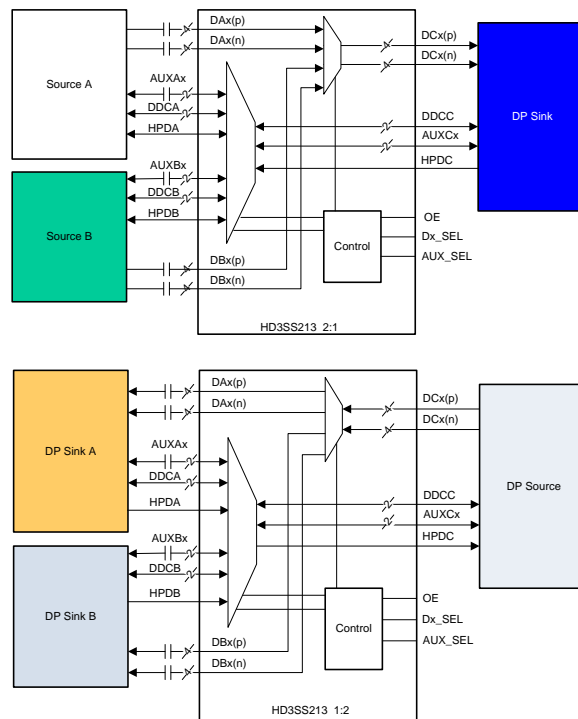
One typical application is a mother board that includes two GPUs that need to drive one DisplayPort sink. The GPU is selected by the Dx_SEL pin. Another application is when one source needs to switch between one of two sinks which the example is a side connector and a docking station connector. The switching is controlled using the Dx_SEL and AUX_SEL pins. The HD3SS213 operates from a single supply voltage of 3.3 V over the full industrial temperature range of –40°C to 105°C.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| HD3SS213 | BGA Microstar Junior (50) | 5.00 mm x 5.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### HD3SS213 Application Block Diagram



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## Table of Contents

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (September 2013) to Revision B**                                                                    **Page**

* Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ..................................... 1
* Added A2 to J4 row in *Pin Functions* table ......................................................................................................................... 4

**Changes from Original (September 2013) to Revision A**                                                                    **Page**

* Deleted Ordering Information ................................................................................................................................................. 3

# 5 Pin Configuration and Functions

**BGA Microstar Junior**
**50-Pin ZQE Package**
**Top View**

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| **A** | Dx_SEL | VDD |  | DA0(n) | DA1(n) | DA2(n) |  | DA3(p) | DA3(n) |
| **B** | DC0(n) | DC0(p) | GND | DA0(p) | DA1(p) | DA2(p) | OE | DB0(p) | DB0(n) |
| **C** |  | AUX_SEL |  |  |  |  |  | GND |  |
| **D** | DC1(n) | DC1(p) |  |  |  |  |  | DB1(p) | DB1(n) |
| **E** | DC2(n) | DC2(p) |  |  |  |  |  | DB2(p) | DB2(n) |
| **F** | DC3(n) | DC3(p) |  |  |  |  |  | DB3(p) | DB3(n) |
| **G** |  | GND |  |  |  |  |  | GND |  |
| **H** | AUXC(n) | AUXC(p) | HPDB | GND | DDCCLK_B | AUXB(p) | GND | DDCCLK_A | AUXA(p) |
| **J** | HPDC | HPDA | DDCCLK_C | VDD | DDCDAT_B | AUXB(n) | DDCDAT_C | DDCDAT_A | AUXA(n) |

## Pin Functions

| PIN | | TYPE[1] | DESCRIPTION[2] |
|---|---|---|---|
| NO. | NAME | | |
| H9, J9 | AUXA(p), AUXA(n) | I/O | Port A AUX positive signal<br>Port A AUX negative signal |
| H6, J6 | AUXB(p), AUXB(n) | I/O | Port B AUX positive signal<br>Port B AUX negative signal |
| H2, H1 | AUXC(p), AUXC(n) | I/O | Port C AUX positive signal<br>Port C AUX negative signal |
| C2 | AUX_SEL | I | AUX/DDC selection control pin in conjunction with Dx_SEL Pin |
| NA | CADA/B/C | I/O | Port A/B/C cable activity detect |
| B4, A4 | DA0(p), DA0(n) | I/O | Port A, Channel 0, High speed positive signal<br>Port A, Channel 0, High speed negative signal |
| B5, A5 | DA1(p), DA1(n) | I/O | Port A, Channel 1, High speed positive signal<br>Port A, Channel 1, High speed negative signal |
| B6, A6 | DA2(p), DA2(n) | I/O | Port A, Channel 2, High speed positive signal<br>Port A, Channel 2, High speed negative signal |
| A8, A9 | DA3(p), DA3(n) | I/O | Port A, Channel 3, High speed positive signal<br>Port A, Channel 3, High speed negative signal |
| B8, B9 | DB0(p), DB0(n) | I/O | Port B, Channel 0, High speed positive signal<br>Port B, Channel 0, High speed negative signal |
| D8, D9 | DB1(p), DB1(n) | I/O | Port B, Channel 1, High speed positive signal<br>Port B, Channel 1, High speed negative signal |
| E8, E9 | DB2(p), DB2(n) | I/O | Port B, Channel 2, High speed positive signal<br>Port B, Channel 2, High speed negative signal |
| F8, F9 | DB3(p), DB3(n) | I/O | Port B, Channel 3, High speed positive signal<br>Port B, Channel 3, High speed negative signal |
| B2, B1 | DC0(p), DC0(n) | I/O | Port C, Channel 0, High speed positive signal<br>Port C, Channel 0, High speed negative signal |
| D2, D1 | DC1(p), DC1(n) | I/O | Port C, Channel 1, High speed positive signal<br>Port C, Channel 1, High speed negative signal |
| E2, E1 | DC2(p), DC2(n) | I/O | Port C, Channel 2, High speed positive signal<br>Port C, Channel 2, High speed negative signal |
| F2, F1 | DC3(p), DC3(n) | I/O | Port C, Channel 3, High speed positive signal<br>Port C, Channel 3, High speed negative signal |
| H8, J8 | DDCCLK_A, DDCDAT_A | I/O | Port A DDC clock signal<br>Port A DDC data signal |
| H5, J5 | DDCCLK_B, DDCDAT_B | I/O | Port B DDC clock signal<br>Port B DDC data signal |
| J3, J7 | DDCCLK_C, DDCDAT_C | I/O | Port C DDC clock signal<br>Port C DDC data signal |
| A1 | Dx_SEL | I | High speed port selection control pins |
| B3, C8, G2, G8, H4, H7 | GND | S | Ground |
| J2 | HPDA | I/O | Port A hot plug detect |
| H3 | HPDB | I/O | Port B hot plug detect |
| J1 | HPDC | I/O | Port C hot plug detect |
| B7 | OE | I | Output enable:<br>OE = $V_{IH}$: Normal operation<br>OE = $V_{IL}$: Standby mode |
| A2, J4 | VDD | S | 3.3-V positive power supply voltage |

(1) I = Input, O = Output, S = Supply
(2) The high speed data ports incorporate 20-kΩ pulldown resistors that are switched in when a port is not selected and switched out when the port is selected.

Product Folder Links: *HD3SS213*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$[2] |  | −0.5 | 4 | V |
| Voltage | Differential I/O | −0.5 | 4 | V |
|  | Control pin | −0.5 | $V_{DD}$ + 0.5 |  |
| Continuous power dissipation |  | See *Thermal Information* |  |  |
| Operating free-air temperature, $T_A$ |  | −40 | 105 | °C |
| Storage temperature, $T_{stg}$ |  |  | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
|  |  | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 |  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Typical values for all parameters are at $V_{CC}$ = 3.3 V and $T_A$ = 25°C (unless otherwise noted). All temperature limits are specified by design.

| PARAMETER |  | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage |  | 3 | 3.3 | 3.6 | V |
| $V_{IH}$ | Input high voltage | Control pins and signal pins (Dx_SEL, AUX_SEL, OE, HPDx) | 2 |  | $V_{DD}$ | V |
| $V_{IM}$ | Input mid level voltage | AUX_SEL pin | $V_{DD}$/2 − 300 mV | $V_{DD}$/2 | $V_{DD}$/2 + 300 mV | V |
| $V_{IL}$ | Input low voltage | Control pins and signal pins (Dx_SEL, AUX_SEL, OE, HPDx) | −0.1 |  | 0.8 | V |
| $V_{I/O\_Diff}$ | Differential voltage (Dx, AUXx) | Switch I/O differential voltage | 0 |  | 1.8 | $V_{PP}$ |
| $V_{I/O\_CM}$ | Dx switching I/O common-mode voltage | Switch I/O common-mode voltage | 0 |  | 2 | V |
|  | AUXx switching I/O common-mode voltage | Switch I/O common-mode voltage | 0 |  | 3.6 | V |
| $I_{IH}$ | Input high current (Dx_SEL, AUX_SEL) | $V_{DD}$ = 3.6 V, $V_{IN}$ = $V_{DD}$ |  |  | 1 | µA |
| $I_{IM}$ | Input mid level current (AUX_SEL) | $V_{DD}$ = 3.6V, $V_{IN}$ = $V_{DD}$/2 |  |  | 1 | µA |
| $I_{IL}$ | Input low current (Dx_SEL, AUX_SEL) | $V_{DD}$ = 3.6 V, $V_{IN}$ = GND |  |  | 1 | µA |
| $I_{LK}$ | Leakage current (Dx_SEL, AUX_SEL) | $V_{DD}$ = 3.3 V, $V_I$ = 2 V, OE = 3.3 V |  |  | 1 | µA |
|  | Leakage current (HPDx) | $V_{DD}$ = 3.3 V, $V_I$ = 2 V, OE = 3.3 V, Dx_SEL = 3.3 V |  |  | 1 | µA |
|  |  | $V_{DD}$ = 3.3 V, $V_I$ = 2 V, OE = 3.3 V, Dx_SEL = GND |  |  | 1 |  |
| $I_{off}$ | Device shut down current | $V_{DD}$ = 3.6 V, OE = GND |  |  | 2.5 | µA |
| $I_{DD}$ | Supply current | $V_{DD}$ = 3.6 V, Dx_SEL or AUX_SEL = $V_{DD}$ or GND |  | 0.6 | 1 | mA |

## Recommended Operating Conditions (continued)

Typical values for all parameters are at $V_{CC}$ = 3.3 V and $T_A$ = 25°C (unless otherwise noted). All temperature limits are specified by design.

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DA, DB, DC HIGH SPEED SIGNAL PATH** | | | | | | |
| $C_{ON}$ | Outputs ON capacitance | $V_I$ = 0 V, outputs open, switch ON | | 1.5 | | pF |
| $C_{OFF}$ | Outputs OFF capacitance | $V_I$ = 0 V, outputs open, switch OFF | | 1 | | pF |
| $R_{ON}$ | ON resistance | $V_{DD}$ = 3.3 V, VCM = 0.5 V to 1.5 V, $I_O$ = −40 mA | | 8 | 12 | Ω |
| $\Delta R_{ON}$ | ON resistance match between pairs of the same channel | $V_{DD}$ = 3.3 V, 0.5 V ≤ $V_I$ ≤ 1.2V, $I_O$ = −40 mA | | | 1.5 | Ω |
| $R_{FLAT\_ON}$ | ON resistance flatness, $R_{ON(max)} - R_{ON(min)}$ | $V_{DD}$ = 3.3 V, 0.5 V ≤ $V_I$ ≤ 1.2 V | | 1.3 | | Ω |
| **AUXx, DDC SIGNAL PATH** | | | | | | |
| $C_{ON}$ | Outputs ON capacitance | $V_I$ = 0 V, outputs open, switch ON | | 9 | | pF |
| $C_{OFF}$ | Outputs OFF capacitance | $V_I$ = 0 V, outputs open, switch OFF | | 3 | | pF |
| $R_{ON(AUX)}$ | ON resistance | $V_{DD}$ = 3.3 V, $V_{CM}$ = 0 V − $V_{DD}$, $I_O$ = −8 mA | | 6 | 10 | Ω |
| $R_{ON(DDC)}$ | ON resistance on DDC channel | $V_{DD}$ = 3.3 V, $V_{CM}$ = 0.4 V, $I_O$ = −3 mA | | 20 | 30 | Ω |

## 6.4 Thermal Information

| THERMAL METRIC | | HD3SS213 | UNIT |
|---|---|---|---|
| | | BGA (ZQE) | |
| | | 50 PIN | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 90.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 41.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 53.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 53.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

## 6.5 Electrical Characteristics

over recommended operating conditions; $R_L$ and $R_{SC}$ = 50 Ω (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_L$ | Dx differential return loss | 1.35 GHz | | −17 | | dB |
| | | 2.7 GHz | | −13 | | |
| $X_{TALK}$ | Dx differential crosstalk | 2.7 GHz | | −50 | | dB |
| $O_{IRR}$ | Dx differential off-isolation | 2.7 GHz | | −25 | | dB |
| $I_L$ | Dx differential insertion loss | f = 1.35 GHz | | −1 | | dB |
| | | f = 2.7 GHz | | −1.5 | | |
| | AUX −3-dB bandwidth | | | 360 | | MHz |

(1) For return loss, crosstalk, off-isolation, and insertion loss values, the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

## 6.6 Timing Requirements

over recommended operating conditions; $R_L$ and $R_{SC}$ = 50 Ω (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PD}$ | Switch propagation delay | $R_{SC}$ and $R_L$ = 50 Ω, see Figure 2 | | | 100 | ps |
| $T_{on}$ | Dx_SEL/AUX_SEL-to-switch Ton (Data, AUX and DDC) | $R_{SC}$ and $R_L$ = 50 Ω, see Figure 1 | | 0.7 | 1 | µs |
| $T_{off}$ | Dx_SEL/AUX_SEL-to-switch Toff (Data, AUX and DDC) | $R_{SC}$ and $R_L$ = 50 Ω, see Figure 1 | | 0.7 | 1 | µs |
| $T_{on}$ | Dx_SEL/AUX_SEL-to-switch Ton (HPD) | $R_L$ = 50 Ω, see Figure 1 | | 0.7 | 1 | µs |
| $T_{off}$ | Dx_SEL/AUX_SEL-to-switch Toff (HPD) | $R_L$ = 50 Ω, see Figure 1 | | 0.7 | 1 | µs |
| $T_{SK(O)}$ | Inter-pair output skew (CH-CH) | $R_{SC}$ and $R_L$ = 1 kΩ, see Figure 2 | | | 50 | ps |
| $T_{SK(b-b)}$ | Intra-pair output skew (bit-bit) | $R_{SC}$ and $R_L$ = 1 kΩ, see Figure 2 | | 1 | 5 | ps |
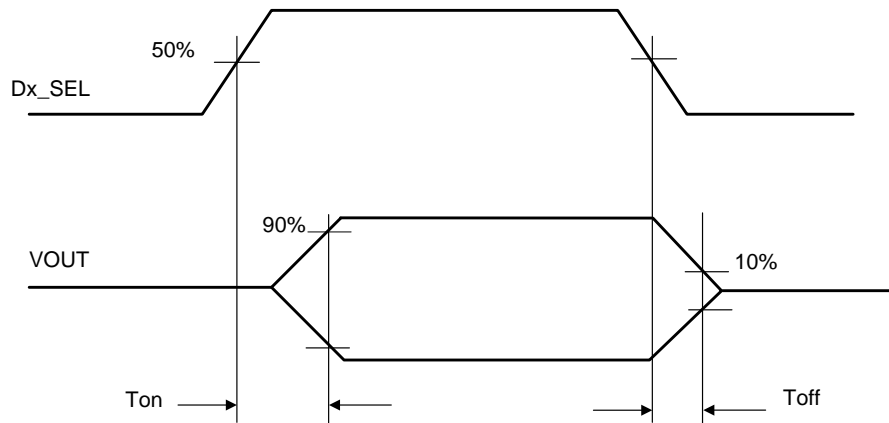


**Figure 1. Select to Switch Ton and Toff**

$t_{PD} = \text{Max}(t_{p1}, t_{p2})$

$t_{SK(O)} = $ Difference between $t_{PD}$ for any two pairs of outputs

$t_{SK(b-b)} = 0.5 \times |(t_4 - t_3) + (t_1 - t_2)|$

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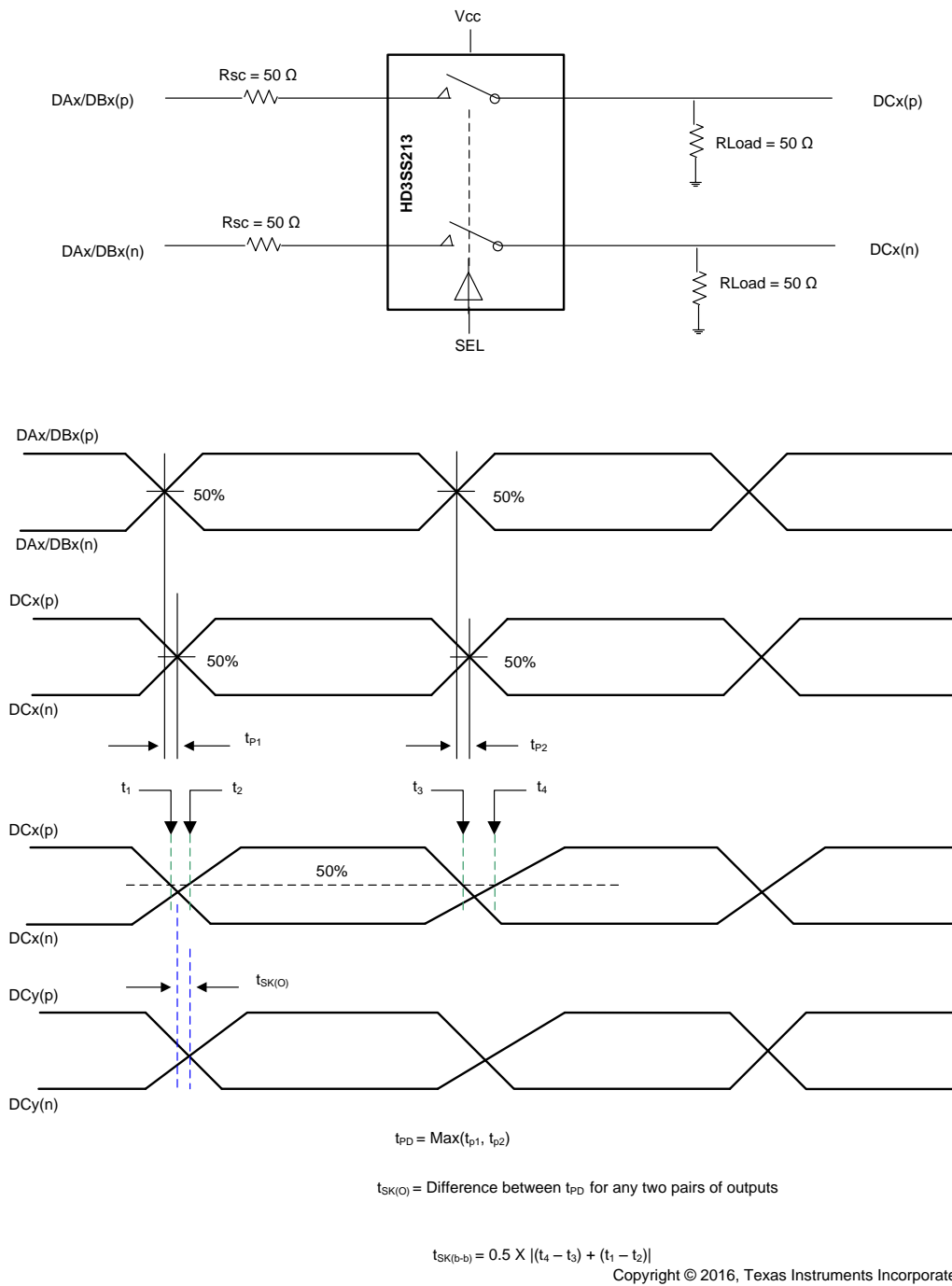
**Figure 2. Propagation Delay and Skew**

Product Folder Links: *HD3SS213*

## 6.7 Typical Characteristics
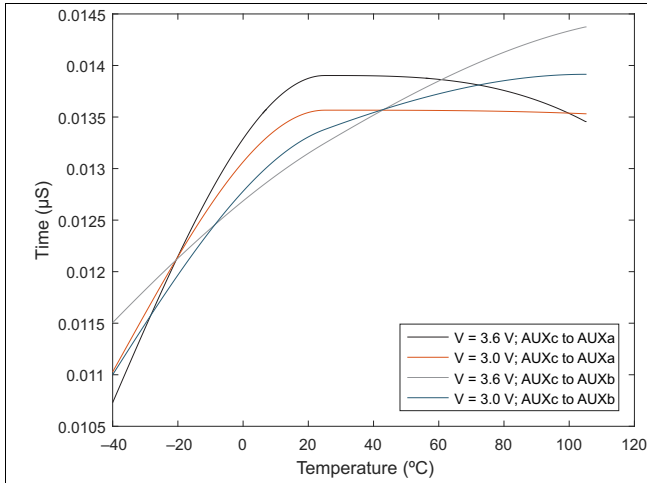


**Figure 3. DxSEL to Switch Toff**
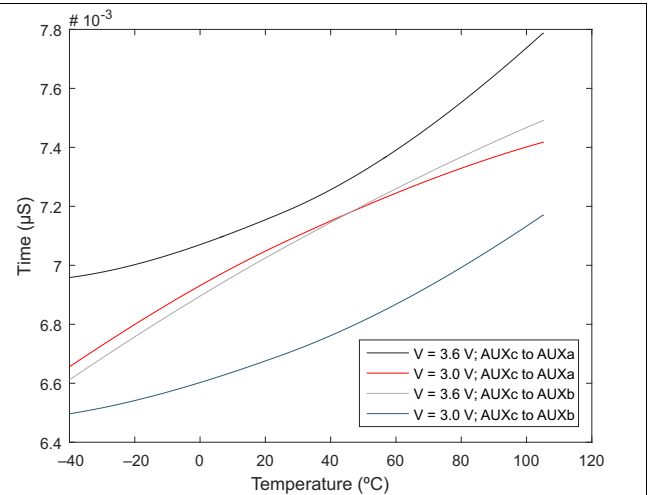


**Figure 4. DxSEL to Switch Ton**
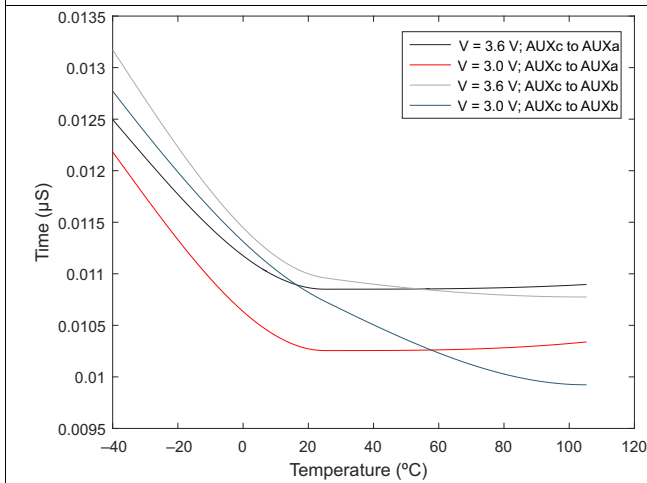


**Figure 5. OUTEN to Switch Toff**
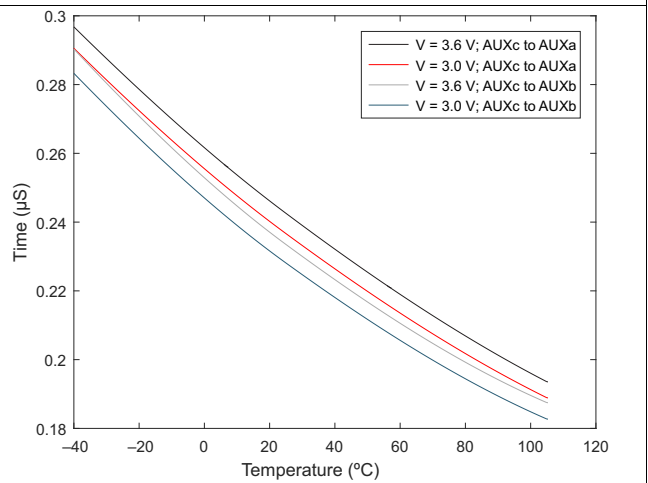


**Figure 6. OUTEN to Switch Ton**

# 7 Detailed Description

## 7.1 Overview

The HD3SS213 device is a high-speed passive switch offered in an industry standard 50-pin BGA Microstar Junior package. The device is specified to operate from a single supply voltage of 3.3 V over the industrial temperature range of –40°C to 105°C. The HD3SS213 is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The HD3SS213 also supports several other high speed data protocols with a differential amplitude of < 1800 mV$_{PP}$ and a common-mode voltage of < 2 V, as with USB 3.0 and DisplayPort 1.2. For display port applications, the HD3SS213 also supports switching of both the auxiliary and hot plug detect signals.

The high speed port selection control inputs of the device, Dx_SEL and AUX_SEL pins can easily be controlled by available GPIO pins within a system.

## 7.2 Functional Block Diagram
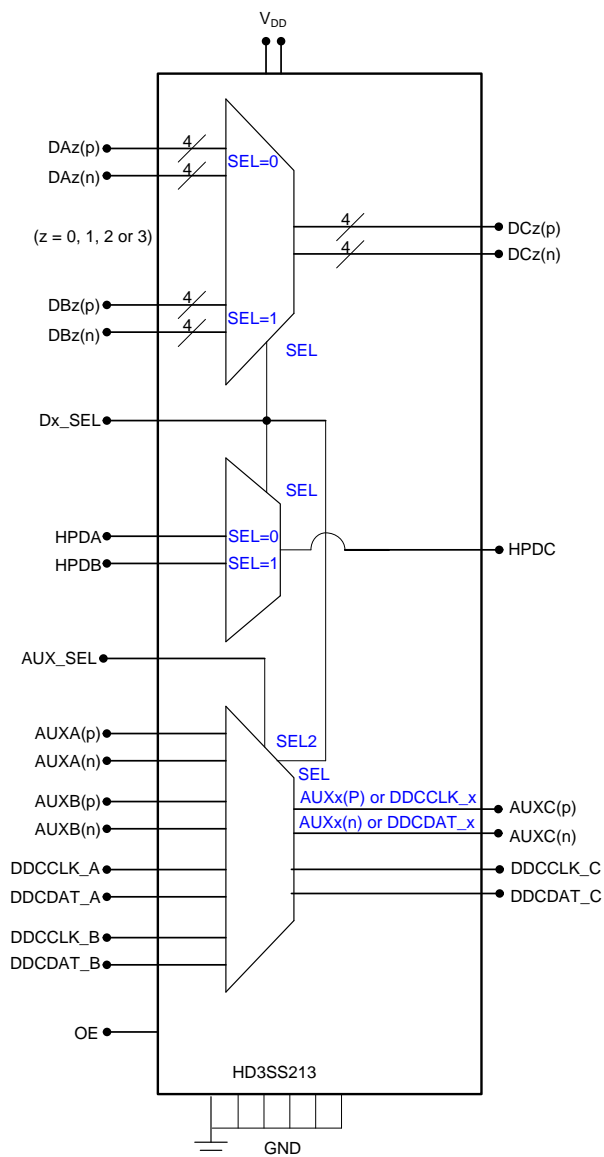


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## 7.3 Feature Description

The HD3SS213 behaves as a two to one or one to two using high bandwidth pass gates (see *Functional Block Diagram*). The input ports are selected using the AUX_SEL and Dx_SEL pins which are shown in Table 1.

### Table 1. AUX/DDC Switch Control Logic

| CONTROL LINES | | SWITCHED I/O PINS | | | | | |
|---|---|---|---|---|---|---|---|
| AUX_SEL | Dx_SEL | AUXA | AUXB | AUXC | DDCA | DDCB | DDCC |
| L | L | To/From AUXC | Z | To/From AUXA | Z | Z | Z |
| L | H | Z | To/From AUXC | To/From AUXB | Z | Z | Z |
| H | L | Z | Z | To/From DDCA | To/From AUXC | Z | Z |
| H | H | Z | Z | To/From DDCB | Z | To/From AUXC | Z |
| M | L | To/From AUXC | Z | To/From AUXA | To/From DDCC | Z | To/From DDCA |
| M | H | Z | To/From AUXC | To/From AUXB | Z | To/From DDCC | To/From DDCB |

## 7.4 Device Functional Modes

The HD3SS213 can be operated in normal operation mode or in shut down mode. In normal operation, the inputs ports of the HD3SS213 are routed to the output ports according to Table 1. In standby mode, the HD3SS213 is disabled to enable power savings with a typical current consumption of 2.5 µA. The functional mode is selected through the OE input pin with HIGH for normal operation and LOW for standby.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

Many interfaces require AC coupling between the source and sink. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs must be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 µF is best and the value must be match for the ± signal pair. There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage must be provided. A few placement options are shown below.

In Figure 7, the coupling capacitors are placed on the source pair. In this situation, the switch is biased by the sink.
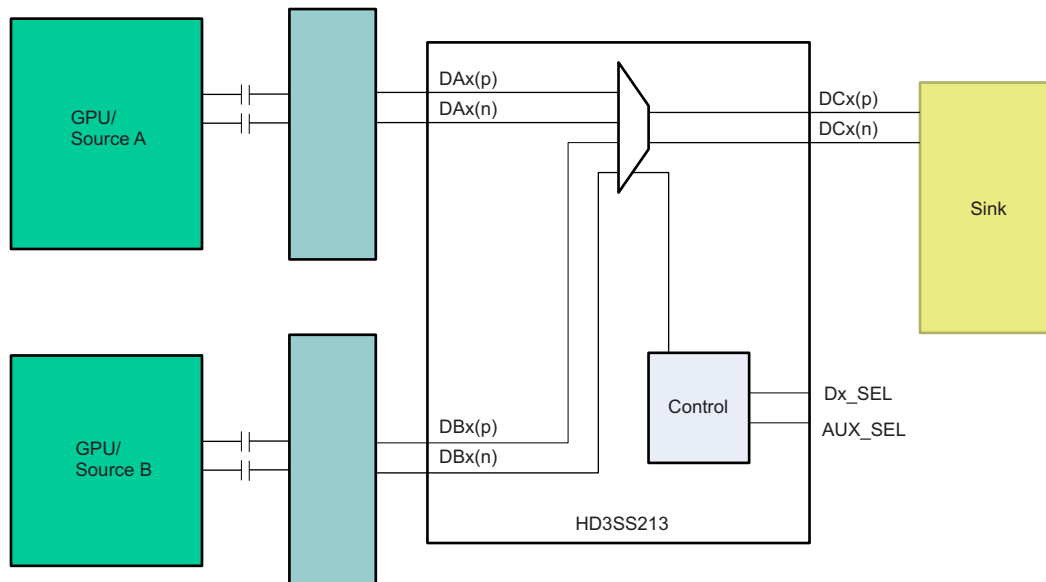


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**Figure 7. Source Biased by the Sink**

In Figure 8, the coupling capacitors are placed between the switch and Sink. In this situation, the switch is biased by the Source

## Application Information (continued)
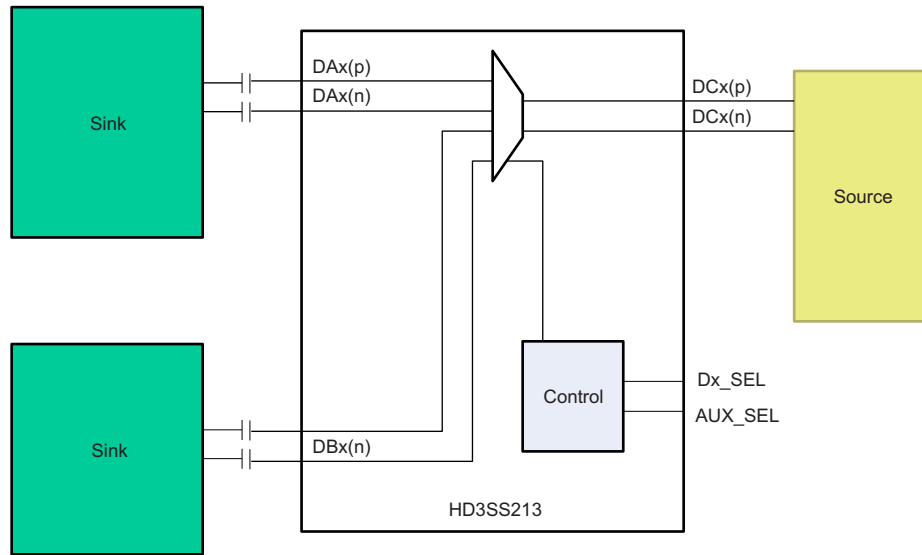


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**Figure 8. Switch Biased by the Source**

## 8.2 Typical Applications

### 8.2.1 HD3SS213 AUX Channel in 2:1 Application
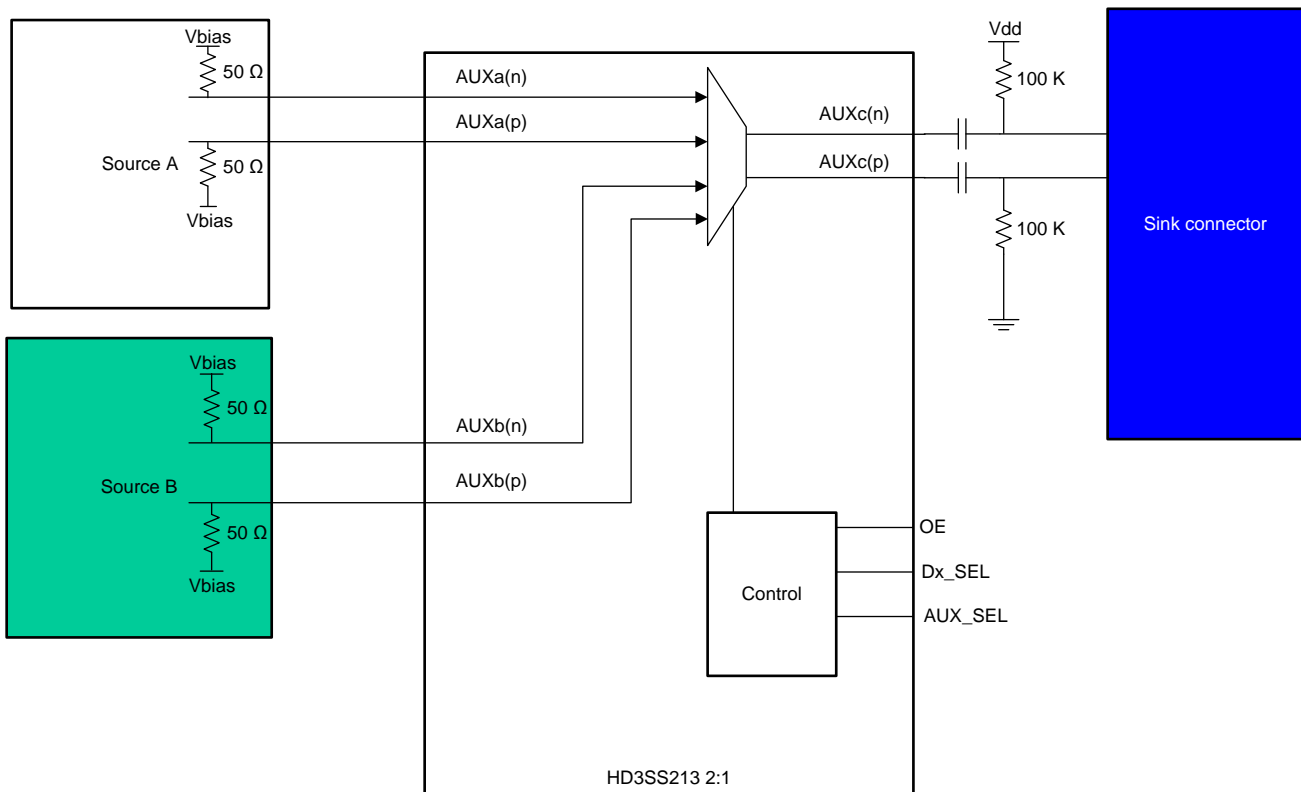


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**Figure 9. HD3SS213 AUX Channel in 2:1 Application Schematic**

Product Folder Links: *HD3SS213*

## Typical Applications  (continued)

### 8.2.1.1  Design Requirements

Table 2 lists the design parameters.

**Table 2. Design Parameters**

| PARAMETERS | VALUE |
|---|---|
| Input voltage | 3.3 V |
| Decoupling capacitors | 0.1 µF |
| AC capacitors[(1)] | 75 nF to 200 nF AC capacitors |

(1)  DAx, AUXAx, AUXBx and DBx require AC capacitors. N lines require AC capacitors. Alternate mode signals may or may not require AC capacitors.

### 8.2.1.2  Detailed Design Procedure

- Connect VDD and GND pins to the power and ground planes of the printed-circuit board with 0.1-µF bypass capacitor
- Use VDD/2 logic level at AUX_SEL pin
- Use 3.3-V TTL/CMOS logic level at Dx_SEL to connect DAx to DCx
- Use GND logic level at Dx_SEL to connect DBx to DCx
- Use controlled-impedance transmission media for all the differential signals
- Ensure the received complimentary signals are with a differential amplitude of <1800 mV$_{PP}$ and a common-mode voltage of <2 V

### 8.2.1.3  Application Curves



Figure 10.  Intra-Pair Skew Ports C to A (µs)



Figure 11.  Intra-Pair Skew Ports C to B (µs)
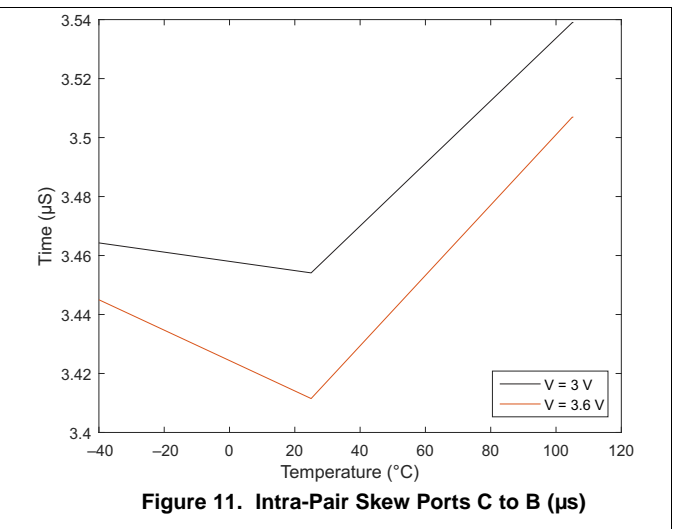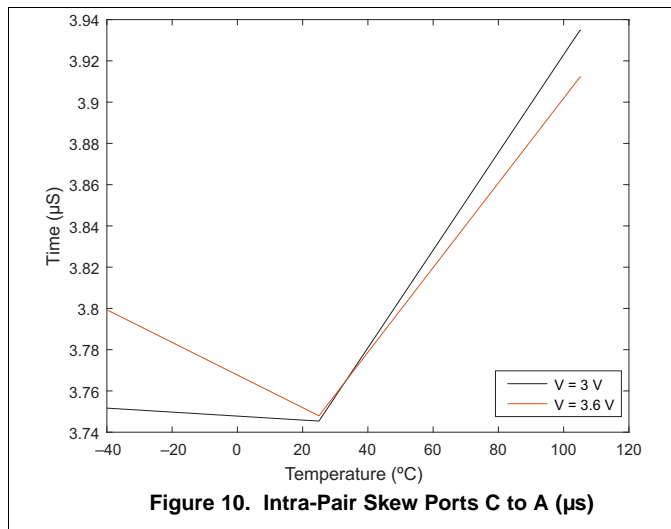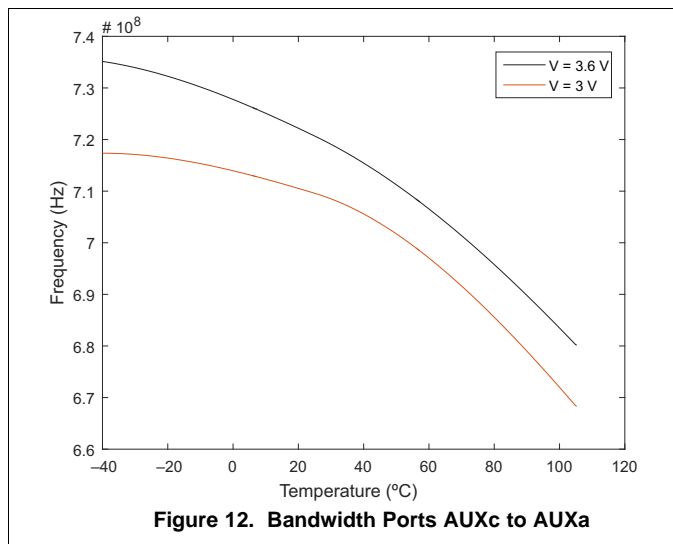
**Figure 12.  Bandwidth Ports AUXc to AUXa**
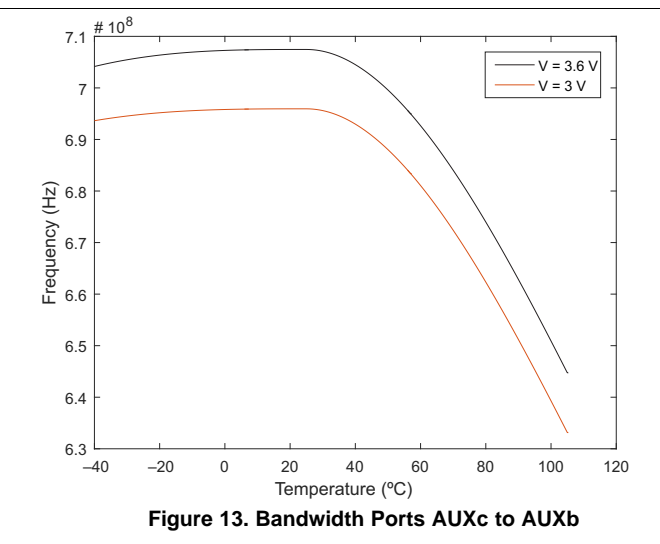


**Figure 13. Bandwidth Ports AUXc to AUXb**

### 8.2.2   HD3SS213 AUX Channel in 1:2 Application

AUX channel is controlled by AUX_SEL. This pin configures the switch to route the incoming AUX signal to the outgoing AUX path, when AUX_SEL = 0 the AUXA channel is routed to AUXC, when AUX_SEL = 1 the AUXB channel is routed to AUXC.
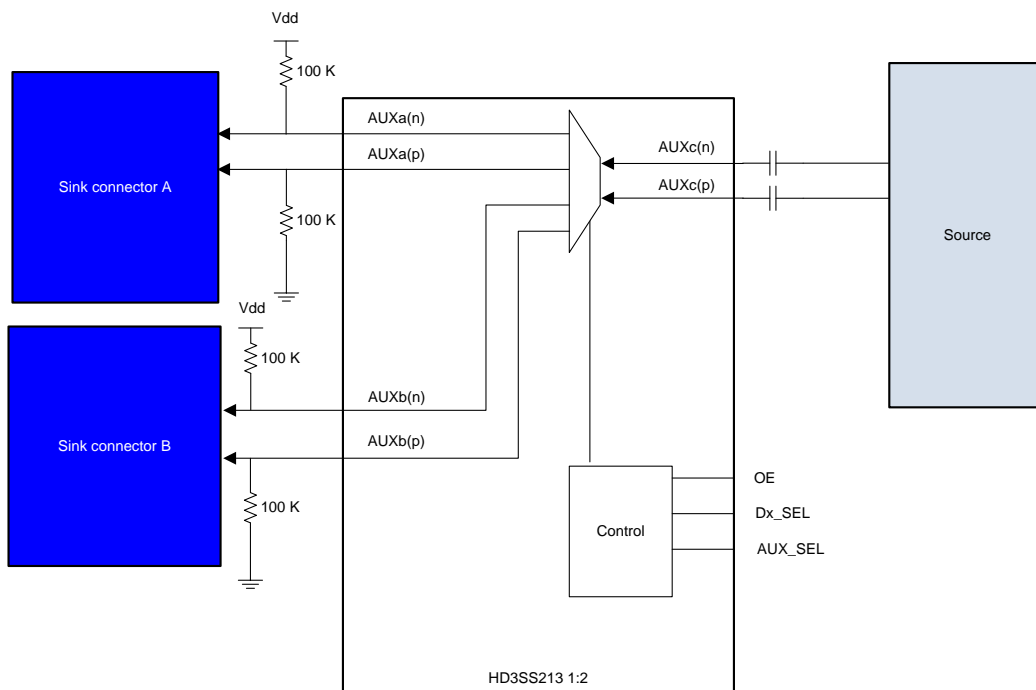


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**Figure 14.  HD3SS213 AUX Channel in 1:2 Application Schematic**

## 9   Power Supply Recommendations

The HD3SS213 requires 3.3 V power sources. 3.3-V supply (VDD) must have 0.1-μF bypass capacitors to VSS (ground) for proper operation. TI recommends one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01 μF are also recommended on the supply terminals.

# 10 Layout

## 10.1 Layout Guidelines

- Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Decoupling capacitors must be placed next to each power terminal on the HD3SS213. Take care to minimize the stub length of the race connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling capacitors.
- Place vias as close as possible to the decoupling capacitor solder pad.
- Widen VDD and/or GND planes to reduce effect if static and dynamic IR drop.

### 10.1.1 Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and lower EMI. Although there seems to be an endless number of precautions, this section provides only a few main recommendations as layout guidance.

1. Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.
2. Reduce inter-pair skew, caused by component placement and IC pinouts, by making larger meandering correction along the signal path. Use chamfered corners with a length-to-trace width ratio of between 3 and 5. The distance between bends must be 8 to 10 times the trace width
3. Use 45° bends instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45° bends is seen as a smaller discontinuity.
4. When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur
5. Place passive components within the signal path, such as source-matching resistors or AC coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b). However, the resulting discontinuity is limited to a far narrower area.
6. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below
7. Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise, they cause the differential impedance to drop below 75 $\Omega$ and fail the board during TDR testing.
8. Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 100 $\Omega$ differential impedance. Large vias and pads can cause the impedance to drop below 85 $\Omega$.
9. Use solid power and ground planes for 100 $\Omega$ impedance control and minimum power noise.
10. For 100 $\Omega$ differential impedance use the smallest trace spacing possible, which is usually specified by the PCB vendor.
11. Keep the trace length between the DisplayPort connector and the DisplayPort device as short as possible to minimize attenuation.
12. Use good DisplayPort connectors whose impedances meet the specifications.
13. Place bulk capacitors (for example, 10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
14. Place smaller 0.1-µF or 0.01-µF capacitors at the device.

## 10.2   Layout Example
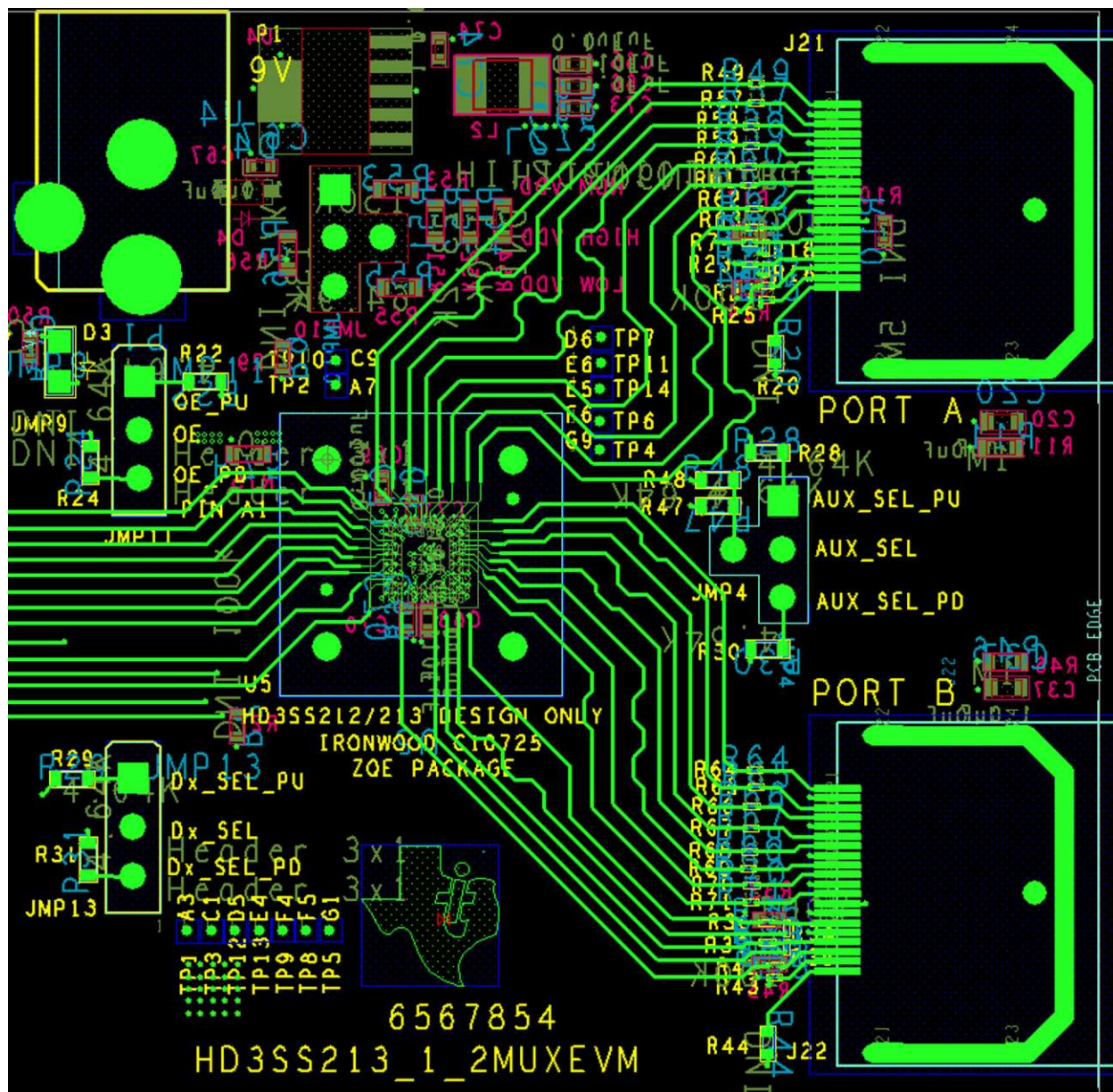


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**Figure 15.  HD3SS213 Layout Example**

# 11 Device and Documentation Support

## 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TEXAS INSTRUMENTS

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| HD3SS213IZQET | PREVIEW | BGA MICROSTAR JUNIOR | ZQE | 50 | 250 | TBD | Call TI | Call TI | | | |
| HD3SS213ZQER | ACTIVE | BGA MICROSTAR JUNIOR | ZQE | 50 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | HD3SS213 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and the leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| HD3SS213ZQER | BGA MICROSTAR JUNIOR | ZQE | 50 | 2500 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| HD3SS213ZQER | BGA MICROSTAR JUNIOR | ZQE | 50 | 2500 | 336.6 | 336.6 | 31.8 |

BALL A1 CORNER
INDEX AREA

5.1
4.9

5.1
4.9

(0.74)

1 MAX

0.25
0.15 TYP

BALL TYP

C

SEATING PLANE

0.08 | C

4 TYP

SYMM
¢

(0.5) TYP

(0.5) TYP

SYMM
¢

4
TYP

50X ∅ 0.35
0.25

∅ 0.15 Ⓜ | C | A Ⓢ | B Ⓢ
∅ 0.05 Ⓜ | C

0.5 TYP

0.5 TYP
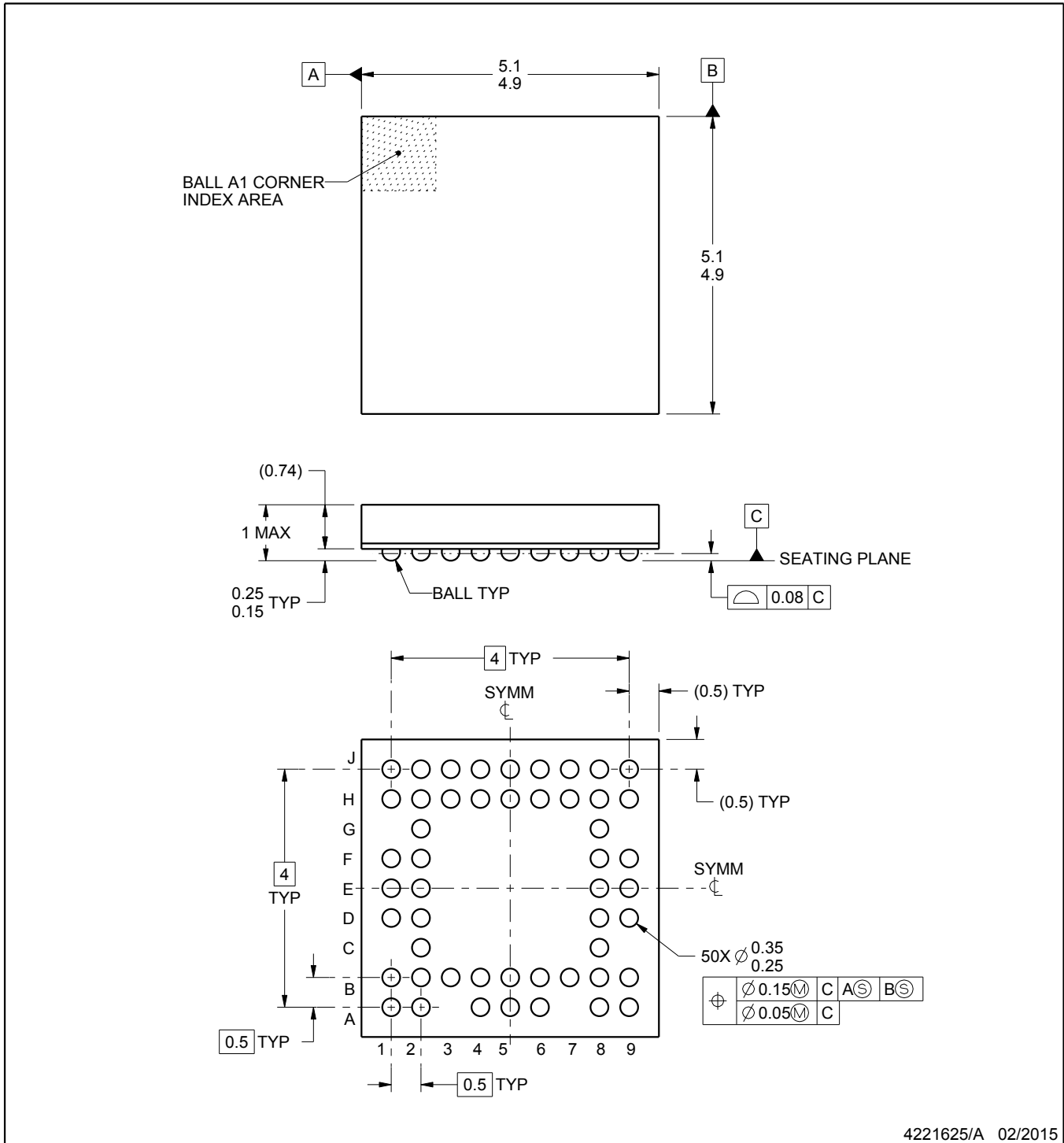
4221625/A   02/2015

MicroStar Junior is trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-225.

## ZQE0050A

## BGA MicroStar Jr ™ - 1 mm max height

PLASTIC BALL GRID ARRAY
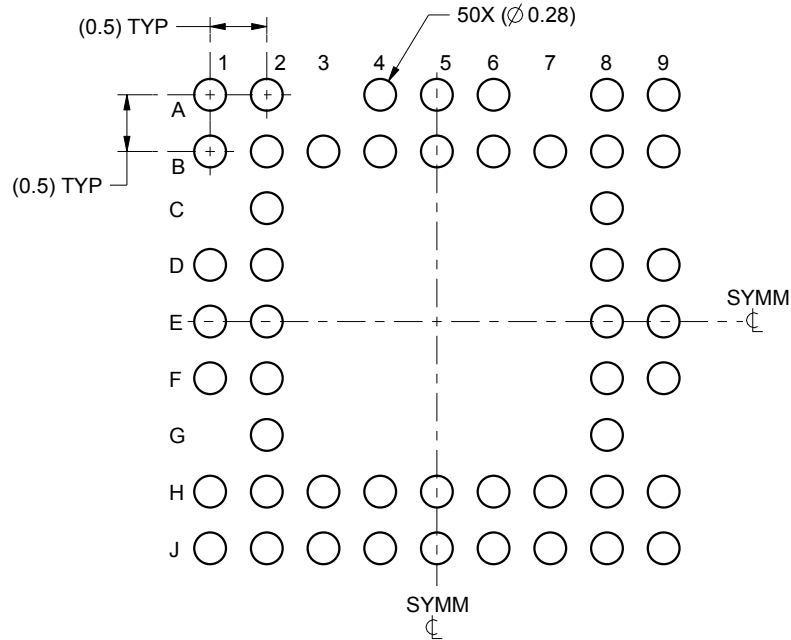


LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

4221625/A   02/2015

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SSYZ015 (www.ti.com/lit/ssyz015).

50X (□ 0.28)

(0.5) TYP

(R0.05) TYP

(0.5) TYP

METAL
TYP

SYMM
℄

SYMM
℄

## SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221625/A   02/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# IMPORTANT NOTICE

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|---|---|---|---|
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| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
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| RFID | www.ti-rfid.com | | |
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