

CSD18512Q5B 40 V N-Channel NexFET™ Power MOSFET

1 Features

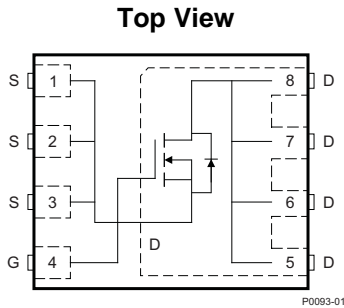
- Low $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen-Free
- SON 5 mm x 6 mm Plastic Package

2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 40 V, 1.3 mΩ, 5 mm x 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain to source voltage	40		V
Q_g	Gate charge total (10 V)	75		nC
Q_{gd}	Gate charge gate to drain	13.3		nC
$R_{DS(on)}$	Drain to source on resistance	$V_{GS} = 4.5\text{ V}$	1.8	mΩ
		$V_{GS} = 10\text{ V}$	1.3	mΩ
$V_{GS(th)}$	Threshold voltage	1.6		V

Ordering Information⁽¹⁾

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18512Q5B	2500	13-Inch Reel	SON 5 mm x 6 mm Plastic Package	Tape and Reel
CSD18512Q5BT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

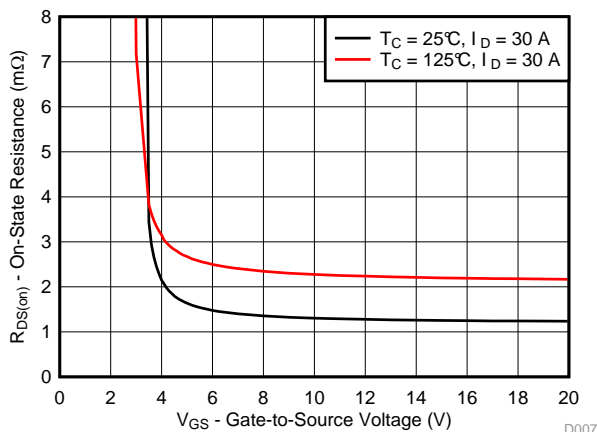
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain to source voltage	40	V
V_{GS}	Gate to source voltage	±20	V
I_D	Continuous drain current (package limited)	100	A
	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	211	
	Continuous drain current ⁽¹⁾	32	
I_{DM}	Pulsed drain current ⁽²⁾	400	A
P_D	Power dissipation ⁽¹⁾	3.1	W
	Power dissipation, $T_C = 25^\circ\text{C}$	139	
T_J, T_{stg}	Operating Junction, Storage Temperature	-55 to 150	°C
E_{AS}	Avalanche energy, single pulse $I_D = 64\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	205	mJ

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1 inch², 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 0.9^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$

$R_{DS(on)}$ vs V_{GS}



Gate Charge

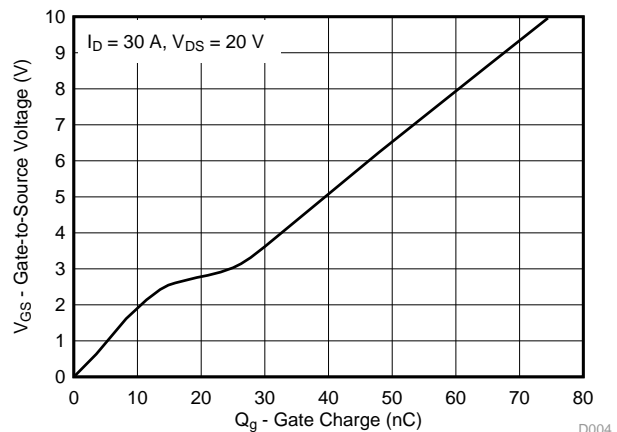


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4 Revision History

DATE	REVISION	NOTES
December 2016	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

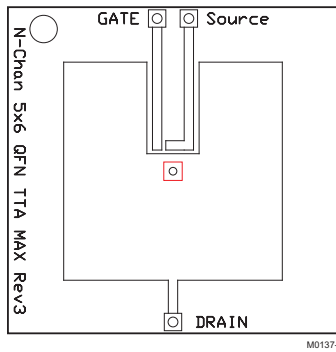
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain to source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
I_{DSS}	Drain to source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 32\text{ V}$			1	μA
I_{GSS}	Gate to source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate to source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.3	1.6	2.2	V
$R_{DS(on)}$	Drain to source on resistance	$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		1.8	2.3	m Ω
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		1.3	1.6	m Ω
g_{fs}	Transconductance	$V_{DS} = 20\text{ V}, I_D = 30\text{ A}$		136		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$		5480	7120	pF
C_{oss}	Output capacitance			537	699	pF
C_{rss}	Reverse transfer capacitance			256	333	pF
R_G	Series gate resistance			1.0	2.0	Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 20\text{ V}, I_D = 30\text{ A}$		37	48	nC
Q_g	Gate charge total (10 V)			75	98	nC
Q_{gd}	Gate charge gate to drain			13.3		nC
Q_{gs}	Gate charge gate to source			15.1		nC
$Q_{g(th)}$	Gate charge at V_{th}			8.2		nC
Q_{oss}	Output charge		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		23	
$t_{d(on)}$	Turn on delay time	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 30\text{ A}, R_G = 0\ \Omega$		7		ns
t_r	Rise time			16		ns
$t_{d(off)}$	Turn off delay time			31		ns
t_f	Fall time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 30\text{ A}, V_{GS} = 0\text{ V}$		0.75	1.0	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 20\text{ V}, I_F = 30\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		22		nC
t_{rr}	Reverse recovery time			17		ns

5.2 Thermal Information

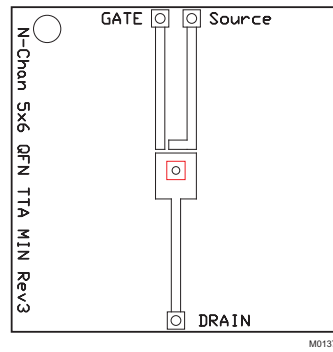
($T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case (top of package) thermal resistance ⁽¹⁾			0.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			50	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2
oz. (0.071 mm thick)
Cu.



Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of 2
oz. (0.071 mm thick)
Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)

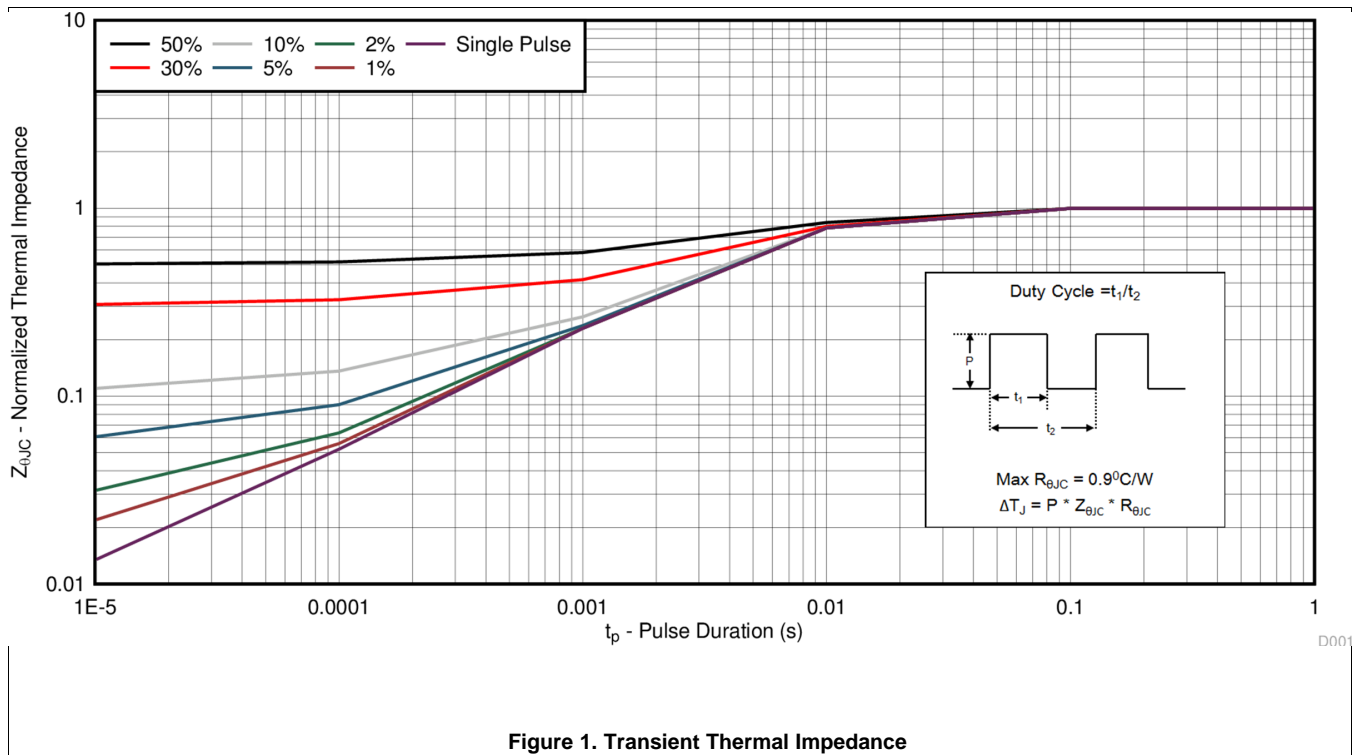
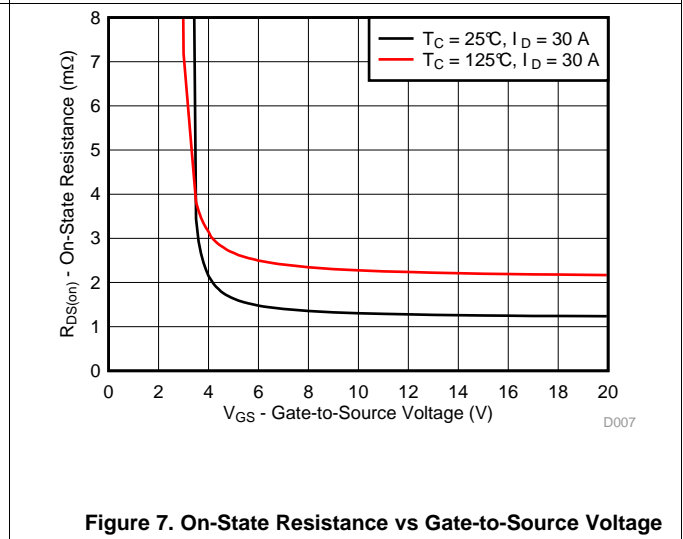
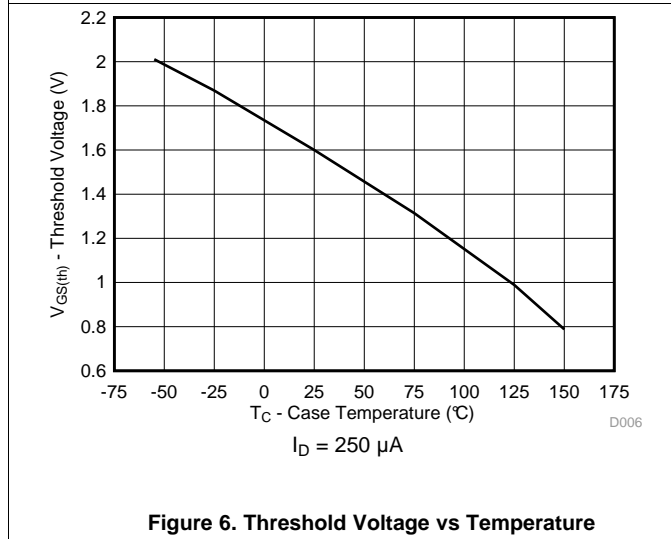
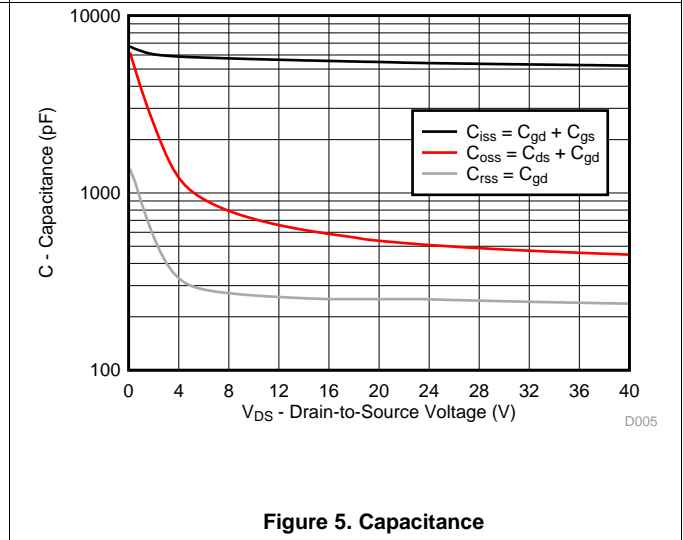
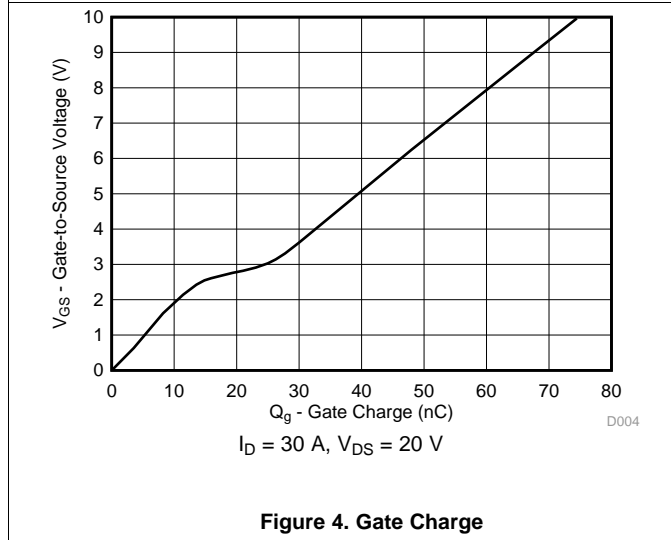
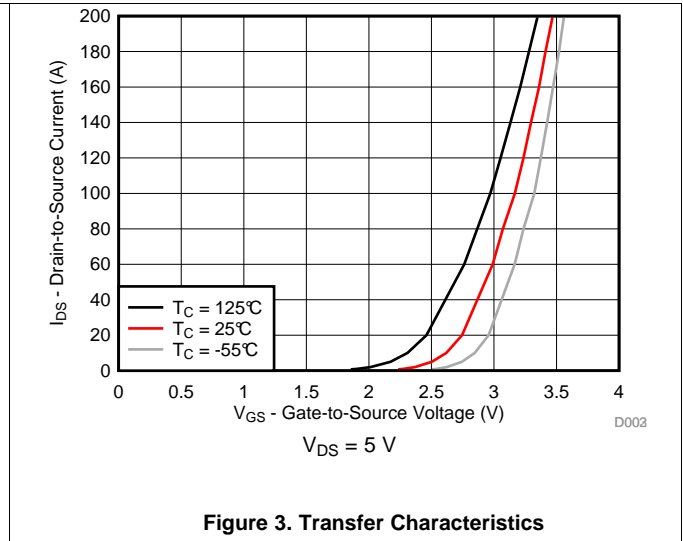
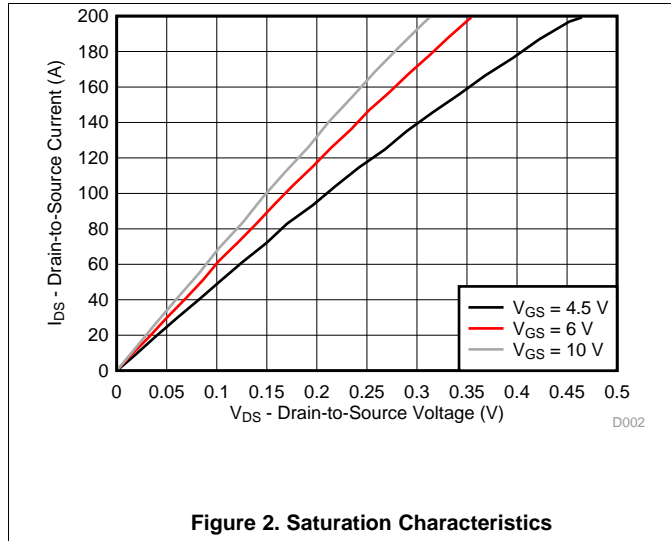


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

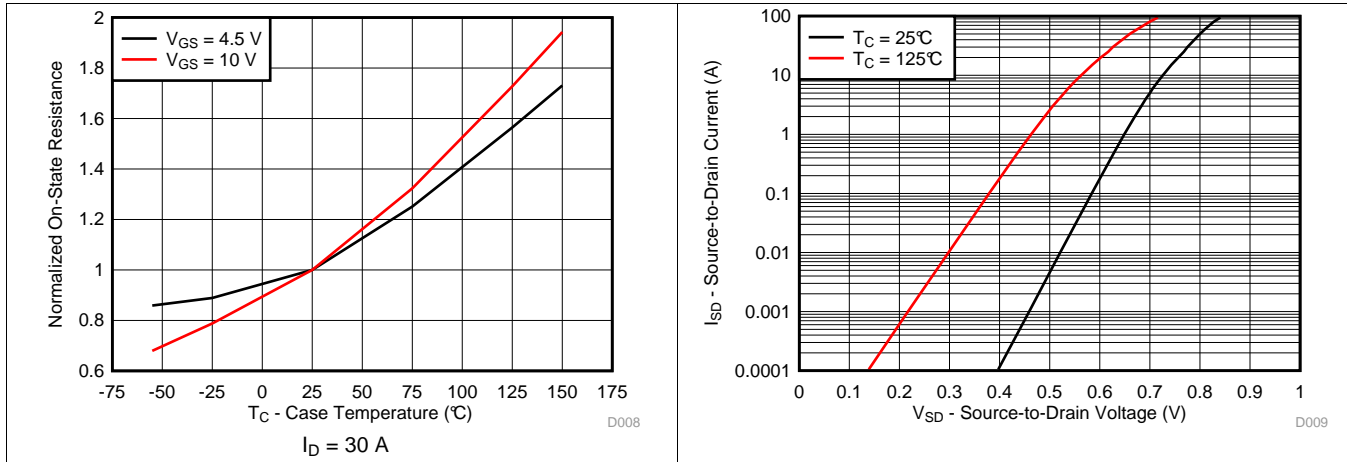


Figure 8. Normalized On-State Resistance vs Temperature

Figure 9. Typical Diode Forward Voltage

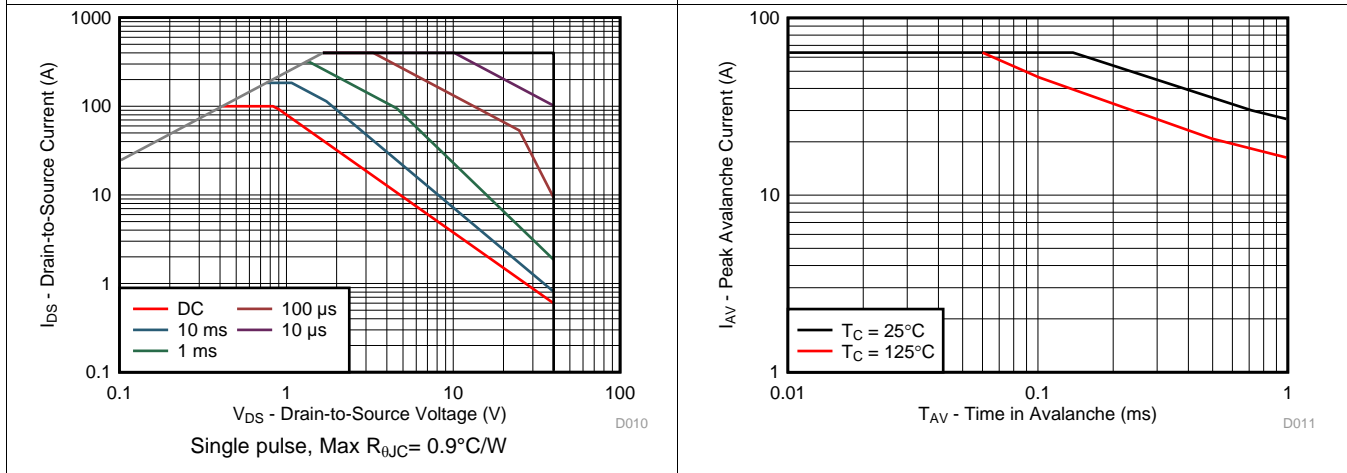


Figure 10. Maximum Safe Operating Area

Figure 11. Single Pulse Unclamped Inductive Switching

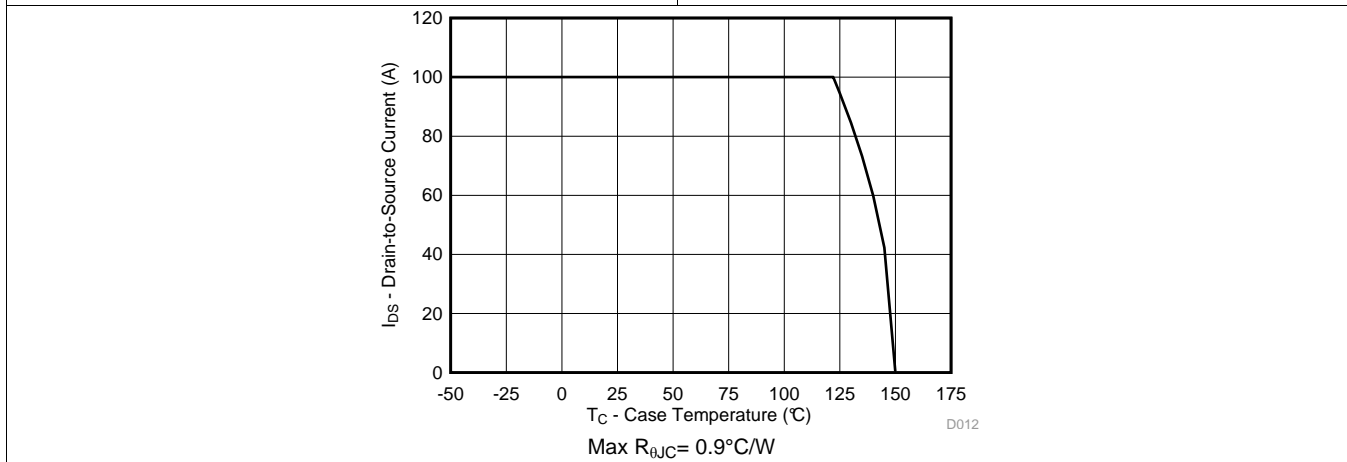


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

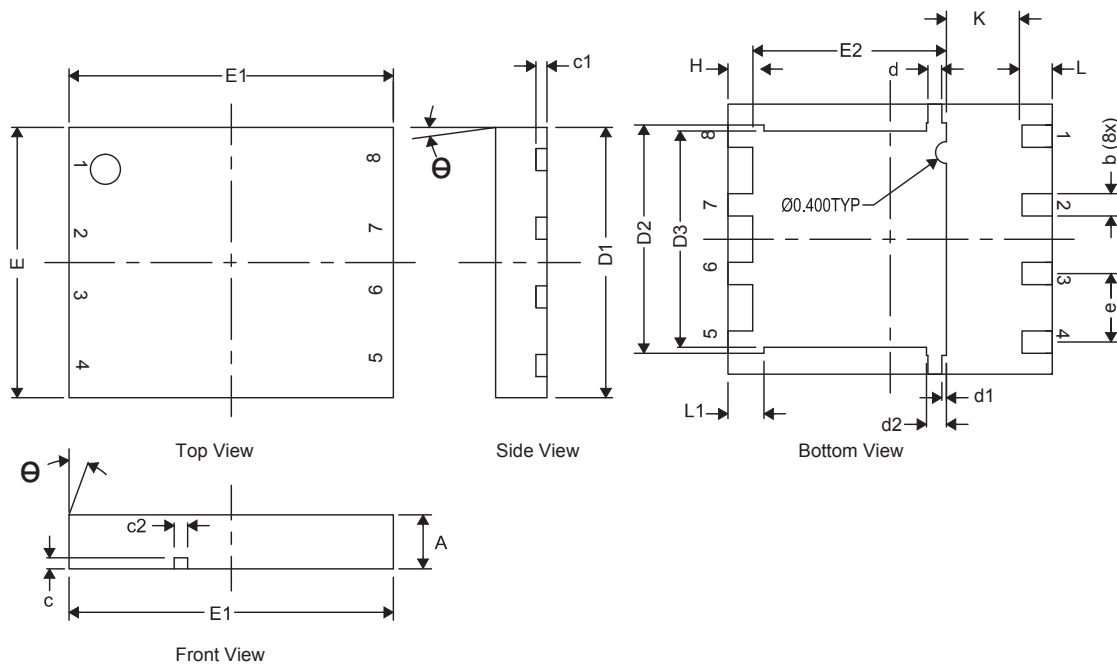
6.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

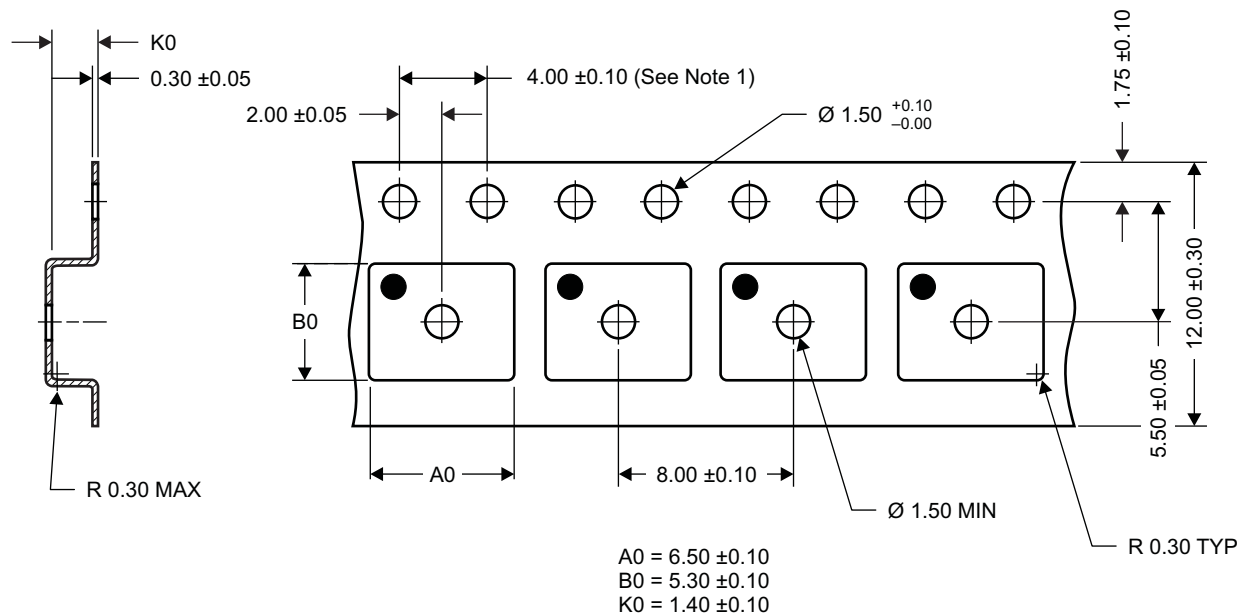
7 Mechanical, Packaging, and Orderable Information

7.1 Q5B Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 TYP		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	-	-
K	1.40 TYP		

7.4 Q5B Tape and Reel Information



M0138-01

Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2 .
- Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
- Material: black static-dissipative polystyrene.
- All dimensions are in mm (unless otherwise specified).
- $A0$ and $B0$ measured on a plane 0.3 mm above the bottom of the pocket.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18512Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18512	Samples
CSD18512Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18512	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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