

SN74CB3Q3305 Dual FET Bus Switch

2.5-V/3.3-V Low-Voltage High-Bandwidth Bus Switch

1 Features

- High-Bandwidth Data Path (Up to 500 MHz⁽¹⁾)
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range ($r_{on} = 3 \Omega$ Typical)
- Rail-to-Rail Switching on Data I/O Ports
 - 0- to 5-V Switching With 3.3-V V_{CC}
 - 0- to 3.3-V Switching With 2.5-V V_{CC}
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 3.5$ pF Typical)
- Fast Switching Frequency ($f_{OE} = 20$ MHz Maximum)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 0.25$ mA Typical)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

⁽¹⁾ For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, [SCDA008](#).

2 Applications

- IP Phones: Wired and Wireless
- Optical Modules
- Optical Networking: Video Over Fiber and EPON
- Private Branch Exchange (PBX)
- WiMAX and Wireless Infrastructure Equipment
- USB, Differential Signal interface
- Bus isolation

3 Description

The SN74CB3Q3305 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3305 device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

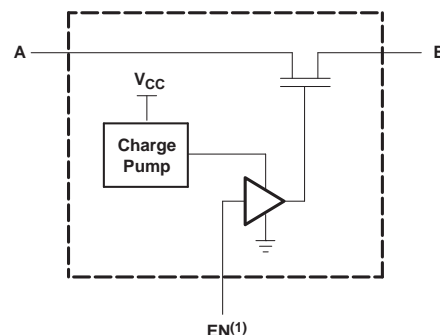
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CB3Q3305	VSSOP (8)	2.00 mm × 3.10 mm
	TSSOP (8)	3.00 mm × 6.10 mm

⁽¹⁾ For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic, Each FET Switch (SW)



⁽¹⁾ EN is the internal enable signal applied to the switch.



Table of Contents

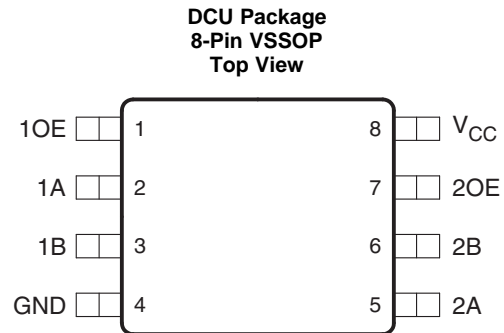
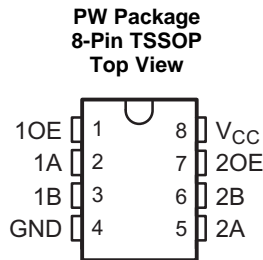
1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Pin Configuration and Functions 3 6 Specifications 3 6.1 Absolute Maximum Ratings 3 6.2 ESD Ratings..... 4 6.3 Recommended Operating Conditions 4 6.4 Thermal Information 4 6.5 Electrical Characteristics..... 4 6.6 Switching Characteristics 5 6.7 Typical Characteristics 6 7 Parameter Measurement Information 7 8 Detailed Description 8 8.1 Overview 8 8.2 Functional Block Diagram 8	8.3 Feature Description..... 8 8.4 Device Functional Modes..... 8 9 Application and Implementation 9 9.1 Application Information..... 9 9.2 Typical Application 9 10 Power Supply Recommendations 10 11 Layout 10 11.1 Layout Guidelines 10 11.2 Layout Example 10 12 Device and Documentation Support 11 12.1 Documentation Support 11 12.2 Community Resources..... 11 12.3 Trademarks 11 12.4 Electrostatic Discharge Caution..... 11 12.5 Glossary 11 13 Mechanical, Packaging, and Orderable Information 11
---	--

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2009) to Revision C	Page
<ul style="list-style-type: none"> • Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I/O	Channel 1 A port
1B	3	I/O	Channel 1 B port
1OE	1	I	Output Enable for switch 1
2A	5	I/O	Channel 2 A port
2B	6	I/O	Channel 2 B port
2OE	7	I	Output Enable for switch 2
GND	4	—	Ground
V _{CC}	8	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
V _{CC} Supply voltage	−0.5	4.6	V
V _{IN} Control input voltage ⁽²⁾⁽³⁾	−0.5	7	V
V _{I/O} Switch I/O voltage ⁽²⁾⁽³⁾⁽⁴⁾	−0.5	7	V
I _{IK} Control input clamp current		−50	mA
I _{I/O} K I/O port clamp current		−50	mA
I _{I/O} ON-state switch current ⁽⁵⁾		±64	mA
Continuous current through V _{CC} or GND		±100	mA
θ _{JA} Package thermal impedance ⁽⁶⁾		88	°C/W
T _j Junction temperature		150	°C
T _{stg} Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) V_I and V_O are used to denote specific conditions for V_{I/O}.

(5) I_I and I_O are used to denote specific conditions for I_{I/O}.

(6) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	
V_{IO}	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74CB3Q3305	SN74CB3Q3305	UNIT
		DCU (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183	190.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.2	74.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.5	119.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	120.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.1	117.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3.6\text{ V}$,	$I_I = -18\text{ mA}$				-1.8	V
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$,	$V_{IN} = 0\text{ to }5.5\text{ V}$				±1	μA
$I_{OZ}^{(3)}$		$V_{CC} = 3.6\text{ V}$,	$V_O = 0\text{ to }5.5\text{ V}$, $V_I = 0$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$			±1	μA
I_{off}		$V_{CC} = 0$,	$V_O = 0\text{ to }5.5\text{ V}$,	$V_I = 0$			1	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$,	$I_{IO} = 0$, Switch ON or OFF,	$V_{IN} = V_{CC}\text{ or GND}$		0.25	0.7	mA
$\Delta I_{CC}^{(4)}$	Control inputs	$V_{CC} = 3.6\text{ V}$, One input at 3 V, Other inputs at V_{CC} or GND					25	μA
$I_{CCD}^{(5)}$	Per control input	$V_{CC} = 3.6\text{ V}$,	A and B ports open, Control input switching at 50% duty cycle			0.040	0.045	mA/ MHz

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see [Figure 5](#)).

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
C _{in}	Control inputs	V _{CC} = 3.3 V,	V _{IN} = 5.5 V, 3.3 V, or 0		2.5	3.5	pF
C _{io(OFF)}		V _{CC} = 3.3 V,	Switch OFF, V _{IN} = V _{CC} or GND,		3.5	5	pF
C _{io(ON)}		V _{CC} = 3.3 V,	Switch ON, V _{IN} = V _{CC} or GND,		8	10.5	pF
r _{on} ⁽⁶⁾	V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V	V _I = 0, I _O = 30 mA			3	8	Ω
		V _I = 1.7 V, I _O = -15 mA			3.5	9	
	V _{CC} = 3 V	V _I = 0, I _O = 30 mA			3	6	
		V _I = 2.4 V, I _O = -15 mA			3.5	8	

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	MIN	MAX	UNIT
f _{OE} ⁽¹⁾	OE	A or B	V _{CC} = 2.5 V ± 0.2 V		10	MHz
			V _{CC} = 3.3 V ± 0.3 V		20	
t _{pd} ⁽²⁾	A or B	B or A	V _{CC} = 2.5 V ± 0.2 V		0.09	ns
			V _{CC} = 3.3 V ± 0.3 V		0.15	
t _{en}	OE	A or B	V _{CC} = 2.5 V ± 0.2 V	1	5	ns
			V _{CC} = 3.3 V ± 0.3 V	1	4.5	
t _{dis}	OE	A or B	V _{CC} = 2.5 V ± 0.2 V	1	4.5	ns
			V _{CC} = 3.3 V ± 0.3 V	1	5	

(1) Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0).

(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristics

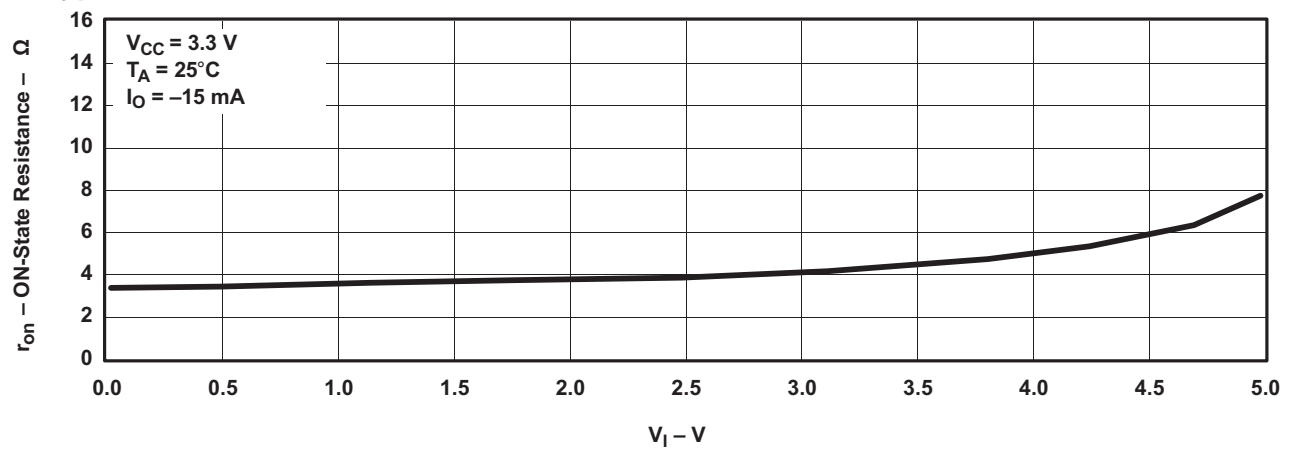
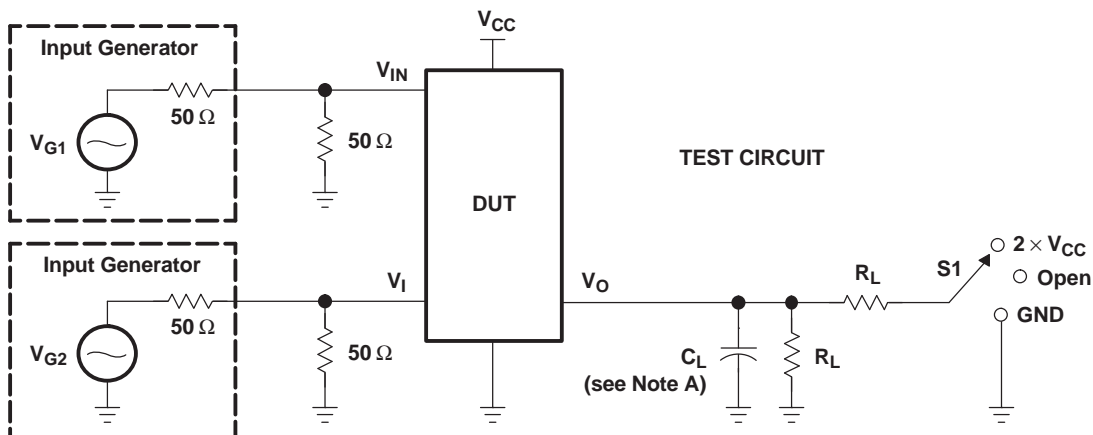
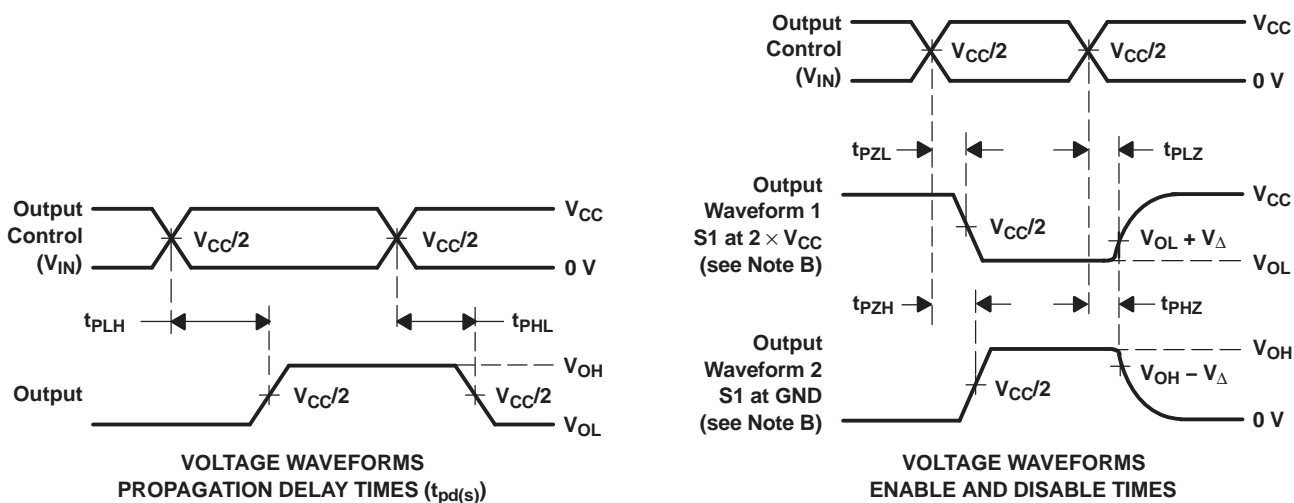


Figure 1. Typical r_{on} vs V_I

7 Parameter Measurement Information



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V	Open	500 Ω	V _{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × V _{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V _{CC}	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V _{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V _{CC}	50 pF	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PZH} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CB3Q3305 device is organized as two 1-bit switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF and a high-impedance state exists between the A and B ports.

8.2 Functional Block Diagram

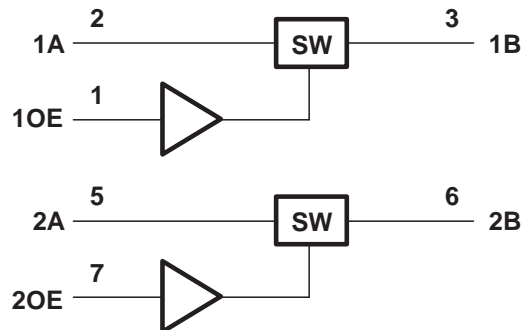


Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

The device supports High-Bandwidth data path up to 500 MHz. The I/O ports are 5-V tolerant when powered up or powered down due to I_{OFF} . The charge pump creates low and flat ON-state resistance characteristics over the whole operating temperature range.

Rail-to-Rail switching on data I/O ports is 0-V to 5-V with 3.3-V V_{CC} or 0-V to 3.3-V with 2.5-V V_{CC}

The data flow is bidirectional with near-zero propagation delay. Reduced input/output capacitance for higher speed applications. OE can be toggled at the high speeds of 20 MHz for fast switching applications.

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74CB3Q3305.

Table 1. Function Table (Each Bus Switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CB3Q3305 can be used as bidirectional switch as shown in the application [Figure 4](#). The master operates at 5 V and the slave can accept 5 V. With 3 V_{CC} on the device, the two ports can be connected. OE pin is used to control the chip from Master controller. This is a very generic example and could apply to many situations. If an application requires 1 bit, tie the OE to low and the ports A and B side to either high or low (not shown).

9.2 Typical Application

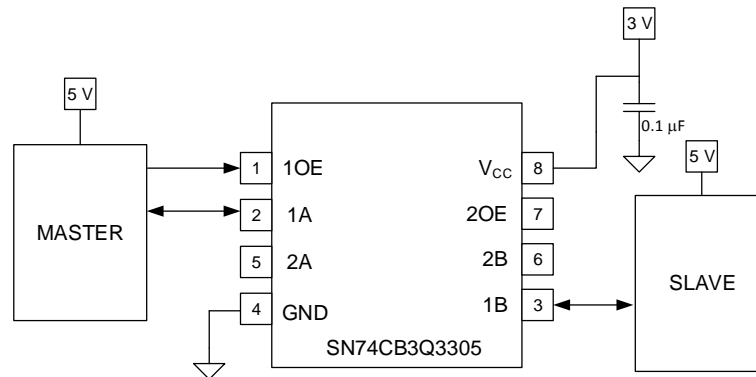


Figure 4. Typical Application of the SN74CB3Q3305

9.2.1 Design Requirements

- Recommended Input Conditions:
 - For specified high and low levels, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#)⁽¹⁾.
 - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Absolute Maximum Conditions:
 - I/O currents should not exceed ± 64 mA per channel.
 - Continuous current through GND or V_{CC} should not exceed ± 100 mA.
- Frequency Selection Criterion:
 - Maximum frequency tested is 500 MHz.
 - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in [Layout](#).

9.2.2 Detailed Design Procedure

The 0.1- μ F capacitor should be placed as close as possible to the device.

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs, SCBA004](#).

Typical Application (continued)

9.2.3 Application Curve

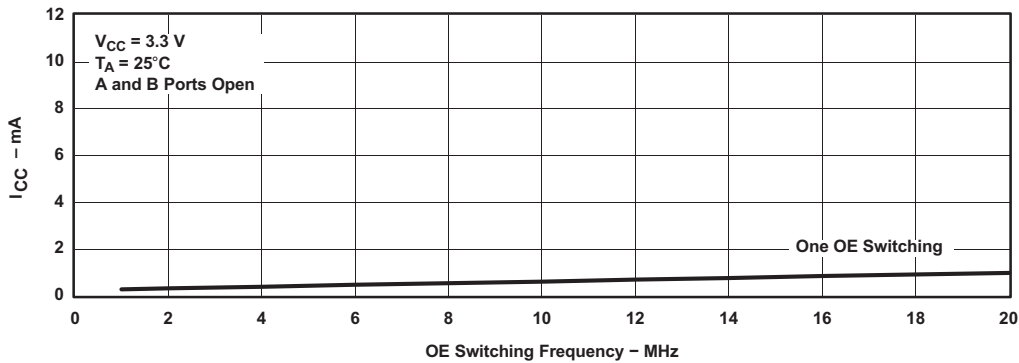


Figure 5. Typical I_{CC} vs OE Switching Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Absolute Maximum Ratings](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 6](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

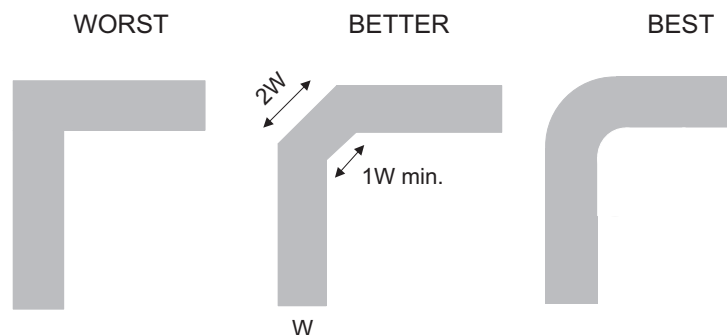


Figure 6. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *CBT-C, CB3T, and CB3Q Signal-Switch Families*, [SCDA008](#)
- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *Selecting the Right Texas Instruments Signal Switch*, [SZZA030](#)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CB3Q3305DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GARR	Samples
SN74CB3Q3305DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	(GARQ ~ GARR)	Samples
SN74CB3Q3305PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3305PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3305PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
SN74CB3Q3305PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

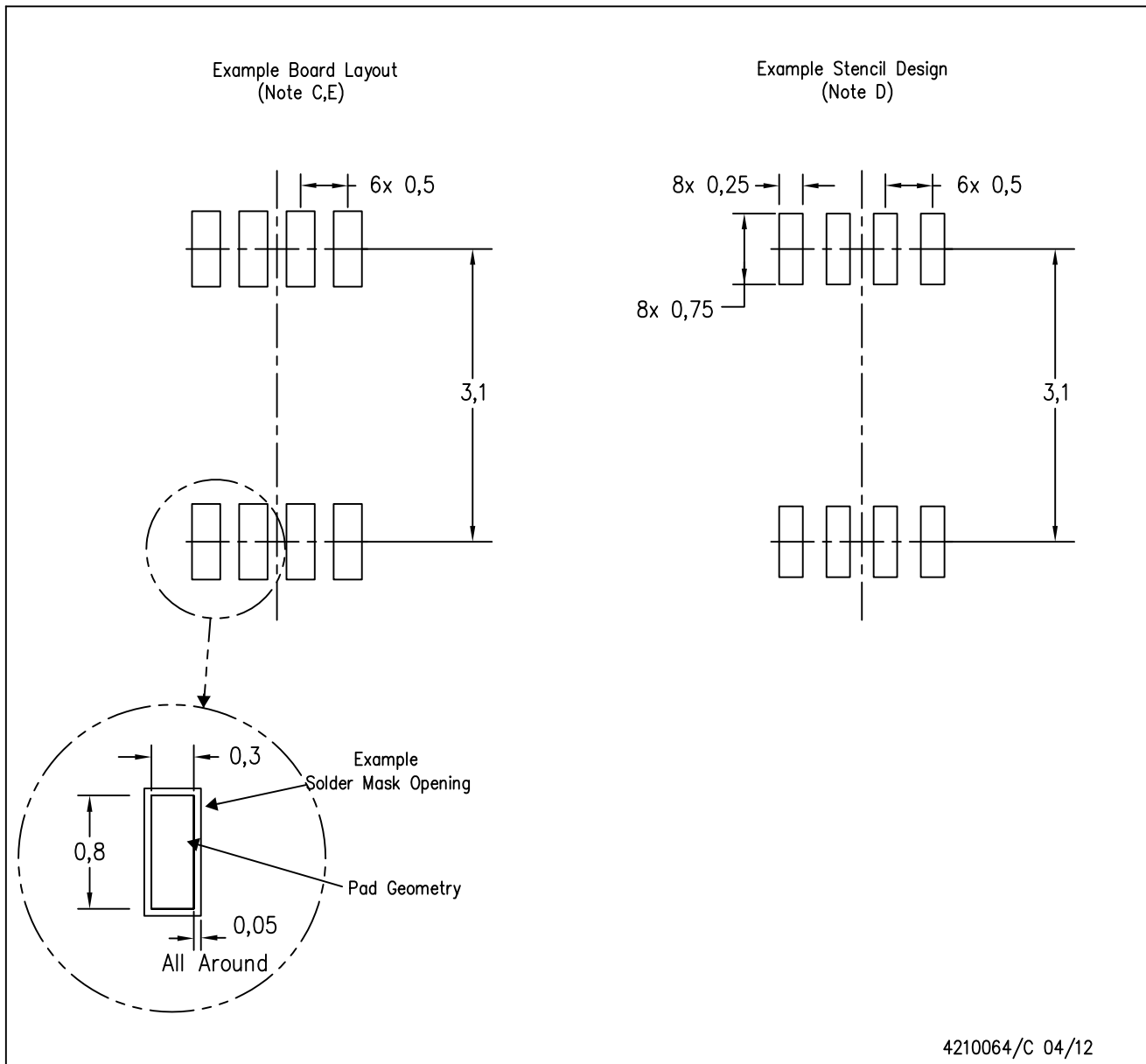
4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.