# MC14576C
# MC14577C

*Advance Information*

# Dual Video Amplifiers

## CMOS

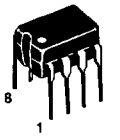
Each of these devices contains two amplifiers realized in CMOS. Each amp also employs two lateral NPN bipolar transistors.

The MC14576 contains two internally–compensated operational amplifiers. On–chip gain–setting resistors result in a noninverting voltage gain of 6.0 dB ± 1.0 dB at 4.43 MHz for each amp. Each noninverting input of the MC14576 appears as a mostly–capacitive load of about 10 pF.

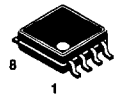
The MC14577 also contains two internally–compensated operational amplifiers. However, the gain for each amp is adjustable with external components. (The value of the closed–loop voltage gain with a 150 Ω load should not exceed 10 dB at 5 MHz and 6 dB at 10 MHz.) All inputs of the MC14577 appear as mostly–capacitive loads of about 10 pF.

*The MC14576C and MC14577C are drop–in replacements for the MC14576B and MC14577B, respectively.*

- Direct Drive of 150 Ω Loads
- Maximum Supply Current: 40 mA per Package
- Operating Voltage Range — P Suffix: 5.0 to 12 V Relative to $V_{SS}$
  F Suffix: 5.0 to 10 V Relative to $V_{SS}$
- May Be Used with Single or Dual Supplies
- Operating Temperature Range — P Suffix: – 20 to 70°C
  F Suffix: – 20 to 50°C
- Excellent Differential Gain: 3% Maximum @ 4.43 MHz
- Excellent Differential Phase: 3° Maximum @ 4.43 MHz
- Guaranteed Bandwidth: 10 MHz
- Minimal External Components Required



**P SUFFIX**
PLASTIC DIP
CASE 626–05

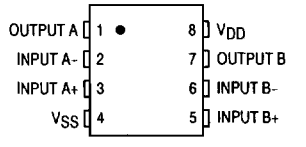


**F SUFFIX**
SOG PACKAGE
CASE 904–01

**ORDERING INFORMATION**

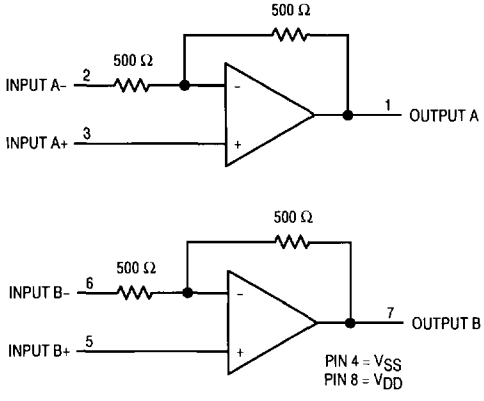
| | |
|---|---|
| MC14576CP, MC14577CP | Plastic DIP |
| MC14576CF, MC14577CF | SOG Package |

**PIN ASSIGNMENT**

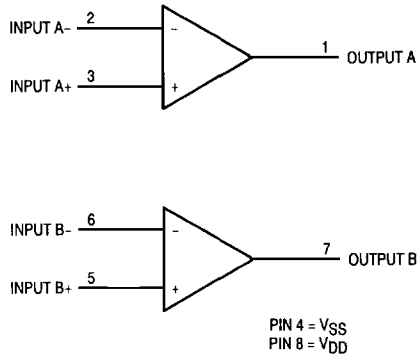



**SYMBOLIC REPRESENTATIONS**

**MC14576**




**MC14577**




NOTE: Resistors are shown above with nominal values.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**MAXIMUM RATINGS** (See Note)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage (Referenced to $V_{SS}$) | – 0.5 to + 14 | V |
| $V_{in}$ | DC Input Voltage | $V_{SS}$ – 0.5 to $V_{DD}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage | $V_{SS}$ – 0.5 to $V_{DD}$ + 0.5 | V |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature (10–Second Soldering) | 260 | °C |

NOTE: Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

2

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, Reference Figures 1 and 2, $R_L$ = 150 Ω Unless Otherwise Indicated)

| Symbol | Parameter | Test Condition | $V_{DD}$ V | $V_{SS}$ V | Guaranteed Limit | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage Range (Referenced to $V_{SS}$) P Suffix<br>F Suffix | | —<br>— | —<br>— | 5.0 to 12<br>5.0 to 10 | V |
| $I_{DD}$ | Maximum Power Supply Current (Per Package) | $V_{in}$ = 0 V, $R_L$ = ∞ (open) | + 5.0 | – 5.0 | 40 | mA |
| N | Maximum Output Noise | $V_{in}$ = 0 V, BW = 30 Hz to 25 MHz | + 5.0 | – 5.0 | 250 | μV RMS |
| $A_V$ | Closed–Loop Voltage Gain | $V_{in}$ = 2.0 V p–p, f = 4.43 MHz | + 5.0 | – 5.0 | 5.0 to 7.0 | dB |
| BW | Bandwidth | $V_{in}$ = 2.0 V p–p, $A_V$ within ± 3.0 dB of the gain at 4.43 MHz | + 5.0 | – 5.0 | 10 | MHz |
| $V_{out}$ | Minimum Output Voltage Swing | $V_{in}$ = 4.0 V p–p, f = 10 MHz | + 5.0 | – 5.0 | 3.5 | V p–p |
| | | $V_{in}$ = 1.5 V p–p, f = 5.0 MHz | + 2.5 | – 2.5 | 2.0 | |
| — | Maximum Differential Gain | $V_{in}$ = 300 mV p–p biased from – 0.5 to + 0.5 V, f = 4.43 MHz | + 5.0 | – 5.0 | 3.0 | % |
| — | Maximum Differential Phase | $V_{in}$ = 300 mV p–p biased from – 0.5 to + 0.5 V, f = 4.43 MHz | + 5.0 | – 5.0 | 3.0 | Degrees |
| PSRR | Minimum Power Supply Rejection Ratio, $V_{DD}$ or $V_{SS}$ pins | $V_{in}$ = 0 V, $\Delta V_{DD}$ or $\Delta V_{SS}$ = 400 mV p–p @ 100 kHz | + 5.0 | – 5.0 | 43 | dB |
| — | Minimum Channel Separation | $V_{in}$ = 1.0 V p–p, f = 4.43 MHz | + 5.0 | – 5.0 | 40 | dB |
| $C_{in}$ | Maximum Input Capacitance | $V_{in}$ = 1.0 V p–p, f = 4.43 MHz | + 5.0 | – 5.0 | 10** | pF |
| $R_{in}$ | Minimum Input Resistance, all Inputs except Input A– and Input B– of the MC14576 | | + 5.0 | – 5.0 | $10^9$** | Ω |

** Typical value only; not guaranteed.

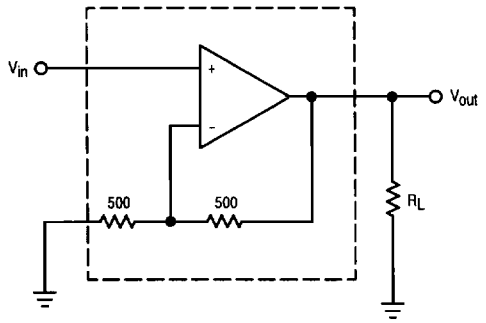



Figure 1. MC14576 Test Circuit

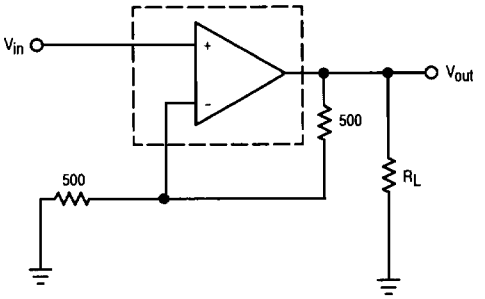



Figure 2. MC14577 Test Circuit



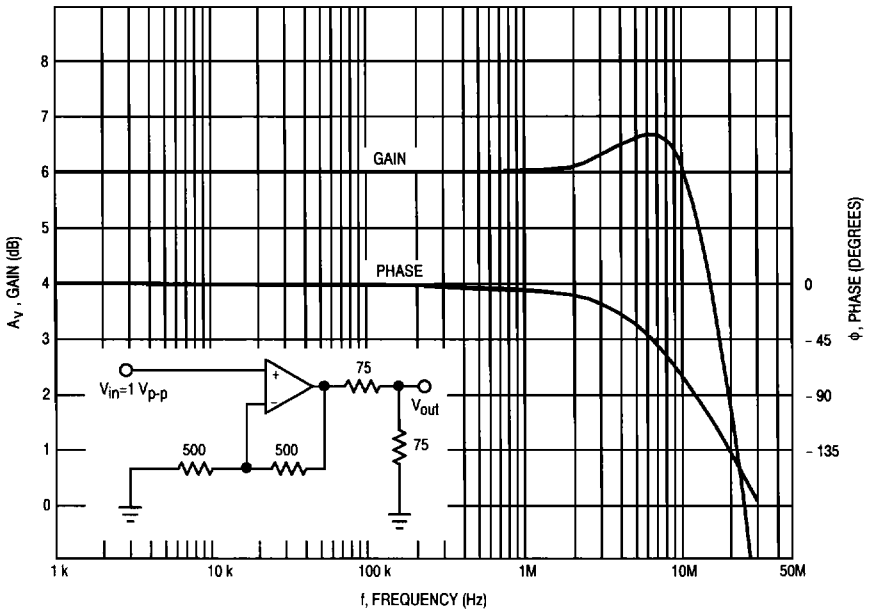



Figure 3. Typical Gain/Phase–Frequency Response (Not Guaranteed)

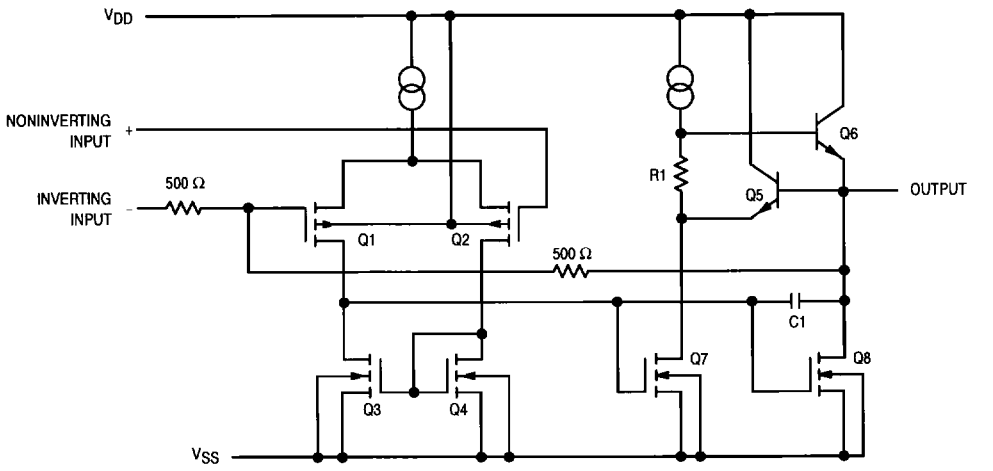



**Figure 4. MC14576 Schematic**

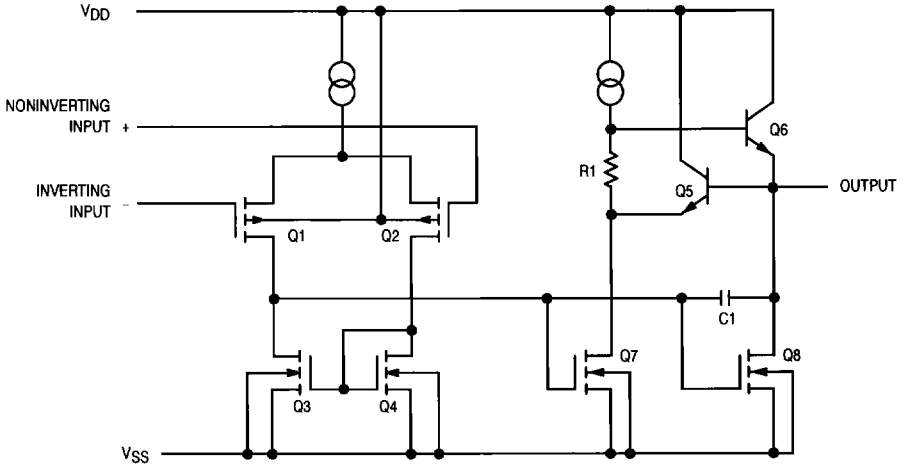



**Figure 5. MC14577 Schematic**

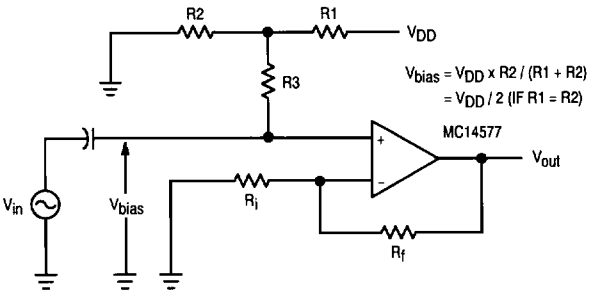



**Figure 6. AC–Coupled Noninverting Amplifier with Single–Supply Operation**

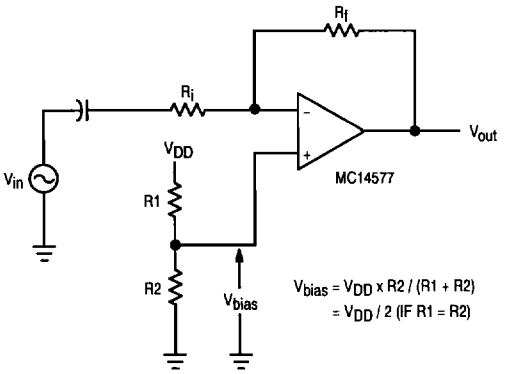



**Figure 7. AC–Coupled Inverting Amplifier with Single–Supply Operation**

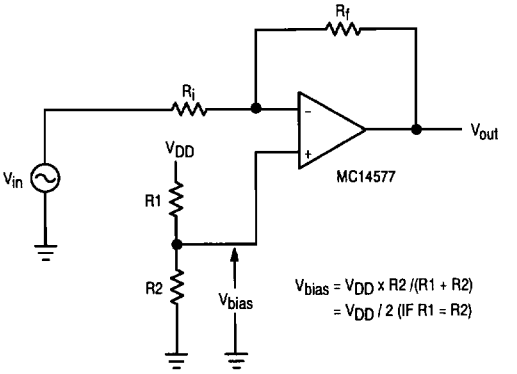



**Figure 8. DC–Coupled Inverting Amplifier with Single–Supply Operation**

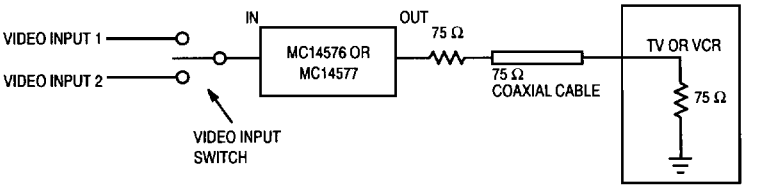



**Figure 9. Typical Application**

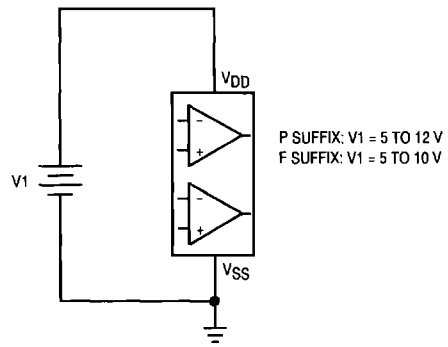



**Figure 10. Single–Supply Operation**

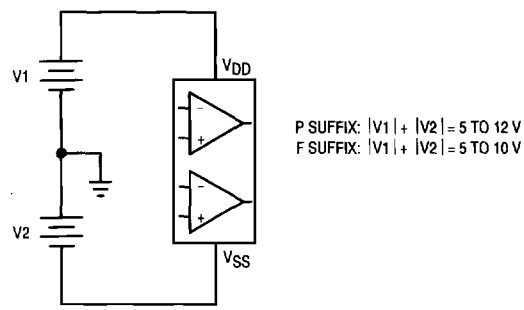



**Figure 11. Dual– or Split–Supply Operation**

## EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 13. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 13. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 12 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

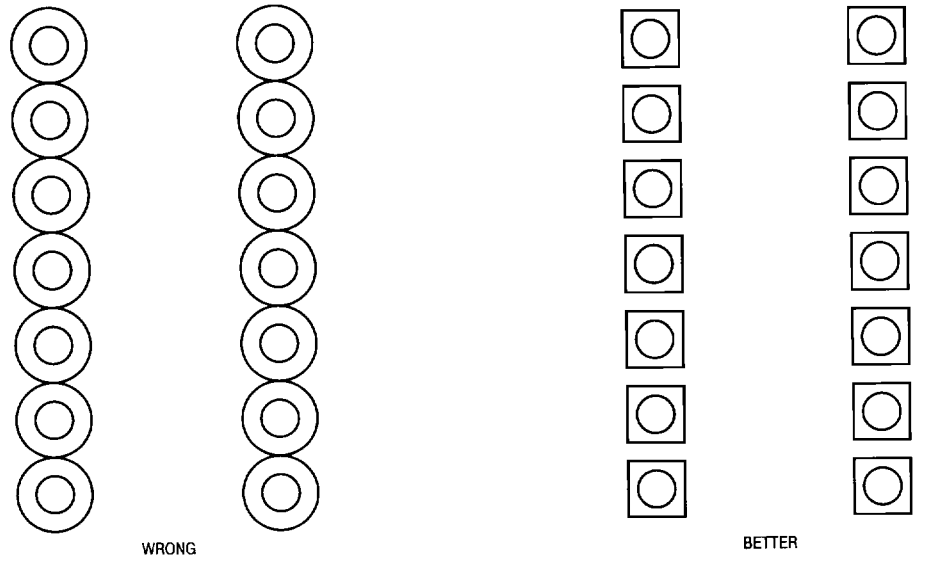



**Figure 12.**

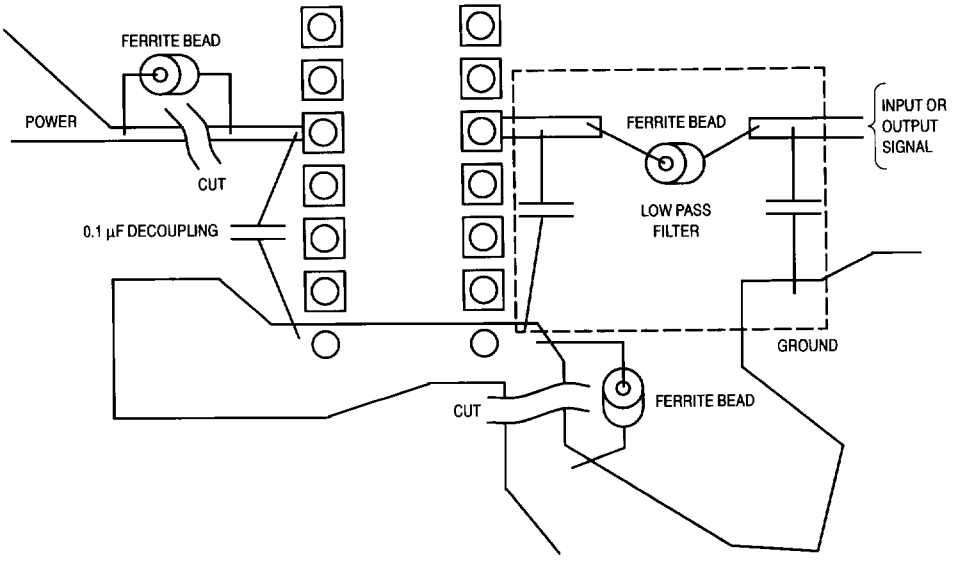



**Figure 13.**