

30V N-Channel MOSFET
N-Channel Enhancement Mode Power MOSFET
General Features

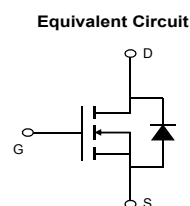
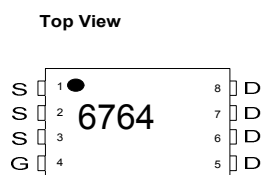
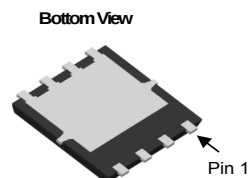
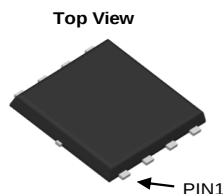
V_{DS}	30V
I_D (at $V_{GS}=10V$)	85A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 4.00m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 5.00m Ω

100% UIS Tested
100% Rg Tested

- Trench Power α MOS Technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial

PDFN5X6-8L


Orderable Part Number		Package Type		Form	Minimum Order Quantity
JSM6764		DFN 5x6		Tape&Reel	3000
Absolute Maximum Ratings T _A =25°C unless otherwise noted					
Parameter		Symbol	Maximum		Units
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	±12		V
Continuous Drain Current ^G	T _C =25°C	I _D	85		A
Pulsed Drain Current ^C		I _{DM}	190		
Continuous Drain Current	T _A =25°C	I _{DSM}	37		A
Avalanche Current ^C		I _{AS}	42		A
Avalanche energy L=0.05mH ^C		E _{AS}	44		mJ
V _{DS} Spike	10μs	V _{SPIKE}	36		V
Power Dissipation ^B	T _C =25°C	P _D	42		W
Power Dissipation ^A	T _A =25°C	P _{DSM}	6.2		W
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150		°C
Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	t ≤ 10s	R _{θJA}	15	20	°C/W
Maximum Junction-to-Ambient ^{A,D}	Steady-State		40	50	°C/W
Maximum Junction-to-Case	Steady-State	R _{θJC}	2.4	3	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=10\text{mA}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$			0.5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.1	1.5	1.9	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$		3.8	4.0	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		4.5	5.0	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		167		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.5	0.7	V
I_S	Maximum Body-Diode Continuous Current				30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		2120		pF
C_{oss}	Output Capacitance			700		pF
C_{rss}	Reverse Transfer Capacitance			69		pF
R_g	Gate resistance	$f=1\text{MHz}$	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=20\text{A}$		37		nC
$Q_g(4.5\text{V})$	Total Gate Charge			16.8		nC
Q_{gs}	Gate Source Charge			5		nC
Q_{gd}	Gate Drain Charge			4.9		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=0.75\Omega$, $R_{GEN}=3\Omega$		7		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(off)}$	Turn-Off DelayTime			36		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		15.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		33		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.

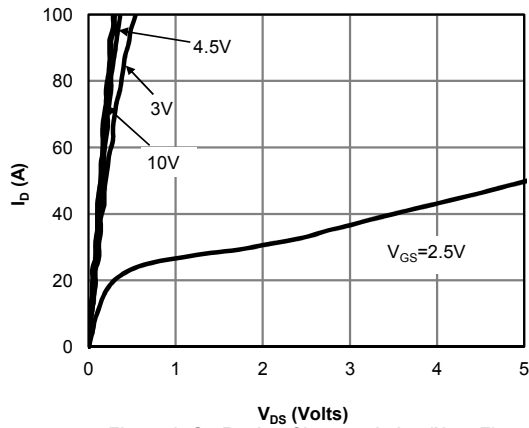
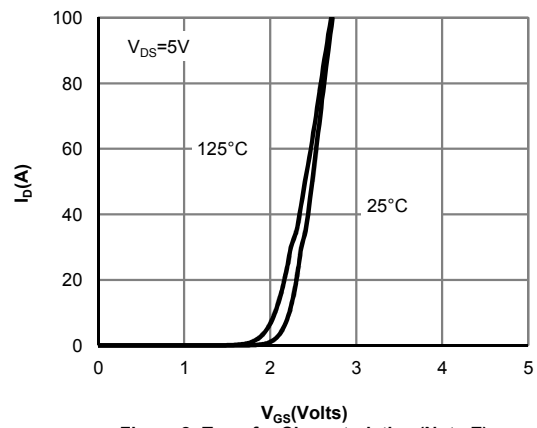
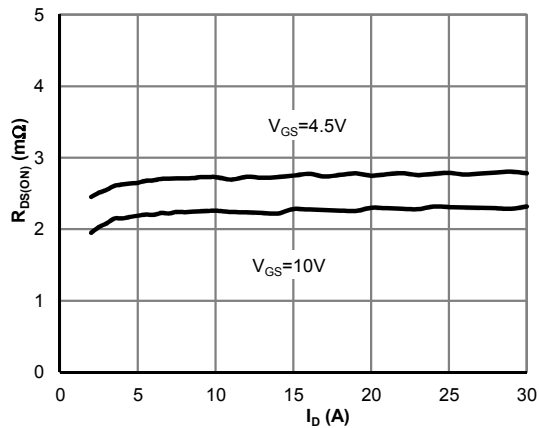
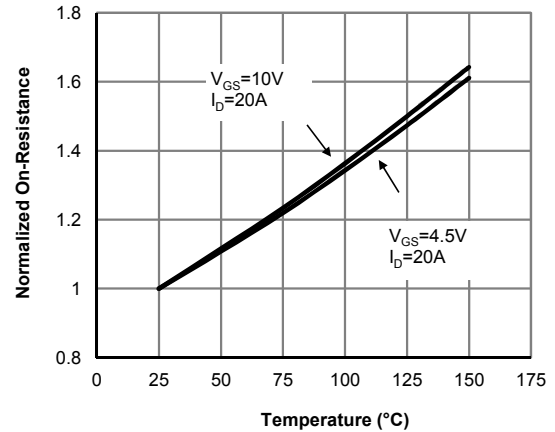
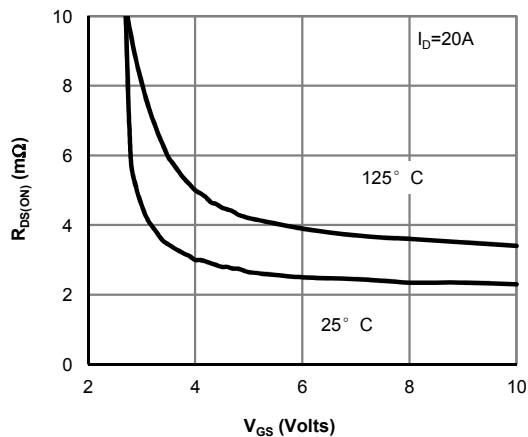
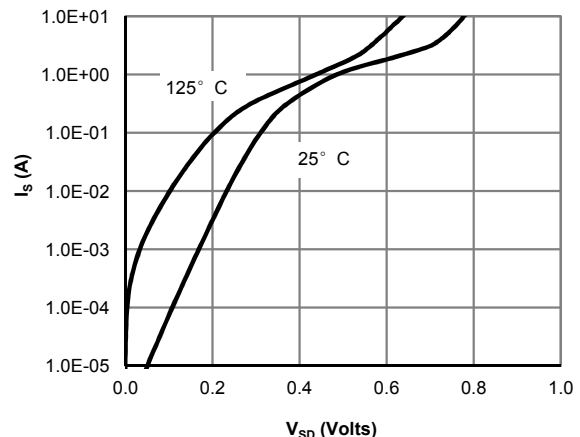
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

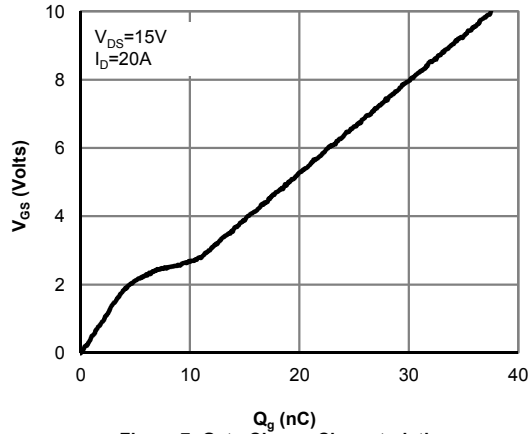
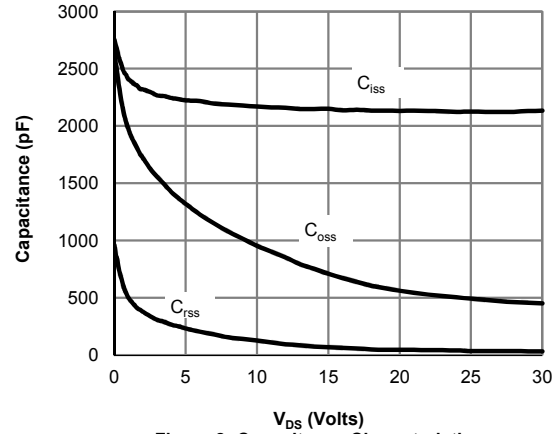
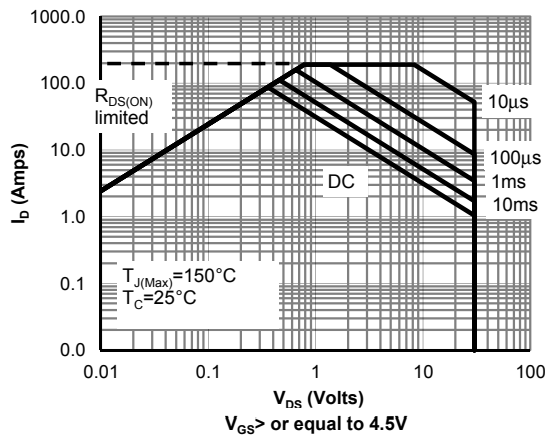
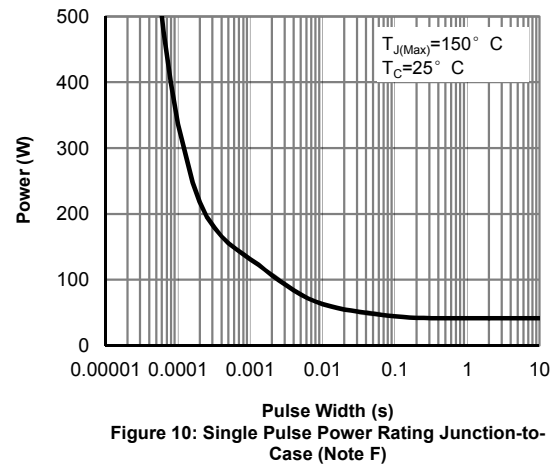
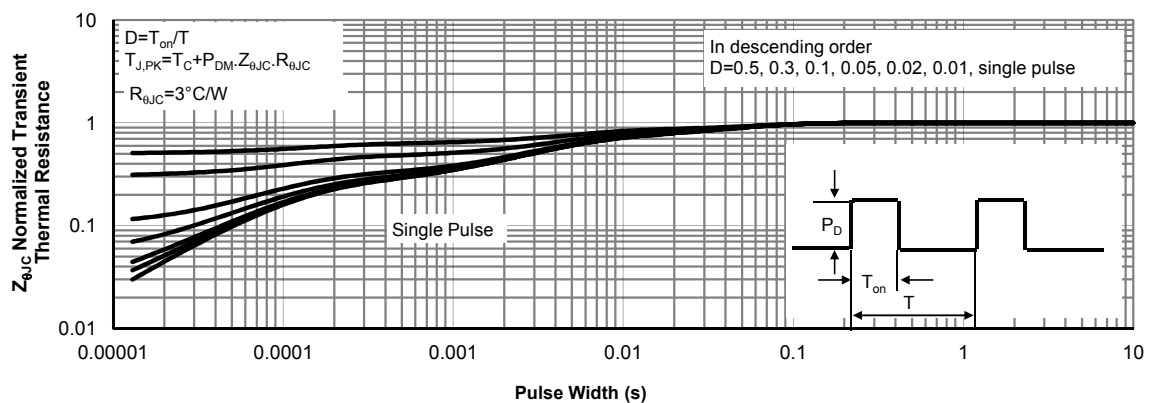
E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

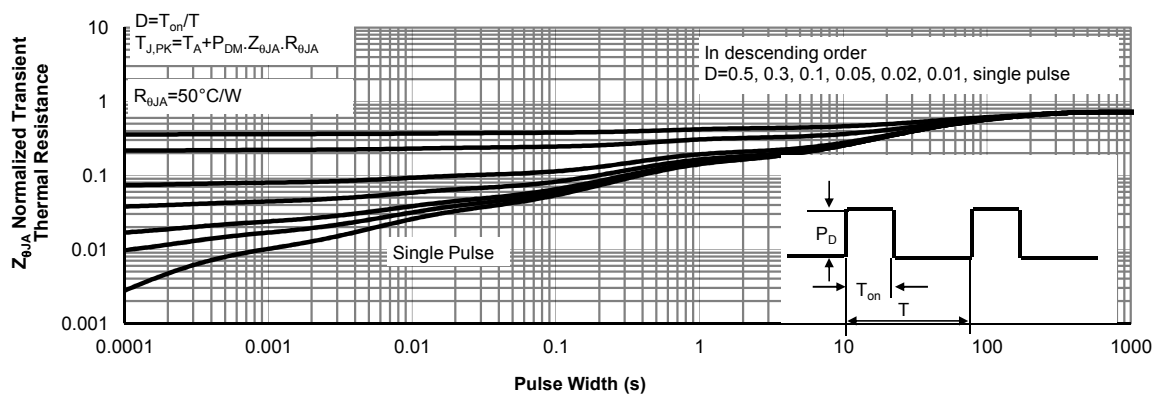
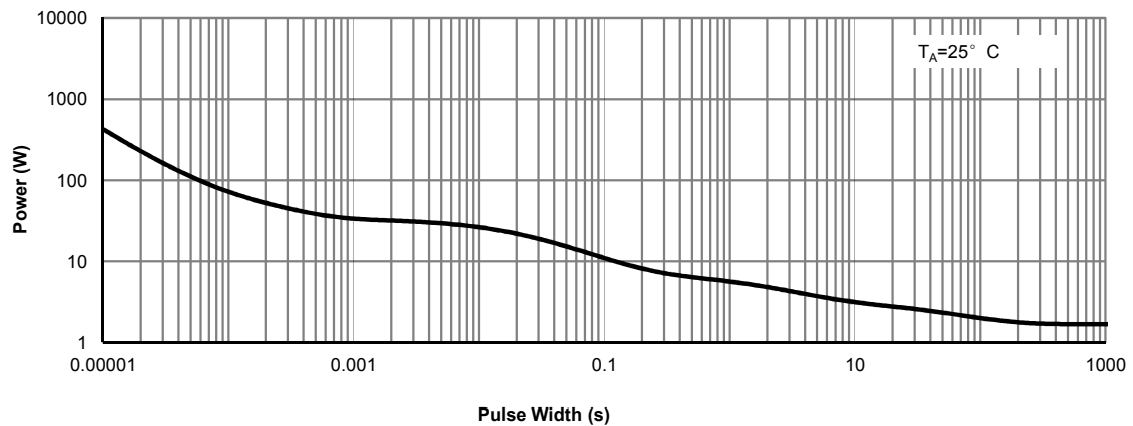
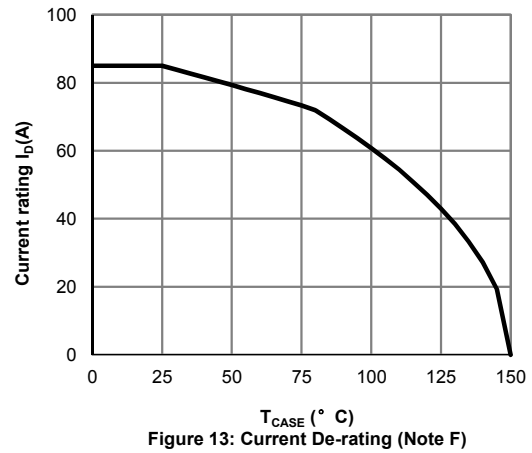
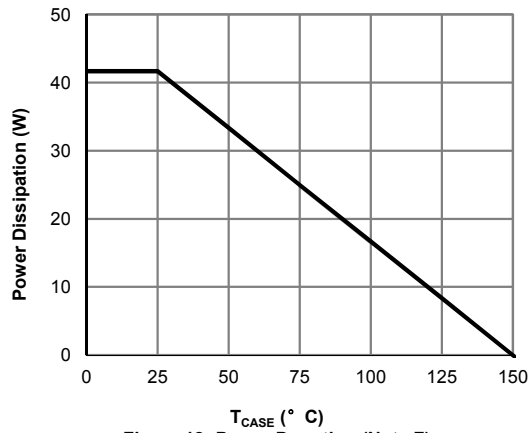
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

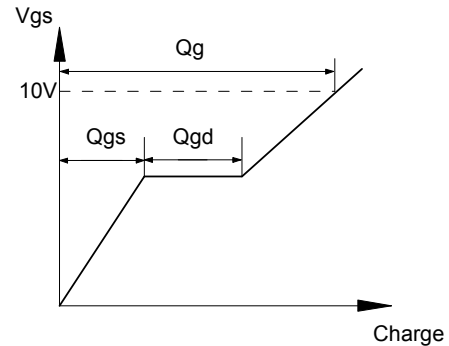
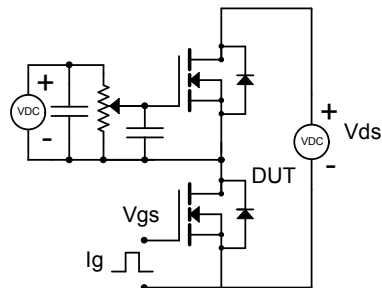
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



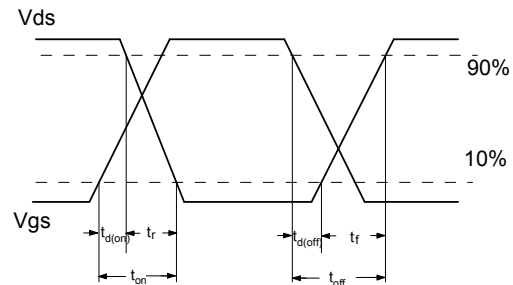
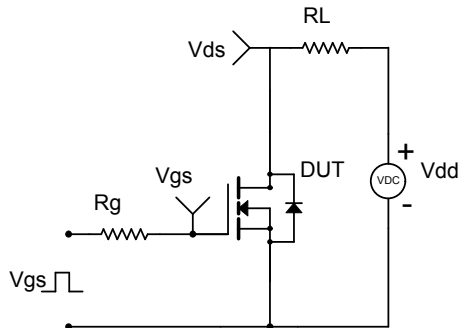
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



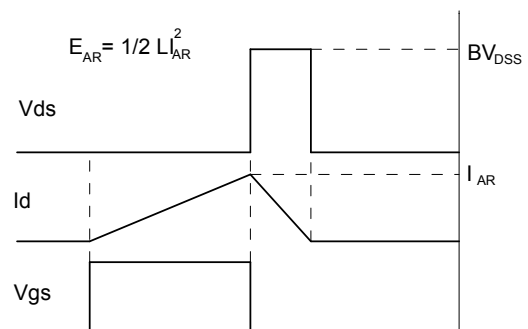
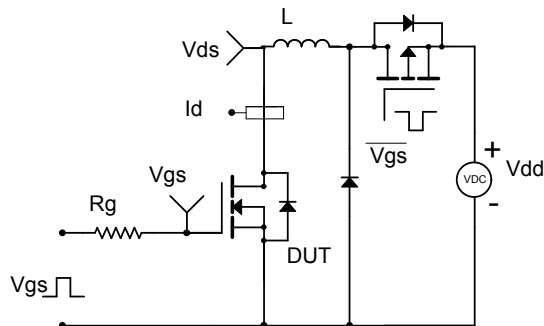
Gate Charge Test Circuit & Waveform



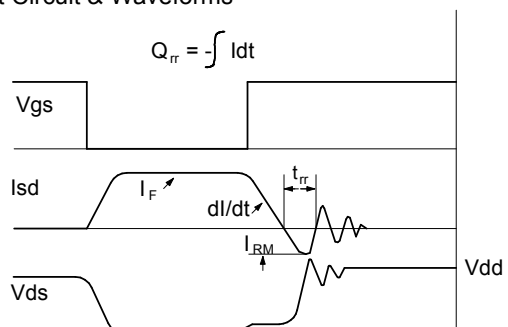
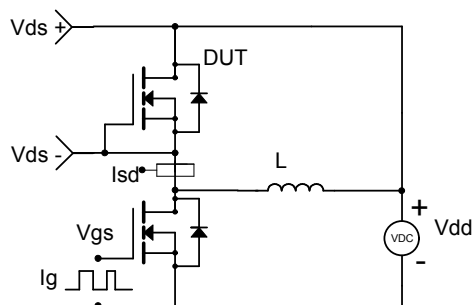
Resistive Switching Test Circuit & Waveforms



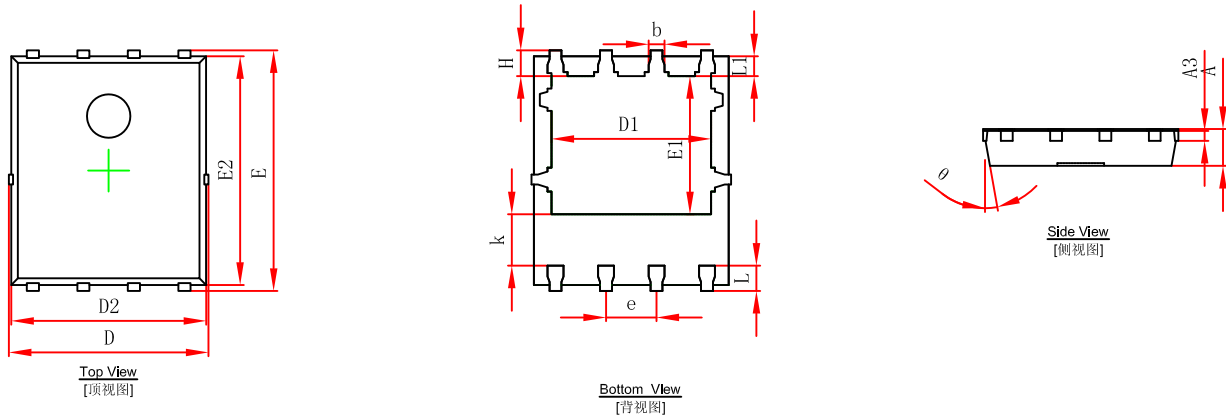
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

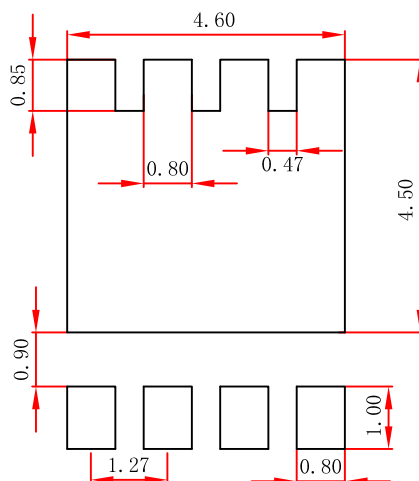


PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.