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ISL6292D

Li-ion/Li Polymer Battery Charger

FN9166
Rev.0.00
July 2004

The ISL6292D is an integrated single-cell Li-ion or Li-polymer battery charger capable of operating with an input voltage as low as 2.4V. This charger is designed to work with various types of ac adapters or a USB port.

The ISL6292D operates as a linear charger when the ac adapter is a voltage source. The battery is charged in a CC/CV (constant current/constant voltage) profile. The charge current is programmable up to 2A. The ISL6292D can also work with a current-limited adapter to minimize the thermal dissipation, in which case the ISL6292D combines the benefits of both a linear charger and a pulse charger.

The ISL6292D features charge current thermal foldback to guarantee safe operation when the printed circuit board is space limited for thermal dissipation. Additional features include preconditioning of an over-discharged battery, an NTC thermistor interface for charging the battery in a safe temperature range, automatic recharge, and thermally enhanced QFN package.

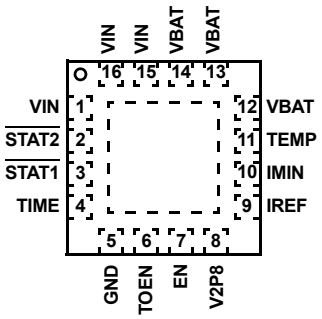
Ordering Information

PART #	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6292DCR4	-20 to 70	16 Ld 4x4 QFN	L16.4x4
ISL6292DCR4-T	16 Ld 4x4 QFN Tape and Reel		
ISL6292DCRZ (Note)	-20 to 70	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6292DCRZ-T (Note)	16 Ld 4x4 QFN Tape and Reel (Pb-free)		

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Pinout

ISL6292D (16 LEAD QFN)
TOP VIEW



Features

- Complete Charger for Single-Cell Li-ion Batteries
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- **Very Low Thermal Dissipation**
- **Two-Speed Blinking Indication at Fault Conditions**
- 1% Voltage Accuracy
- Programmable Current Limit up to 2A
- Programmable End-of-Charge Current
- **Charge Current Thermal Foldback**
- NTC Thermistor Interface for Battery Temperature Monitor
- **Accepts Multiple Types of Adapters or USB BUS Power**
- **Guaranteed to Operate at 2.65V After Start Up**
- Ambient Temperature Range: -20°C to 70°C
- Thermally-Enhanced QFN Packages
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-free Available

Applications

- Handheld Devices including Medical Handhelds
- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Self-Charging Battery Packs
- Stand-Alone Chargers
- USB Bus-Powered Chargers

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . -0.3 to 7V
Output Pin Voltage (VBAT) . . . . . -0.3 to 5.5V
Signal Input Voltage (TOEN, TIME, IREF, IMIN) . . . . . -0.3 to 3.2V
Output Pin Voltage (STAT1, STAT2) . . . . . -0.3 to 7V
Charge Current (For 4x4 QFN Package) 2.1A
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 1500V
Machine Model (Per EIAJ ED-4701 Method C-111) 150V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -20°C to 70°C
Supply Voltage, VIN . . . . . 4.3V to 6.5V

Thermal Information

Thermal Resistance (Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	41	4

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
For recommended soldering conditions, see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising VIN Threshold	V_{POR}		3.0	3.5	4.0	V
Falling VIN Threshold (Note 3)	V_{POR}		2.25	2.4	2.65	V
STANDBY CURRENT						
VBAT Pin Sink Current	$I_{STANDBY}$	VIN floating or EN = LOW	-	-	3.0	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN pulled low	-	30	-	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN floating	-	1	-	mA
VOLTAGE REGULATION						
Output Voltage	V_{CH}		4.158	4.20	4.242	V
Dropout Voltage		VBAT = 3.7V, 0.5A	-	140	-	mV
CHARGE CURRENT						
Constant Charge Current (Note 4)	I_{CHARGE}	R_{IREF} = 80kΩ, V_{BAT} = 3.7V	0.9	1.0	1.1	A
Trickle Charge Current	$I_{TRICKLE}$	R_{IREF} = 80kΩ, V_{BAT} = 2.0V	-	110	-	mA
Constant Charge Current	I_{CHARGE}	IREF Pin Voltage > 1.3V, V_{BAT} = 3.7V	400	450	500	mA
Trickle Charge Current	$I_{TRICKLE}$	IREF Pin Voltage > 1.3V, V_{BAT} = 2.0V	-	45	-	mA
Constant Charge Current	I_{CHARGE}	IREF Pin Voltage < 0.4V, V_{BAT} = 3.7V	-	-	100	mA
Trickle Charge Current	$I_{TRICKLE}$	IREF Pin Voltage < 0.4V, V_{BAT} = 2.0V	-	10	-	mA
End-of-Charge Threshold		R_{IMIN} = 80kΩ	85	110	135	mA
RECHARGE THRESHOLD						
Recharge Voltage Threshold Below V_{CH}	ΔV_{RECHRG}	The threshold in relative to V_{CH}	-	-200	-80	mV
Recharge Voltage Threshold	V_{RECHRG}		3.85	4.0	-	V
TRICKLE CHARGE THRESHOLD						
Trickle Charge Threshold Voltage	V_{MIN}		2.56	2.76	3.0	V

Electrical Specifications Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE MONITORING						
Low Battery Temperature Threshold	V_{TMIN}	V2P8 = 3.0V	1.40	1.50	1.60	V
Low Temperature Threshold Hysteresis		V2P8 = 3.0V	-	214	-	mV
High Battery Temperature Threshold	V_{TMAX}	V2P8 = 3.0V	.587	0.605	.623	V
High Temperature Threshold Hysteresis		V2P8 = 3.0V	-	55	-	mV
Battery Removal Threshold	V_{RMV}	V2P8 = 3.0V	-	2.25	-	V
Charge Current Foldback Threshold (Note 5)	T_{FOLD}		85	100	115	°C
Current Foldback Gain (Note 5)	G_{FOLD}		-	100	-	mA/°C
OSCILLATOR						
Oscillation Period	T_{OSC}	C_{TIME} = 15nF	2.4	3.0	3.6	ms
LOGIC INPUT AND OUTPUT						
TOEN Input High			2.0	-	-	V
TOEN and EN Input Low			-	-	0.8	V
IREF and IMIN Input High			1.2	-	-	V
IREF and IMIN Input Low			-	-	0.4	V
STAT1/STAT2 Sink Current		Pin Voltage = 0.8V	5	-	-	mA

NOTES:

3. The POR falling edge voltage is guaranteed to be lower than the Trickle Charge Threshold Voltage (V_{MIN}) by actual tests.
4. The actual charge current may be affected by the thermal foldback function if the thermal dissipation capability is not enough or by the on resistance of the power MOSFET if the charger input voltage is too close to the output voltage.
5. Guaranteed by design, not a tested parameter.

Pin Description

VIN (Pin 1, 15, 16)

VIN is the input power source. Connect to a wall adapter.

STAT2 (Pin 2)

STAT2 is an open-drain output to indicate the charger status. This pin is pulled to LOW during charging and to HIGH when not charging. When a fault situation occurs, the pin outputs a one-speed blinking indication.

STAT1 (Pin 3)

STAT1 is an open-drain output to indicate the charger status. The STAT1 pin is pulled LOW when the charger is charging a battery and to HIGH when the charge finishes. This pin outputs two different speeds of blinking signal depending on the type of the fault case.

TIME (Pin 4)

The TIME pin determines the oscillation period by connecting a timing capacitor between this pin and GND. The oscillator also provides a time reference for the charger.

GND (Pin 5)

GND is the connection to system ground.

TOEN (Pin 6)

TOEN is the TIMEOUT enable input pin. Pulling this pin to LOW disables the TIMEOUT charge-time limit for the fast charge modes. Leaving this pin HIGH or floating enables the TIMEOUT limit.

EN (Pin 7)

EN is the enable logic input. Connect the EN pin to LOW to disable the charger or leave it floating to enable the charger.

V2P8 (Pin 8)

This is a 2.8V reference voltage output. This pin outputs a 2.8V voltage source when the input voltage is above POR threshold and outputs zero otherwise. The V2P8 pin can be used as an indication for adapter presence. Use a 1µF ceramic capacitor to stabilize the internal linear regulator.

IREF (Pin 9)

This is the programming input for the constant charging current.

IMIN (Pin 10)

IMIN is the programmable input for the end-of-charge current.

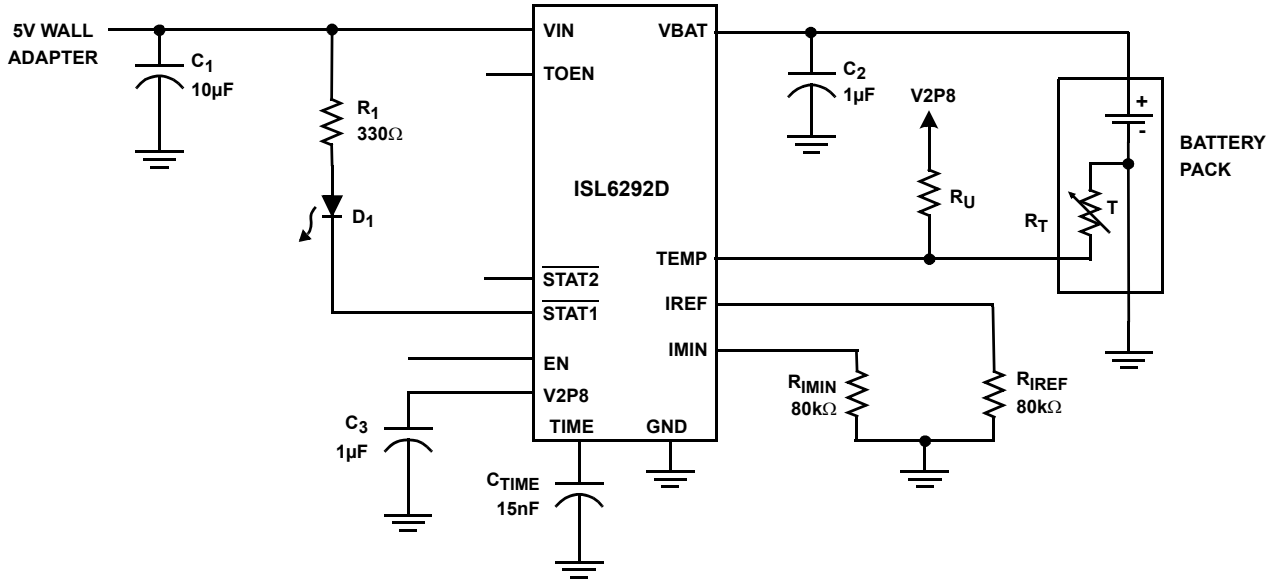
TEMP (Pin 11)

TEMP is the input for an external NTC thermistor. The TEMP pin is also used for battery removal detection.

VBAT (Pin 12, 13, 14)

VBAT is the connection to the battery. Typically a 10µF Tantalum capacitor is needed for stability when there is no battery attached. When a battery is attached, only a 0.1µF ceramic capacitor is required as the minimum decoupling capacitor.

Typical Application



Block Diagram

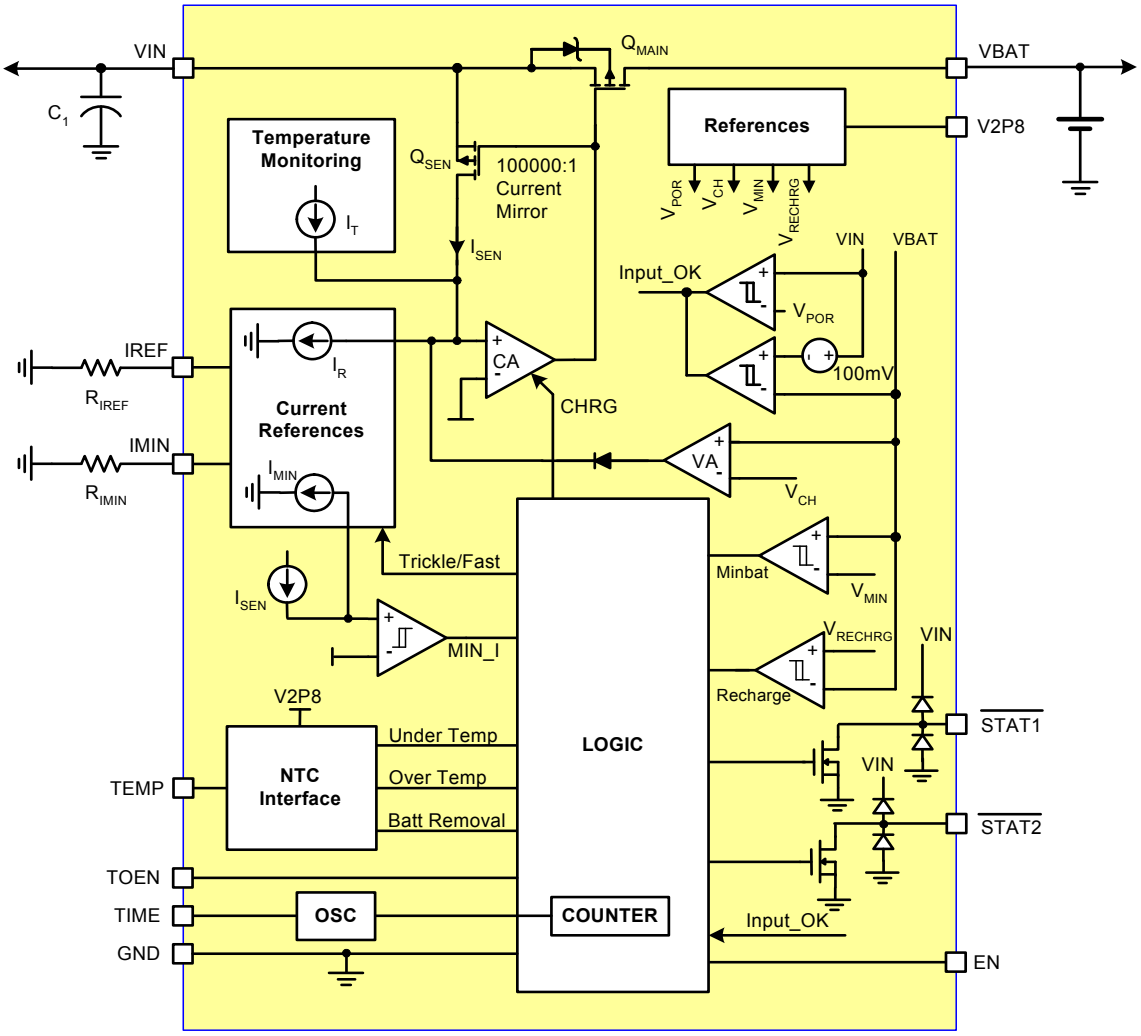
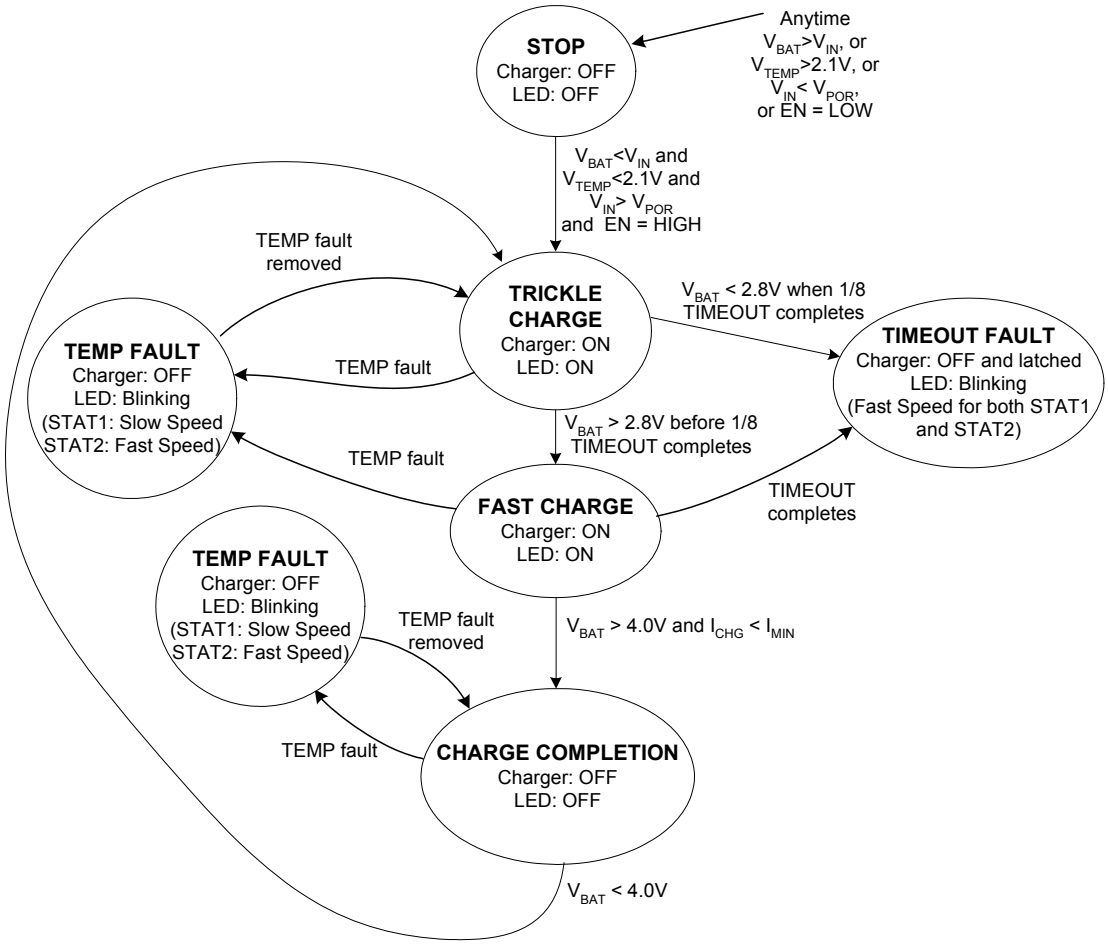


FIGURE 1. BLOCK PROGRAM

Flow Chart


STOP
Charger: OFF
LED: OFF
Anytime
V_{BAT}>V_{IN}, or
V_{TEMP}>2.1V, or
V_{IN}< V_{POR},
or EN = LOW
V_{BAT}<V_{IN} and
V_{TEMP}<2.1V and
V_{IN}> V_{POR}
and EN = HIGH
TRICKLE CHARGE
Charger: ON
LED: ON
TEMP fault removed
TEMP FAULT
Charger: OFF
LED: Blinking
(STAT1: Slow Speed
STAT2: Fast Speed)
TEMP fault
V_{BAT} < 2.8V when 1/8
TIMEOUT completes
TIMEOUT FAULT
Charger: OFF and latched
LED: Blinking
(Fast Speed for both STAT1
and STAT2)
V_{BAT} > 2.8V before 1/8
TIMEOUT completes
TEMP fault
FAST CHARGE
Charger: ON
LED: ON
TIMEOUT
completes
TEMP FAULT
Charger: OFF
LED: Blinking
(STAT1: Slow Speed
STAT2: Fast Speed)
TEMP fault
removed
V_{BAT} > 4.0V and I_{CHG} < I_{MIN}
TEMP fault
CHARGE COMPLETION
Charger: OFF
LED: OFF
V_{BAT} < 4.0V

Theory of Operation

The ISL6292D is an integrated charger for single-cell Li-ion or Li-polymer batteries. The ISL6292D functions as a traditional linear charger when powered with a voltage-source adapter. When powered with a current-limited adapter, the charger minimizes the thermal dissipation commonly seen in traditional linear chargers.

As a linear charger, the ISL6292D charges a battery in the popular constant current (CC) and constant voltage (CV) profile. The constant charge current I_{REF} is programmable up to 2A with an external resistor or a logic input. The charge voltage V_{CH} has 1% accuracy over the entire recommended operating condition range. The charger always preconditions the battery with 10% of the programmed current at the beginning of a charge cycle, until the battery voltage is verified to be above the minimum fast charge voltage, V_{MIN}. This low-current preconditioning charge mode is named trickle mode. The verification takes 15 cycles of an internal oscillator whose period is programmable with the timing capacitor. A thermal-foldback feature removes the thermal concern typically seen in linear chargers. The charger reduces the charge current automatically as the IC internal temperature rises above 100°C to prevent further temperature rise. The thermal-foldback feature guarantees safe operation when the printed circuit board (PCB) is space limited for thermal dissipation.

A TEMP pin monitors the battery temperature to ensure a safe charging temperature range. The temperature range is programmable with an external negative temperature coefficient (NTC) thermistor. The TEMP pin is also used to detect the removal of the battery.

The charger offers a safety timer for setting the fast charge time (TIMEOUT) limit to prevent charging a dead battery for an extensively long time. The TIMEOUT limit can be disabled as needed by the TOEN pin. The trickle mode is limited to 1/8 of TIMEOUT and **cannot** be disabled by the TOEN pin.

The charger automatically re-charges the battery when the battery voltage drops below a recharge threshold. When the wall adapter is not present, the ISL6292D draws less than 3µA current from the battery.

Three indication pins are available from the charger to indicate the charge status. The V2P8 outputs a 2.8V dc voltage when the input voltage is above the power-on reset (POR) level and can be used as the power-present indication. This pin is capable of sourcing a 2mA current, so it can also be used to bias external circuits. The STAT1 pin is an open-drain logic output that turns LOW when the battery is being charged and turns HIGH when the EOC condition is qualified. The EOC condition is: the battery voltage rises above the recharge threshold and the charge current falls below a user-programmable EOC current threshold. Once the EOC condition is qualified, the STAT1 output rises to HIGH and is latched. The latch is released at the beginning of a charge or re-charge cycle. The STAT1 pin blinks when a fault occurs. The blinking frequency of a TIMEOUT fault is twice as fast as a temperature fault. The STAT2 pin behaves the same as the STAT1 except that it blinks at one frequency only when any fault occurs.

Figure 2 shows the typical charge curves in a traditional linear charger powered with a constant-voltage adapter. From the top to bottom, the curves represent the constant input voltage, the battery voltage, the charge current and the power dissipation in the charger. The power dissipation P_{CH} is given by the following equations:

$$P_{CH} = (V_{IN}-V_{BAT}) \cdot I_{CHARGE} \quad \text{(EQ. 1)}$$

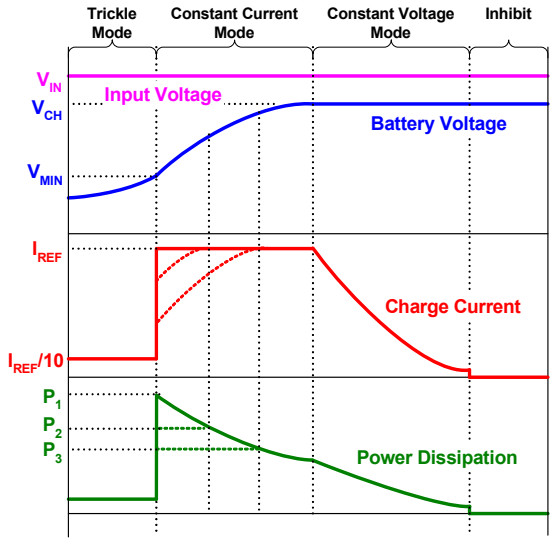


FIGURE 2. TYPICAL CHARGE CURVES USING A CONSTANT-VOLTAGE ADAPTER

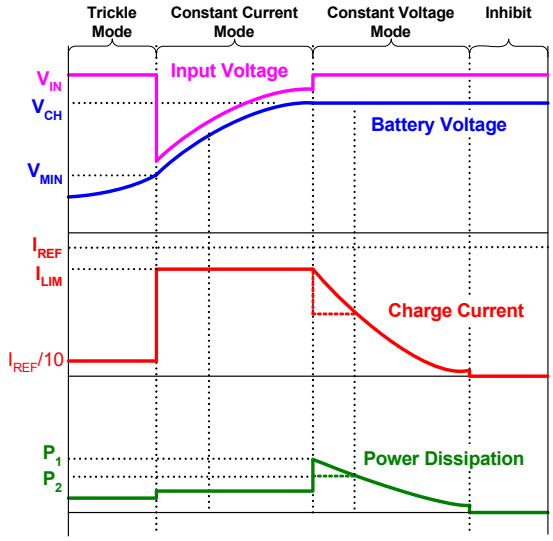


FIGURE 3. TYPICAL CHARGE CURVES USING A CURRENT-LIMITED ADAPTER

where I_{CHARGE} is the charge current. The maximum power dissipation occurs during the beginning of the CC mode. The maximum power the IC is capable of dissipating is dependent on the thermal impedance of the printed-circuit board (PCB). Figure 2 shows, with dotted lines, two cases that the charge currents are limited by the maximum power dissipation capability due to the thermal foldback.

When using a current-limited adapter, the thermal situation in the ISL6292D is totally different. Figure 3 shows the typical charge curves when a current-limited adapter is employed. The operation requires the I_{REF} to be programmed higher than the limited current I_{LIM} of the adapter, as shown in Figure 3. The key difference of the charger operating under such conditions occurs during the CC mode.

The Block Diagram, Figure 1, aids in understanding the operation. The current loop consists of the current amplifier CA and the sense MOSFET Q_{SEN}. The current reference I_R is programmed by the IREF pin. The current amplifier CA regulates the gate of the sense MOSFET Q_{SEN} so that the sensed current I_{SEN} matches the reference current I_R. The main MOSFET Q_{MAIN} and the sense MOSFET Q_{SEN} form a current mirror with a ratio of 100,000:1, that is, the output charge current is 100,000 times I_R. In the CC mode, the current loop tries to increase the charge current by enhancing the sense MOSFET Q_{SEN}, so that the sensed current matches the reference current. On the other hand, the adapter current is limited, the actual output current will never meet what is required by the current reference. As a result, the current error amplifier CA keeps enhancing the Q_{SEN} as well as the main MOSFET Q_{MAIN}, until they are fully turned on. Therefore, the main MOSFET becomes a power switch instead of a linear regulation device. The power dissipation in the CC mode becomes:

$$P_{CH} = R_{DS(ON)} \cdot I_{CHARGE}^2 \quad \text{(EQ. 2)}$$

where $r_{DS(ON)}$ is the resistance when the main MOSFET is fully turned on. This power is typically much less than the peak power in the traditional linear mode.

The worst power dissipation when using a current-limited adapter typically occurs at the beginning of the CV mode, as shown in Figure 3. The equation EQ.1 applies during the CV mode. When using a very small PCB whose thermal impedance is relatively large, it is possible that the internal temperature can still reach the thermal foldback threshold. In that case, the IC is thermally protected by lowering the charge current, as shown with the dotted lines in the charge current and power curves. Appropriate design of the adapter can further reduce the peak power dissipation of the ISL6292D. See the Application Information section for more information.

Figure 4 illustrates the typical signal waveforms for the linear charger from the power-up to a recharge cycle. More detailed Applications Information is given below.

Applications Information

Power on Reset (POR)

The ISL6292D resets itself as the input voltage rises above the POR rising threshold. The V2P8 pin outputs a 2.8V voltage, the internal oscillator starts to oscillate, the internal timer is reset, and the charger begins to charge the battery. The two indication pins, STAT1 and STAT2, indicate LOW. Figure 4 illustrates the start up of the charger between t_0 to t_2.

The ISL6292D has a typical rising POR threshold of 3.4V and a falling POR threshold of 2.4V. The 2.4V falling threshold guarantees charger operation with a current-limited adapter to minimize the thermal dissipation.

Charge Cycle

A charge cycle consists of three charge modes: trickle mode, constant current (CC) mode, and constant voltage (CV) mode. The charge cycle always starts with the trickle mode until the battery voltage stays above V_{MIN} (2.8V typical) for 15 consecutive cycles of the internal oscillator. If the battery voltage drops below V_{MIN} during the 15 cycles, the 15-cycle counter is reset and the charger stays in the trickle mode. The charger moves to the CC mode after verifying the battery voltage. As the battery-pack terminal voltage rises to the final charge voltage V_{CH}, the CV mode begins. The terminal voltage is regulated at the constant V_{CH} in the CV mode and the charge current is expected to decline. After the charge current drops below I_{MIN}, the ISL6292D indicates the end-of-charge (EOC) with the STAT1 or STAT2 pin and terminates. Signals in a charge cycle are illustrated in Figure 4 between points t_2 to t_5.

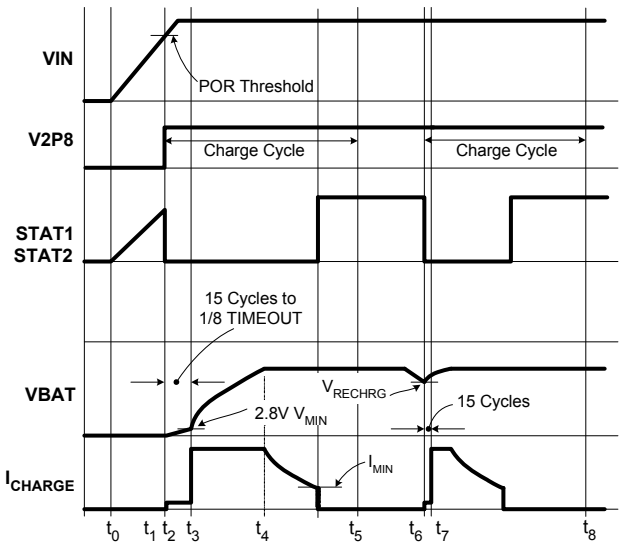


FIGURE 4. OPERATION WAVEFORMS

The following events initiate a new charge cycle:

- POR,
- a new battery being inserted (detected by TEMP pin),
- the battery voltage drops below a recharge threshold after completing a charge cycle,
- recovery from an battery over-temperature fault,
- or, the EN pin is toggled from GND to floating.

Further description of these events are given later in this data sheet.

Recharge

After a charge cycle completes, charging is prohibited until the battery voltage drops to a recharge threshold, V_{RECHRG} (see Electrical Specifications). Then a new charge cycle starts at point t_6 and ends at point t_8, as shown in Figure 4. The safety timer is reset at t_6.

Internal Oscillator

The internal oscillator establishes a timing reference. The oscillation period is programmable with an external timing capacitor, C_{TIME}, as shown in Typical Applications. The oscillator charges the timing capacitor to 1.5V and then discharges it to 0.5V in one period, both with 10µA current. The period T_{OSC} is:

$$T_{OSC} = 0.2 \cdot 10^6 \cdot C_{TIME} \quad (\text{seconds}) \qquad \text{(EQ. 3)}$$

A 1nF capacitor results in a 0.2ms oscillation period. The accuracy of the period is mainly dependent on the accuracy of the capacitance and the internal current source.

Total Charge Time

The total charge time for the CC mode and CV mode is limited to a length of TIMEOUT. A 22-stage binary counter increments each oscillation period of the internal oscillator to set the TIMEOUT. The TIMEOUT can be calculated as:

$$TIMEOUT = 2^{22} \cdot T_{OSC} = 14 \cdot \frac{C_{TIME}}{1nF} \quad (\text{minutes}) \qquad \text{(EQ. 4)}$$

A 1nF capacitor leads to 14 minutes of TIMEOUT. For example, a 15nF capacitor sets the TIMEOUT to be 3.5 hours. The charger has to reach the end-of-charge condition before the TIMEOUT, otherwise, a TIMEOUT fault is issued. The TIMEOUT fault latches up the charger. There are two ways to release such a latch-up: either to recycle the input power, or toggle the EN pin to disable the charger and then enable it again.

The trickle mode charge has a time limit of 1/8 TIMEOUT. If the battery voltage does not reach V_{MIN} within this limit, a TIMEOUT fault is issued and the charger latches up. The charger stays in trickle mode for at least 15 cycles of the internal oscillator and, at most, 1/8 of TIMEOUT, as shown in Figure 4.

Disabling TIMEOUT Limit

The TIMEOUT limit for the fast charge modes can be disabled by pulling the TOEN pin to LOW or shorting it to GND. When this happens, the charger becomes a current-limited LDO (low-dropout) supply with its voltage regulated at the final charge voltage V_{CH} and the current limit determined by the IREF pin. If the LDO load current drops below the end-of-charge current (refer to End-of-Charge section), the STAT1 and the STAT2 pin will indicate.

The trickle charge time limit, however, is not disabled even when the TOEN pin is pulled to LOW. The charger operates in the trickle mode at the beginning of a charge cycle even if the TIMEOUT is disabled. Leaving the TOEN pin floating is recommended to enable the TIMEOUT. Driving the TOEN pin above 3.0V is not recommended.

Charge Current Programming

The charge current is programmed by the IREF pin. There are three ways to program the charge current:

1. driving the IREF pin above 1.3V
2. driving the IREF pin below 0.4V,
3. or using the R_{IREF} as shown in the Typical Applications.

The voltage of IREF is regulated to a 0.8V reference voltage when not driven by any external source. The charging current during the constant current mode is 100,000 times that of the current in the R_{IREF} resistor. Hence, depending on how IREF pin is used, the charge current is,

$$I_{REF} = \begin{cases} 500mA & V_{IREF} > 1.3V \\ \frac{0.8V}{R_{IREF}} \times 10^5 (A) & R_{IREF} \\ 100mA & V_{IREF} < 0.4V \end{cases} \qquad \text{(EQ. 5)}$$

The 500mA current is a guaranteed maximum value for high-power USB port, with the typical value of 450mA. The 100mA current is also a guaranteed maximum value for the low-power USB port. This design accommodates the USB power specification.

The internal reference voltage at the IREF pin is capable of sourcing less than 100µA current. When pulling down the IREF pin with a logic circuit, the logic circuit needs to be able to sink at least 100µA current.

When the adapter is current limited, it is recommended that the reference current be programmed to at least 30% higher than the adapter current limit (which equals the charge current). In addition, the charge current should be at least 350mA so that the voltage difference between the VIN and the VBAT pins is higher than 100mV. The 100mV is the offset voltage of the input-output voltage comparator shown in the block diagram.

End-of-Charge (EOC) Current

The end-of-charge current I_{MIN} sets the level at which the charger indicates the end of the charge with the STAT1 and STAT2 pins, as shown in Figure 4. The charger terminates at this moment. The I_{MIN} is set in two ways, by connecting a resistor between the IMIN pin and ground, or by connecting the IMIN pin to the V2P8 pin. When programming with the resistor, the I_{MIN} is set in the equation below.

$$I_{MIN} = 10000 \cdot \frac{V_{REF}}{R_{IMIN}} = \frac{0.8V}{R_{IMIN}} \times 10^4 (A) \quad \text{(EQ. 6)}$$

where R_{IMIN} is the resistor connected between the IMIN pin and the ground. When connected to the V2P8 pin, the I_{MIN} is set to 1/10 of I_{REF}, except when the IREF pin is shorted to GND. Under this exception, I_{MIN} is 5mA.

Charge Current Thermal Foldback

Over-heating is always a concern in a linear charger. The maximum power dissipation usually occurs at the beginning of a charge cycle when the battery voltage is at its minimum but the charge current is at its maximum. The charge current thermal foldback function in the ISL6292D frees users from the over-heating concern.

Figure 5 shows the current signals at the summing node of the current error amplifier CA in the Block Diagram. I_R is the reference. I_T is the current from the Temperature Monitoring block. The I_T has no impact on the charge current until the internal temperature reaches approximately 100°C; then I_T rises at a rate of 1µA/°C. When I_T rises, the current control loop forces the sensed current I_{SEN} to reduce at the same rate. As a mirrored current, the charge current is 100,000 times that of the sensed current and reduces at a rate of 100mA/°C. For a charger with the constant charge current set at 1A, the charge current is reduced to zero when the internal temperature rises to 110°C. The actual charge current settles between 100°C to 110°C.

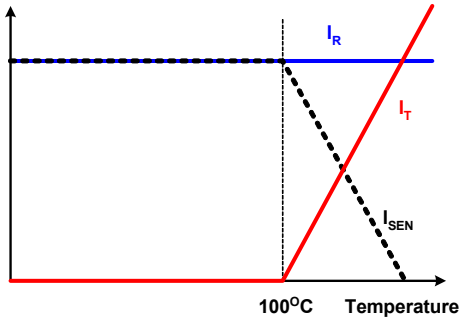


FIGURE 5. CURRENT SIGNALS AT THE AMPLIFIER CA INPUT

Usually the charge current should not drop below I_{MIN} because of the thermal foldback. For some extreme cases if that does happen, the charger does not indicate end-of-charge unless the battery voltage is already above the recharge threshold.

2.8V Bias Voltage

The ISL6292D provides a 2.8V voltage for biasing the internal control and logic circuit. This voltage is also available for external circuits such as the NTC thermistor circuit. The maximum allowed external load is 2mA.

NTC Thermistor

The ISL6292D uses two comparators (CP2 and CP3) to form a window comparator, as shown in Figure 7. When the TEMP pin voltage is "out of the window," determined by the V_{TMIN} and V_{TMAX}, the ISL6292D stops charging and indicates a fault condition. When the temperature returns to the set range, the charger re-starts a charge cycle. The two MOSFETs, Q1 and Q2, produce hysteresis for both upper and lower thresholds. The temperature window is shown in Figure 6.

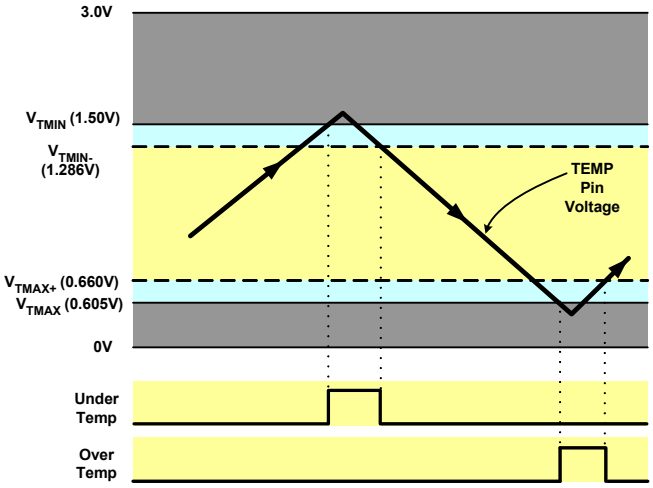


FIGURE 6. CRITICAL VOLTAGE LEVELS FOR TEMP PIN

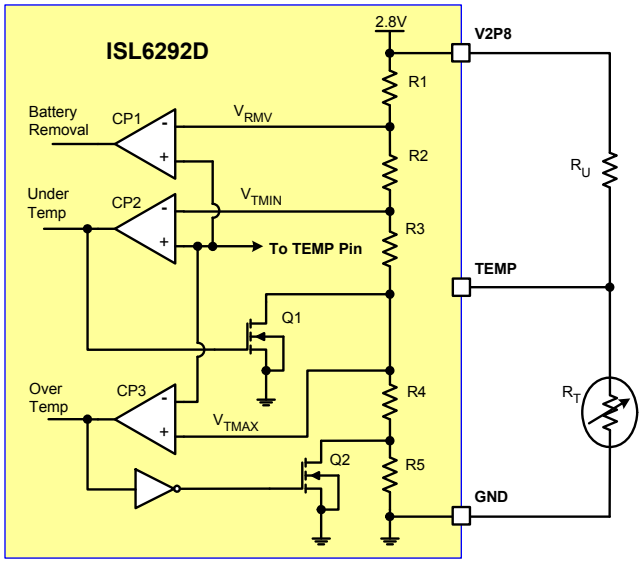


FIGURE 7. THE INTERNAL AND EXTERNAL CIRCUIT FOR THE NTC INTERFACE

As the TEMP pin voltage rises from low and exceeds the 1.5V threshold (when the V2P8 pin is forced with a 3V bias), the under temperature signal rises and does not clear until the TEMP pin voltage falls below the 1.286V falling threshold. Similarly, the over-temperature signal is given when the TEMP pin voltage falls below the 0.605V threshold and does not clear until the voltage rises above 0.66V. The actual accuracy of the 3V bias is **not important** because all the thresholds and the TEMP pin voltage are ratios determined by the resistor dividers, as shown in Figure 7.

The NTC thermistor is required to have a resistance ratio of 3.96:1 at the low and the high temperature limits, that is,

$$\frac{R_{COLD}}{R_{HOT}} = 3.96 \quad \text{(EQ. 7)}$$

This is because at the low temperature limit, the TEMP pin voltage is 1.5V, which is 1/2 of the 3V bias. Thus,

$$R_{COLD} = R_U \quad \text{(EQ. 8)}$$

where R_U is the pull-up resistor as shown in Figure 7. On the other hand, at the high temperature limit the TEMP pin voltage is 0.605V, 20.17% of the 3V bias. Therefore,

$$\frac{R_{HOT}}{R_U} = \frac{0.2017}{1 - 0.2017} \quad \text{(EQ. 9)}$$

For applications that do not need to monitor the battery temperature, the NTC thermistor can be replaced with a regular resistor of a half value of the pull up resistor R_U. Another option is to connect the TEMP pin to the IREF pin that has a 0.8V output. With such connection, the IREF pin can no longer be programmed with logic inputs.

Battery Removal Detection

The ISL6292D assumes that the thermistor is co-packed with the battery and is removed together with the battery. When the charger senses a TEMP pin voltage that is 2.1V or higher, it assumes that the battery is removed. The battery removal detection circuit is also shown in Figure 7. When a battery is removed, the charger is stopped. When a battery is inserted again, a new charge cycle starts.

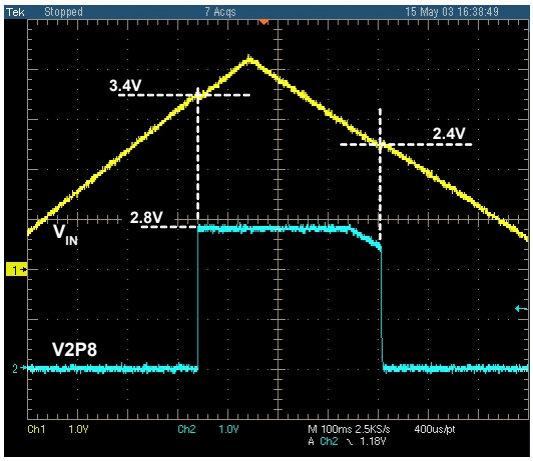


FIGURE 8. THE V2P8 PIN OUTPUT vs THE INPUT VOLTAGE AT THE VIN PIN. VERTICAL: 1V/DIV, HORIZONTAL: 100ms/DIV

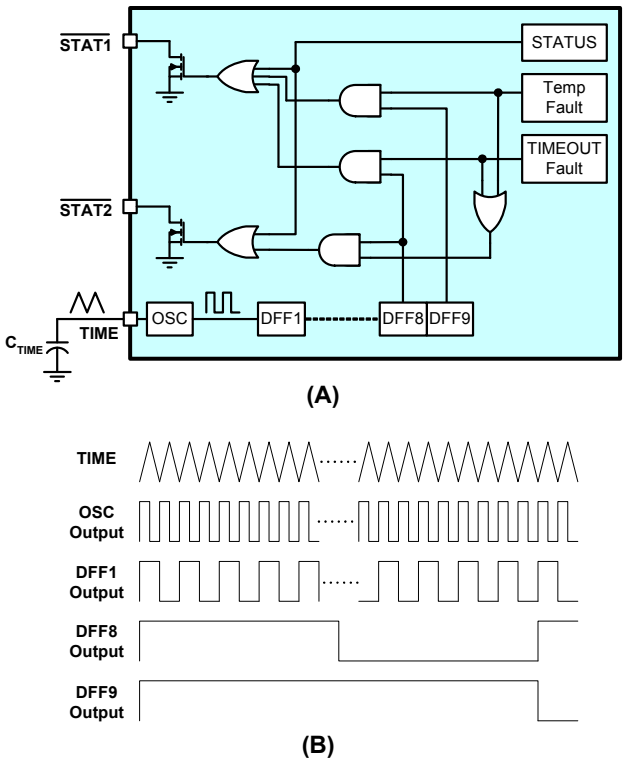


FIGURE 9. EQUIVALENT CIRCUIT FOR THE STAT1/STAT2 INDICATION PINS AND KEY OPERATING WAVEFORMS

Indications

The ISL6292D has three indication pins: V2P8, STAT1, and STAT2. The input presence is indicated by the V2P8 pin. Figure 8 shows the V2P8 pin voltage vs. the input voltage. The equivalent circuit for the STAT1 and STAT2 pins are shown in Figure 9. Both pins have ESD diodes to clamp the pin voltage between ground and the input, as shown in the Block Diagram. The STATUS block outputs a logic HIGH when the charger is charging and a LOW whenever the charger is not charging. When a fault case happens, the charger stops charging, therefore, the STATUS block outputs LOW. Depending on fault cause, either the eighth or the ninth D-type flip-flop output is gated to the STAT1 pin. Both flip-flop outputs are 50% duty ratio blinking signals. The periods of the eighth and ninth flip-flop output are calculated by the following equations:

$$T_{8th} = 2^8 \cdot T_{OSC} = 256 \cdot T_{OSC} \quad \text{(EQ. 10)}$$

$$T_{9th} = 2^9 \cdot T_{OSC} = 512 \cdot T_{OSC} \quad \text{(EQ. 11)}$$

Table 1 and 2 summarize the LED indication driven by STAT1 and STAT2 respectively.

TABLE 1. SUMMARY OF CHARGE STATUS AND LED OUTPUT

STATUS	LED OUTPUT
Charging	On
Charge Completed or Disabled	OFF
Temperature Fault	Blinks at the speed of T_{9th}
TIMEOUT Fault	Blinks at the speed of T_{8th}

TABLE 2. SUMMARY OF CHARGE STATUS AND LED OUTPUT

STATUS	LED OUTPUT
Charging	On
Charge Completed or Disabled	OFF
Fault	Blinks at the speed of T_{8th}

Shutdown

The ISL6292D can be shutdown by pulling the EN pin to ground. When shut down, the charger draws typically less than 30µA current from the input power and the 2.8V output at the V2P8 pin is also turned off. The EN pin needs be driven with an open-drain or open-collector logic output, so that the EN pin is floating when the charger is enabled.

Input and Output Capacitor Selection

Typically any type of capacitors can be used for the input and the output. A 0.47µF or higher value ceramic capacitor for the input is recommended to be placed very close to the input pin and the ground pin. Another 10µF capacitance is required to stabilize the input voltage. When the battery is attached to the charger, the output capacitor can be any ceramic type with the value higher than 0.1µF. However, if there is a chance the charger will be used as an LDO linear regulator, a 10µF tantalum capacitor is recommended.

Working with Current-Limited Adapter

The ISL6292D can work with a current-limited adapter to significantly reduce the thermal dissipation during charging. Refer to the ISL6292 datasheet, which can be found at http://www.intersil.com, for more details.

Board Layout Recommendations

The ISL6292D internal thermal foldback function limits the charge current when the internal temperature reaches approximately 100°C. In order to maximize the current capability, it is very important that the exposed pad under the package is properly soldered to the board and is connected to other layers through thermal vias. More thermal vias and more copper attached to the exposed pad will result in better thermal performance. On the other hand, the number of vias is limited by the size of the pad. The exposed pads for the 4x4 QFN package is able to have 5 vias. Refer to the ISL6292 evaluation boards for layout examples.

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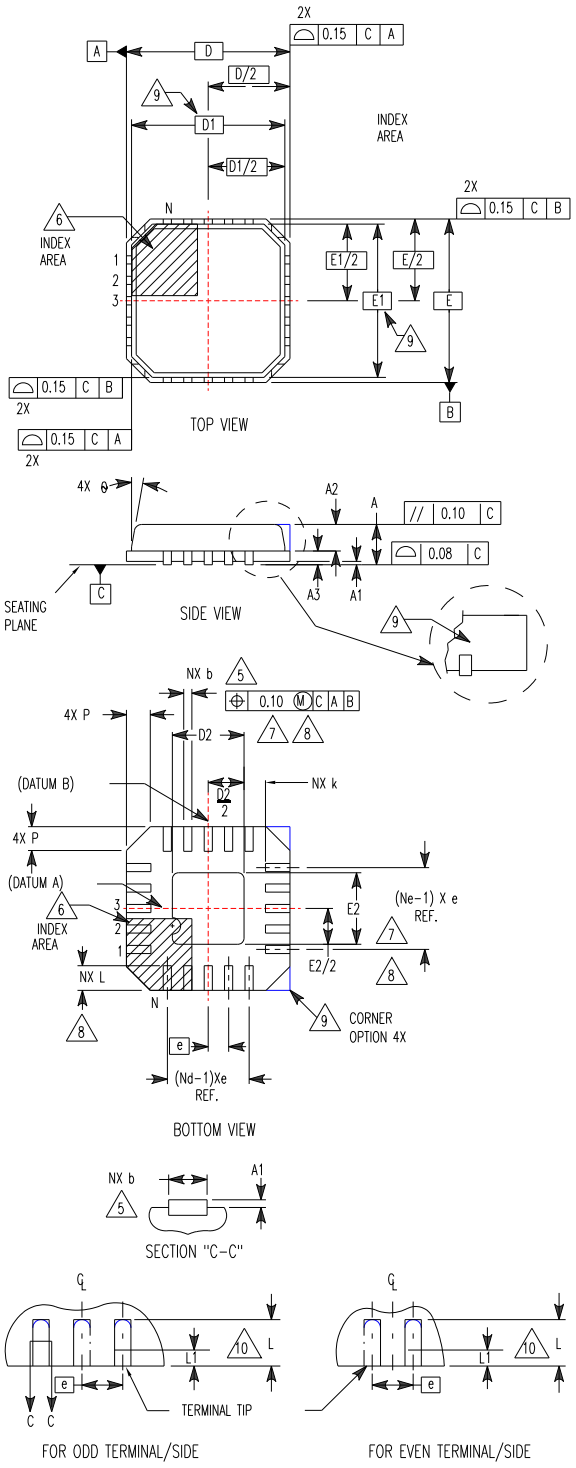
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.