

# CS5101

## Secondary Side Post Regulator for AC/DC and DC/DC Multiple Output Converters

The CS5101 is a bipolar monolithic secondary side post regulator (SSPR) which provides tight regulation of multiple output voltages in AC/DC or DC/DC converters. Leading edge pulse width modulation is used with the CS5101.

The CS5101 is designed to operate over an 8.0 V to 45 V supply voltage ( $V_{CC}$ ) range and up to a 75 V drive voltage ( $V_C$ ).

The CS5101 features include a totem pole output with 1.5 A peak output current capability, externally programmable overcurrent protection, an on chip 2.0% precision 5.0 V reference, internally compensated error amplifier, externally synchronized switching frequency, and a power switch drain voltage monitor. It is available in a 14 lead plastic DIP or a 16 lead wide body SOIC package.

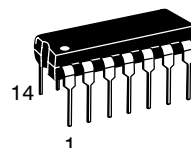
### Features

- 1.5 A Peak Output (Grounded Totem Pole)
- 8.0 V to 75 V Gate Drive Voltage
- 8.0 V to 45 V Supply Voltage
- 300 ns Propagation Delay
- 1.0% Error Amplifier Reference Voltage
- Lossless Turn On and Turn Off
- Sleep Mode: < 100  $\mu$ A
- Overcurrent Protection with Dedicated Differential Amp
- Synchronization to External Clock
- External Power Switch Drain Voltage Monitor
- Pb-Free Packages are Available\*

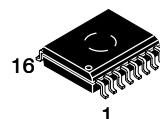


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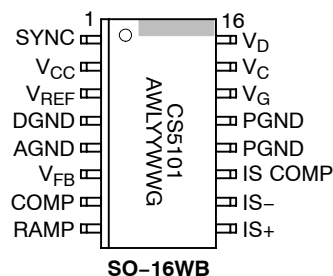
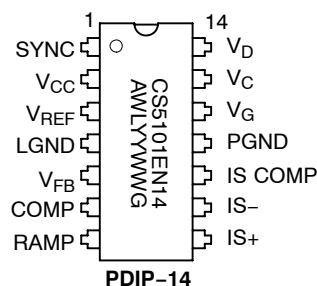


PDIP-14  
N SUFFIX  
CASE 646



SO-16WB  
DW SUFFIX  
CASE 751G

### MARKING DIAGRAMS AND PIN ASSIGNMENTS



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# CS5101

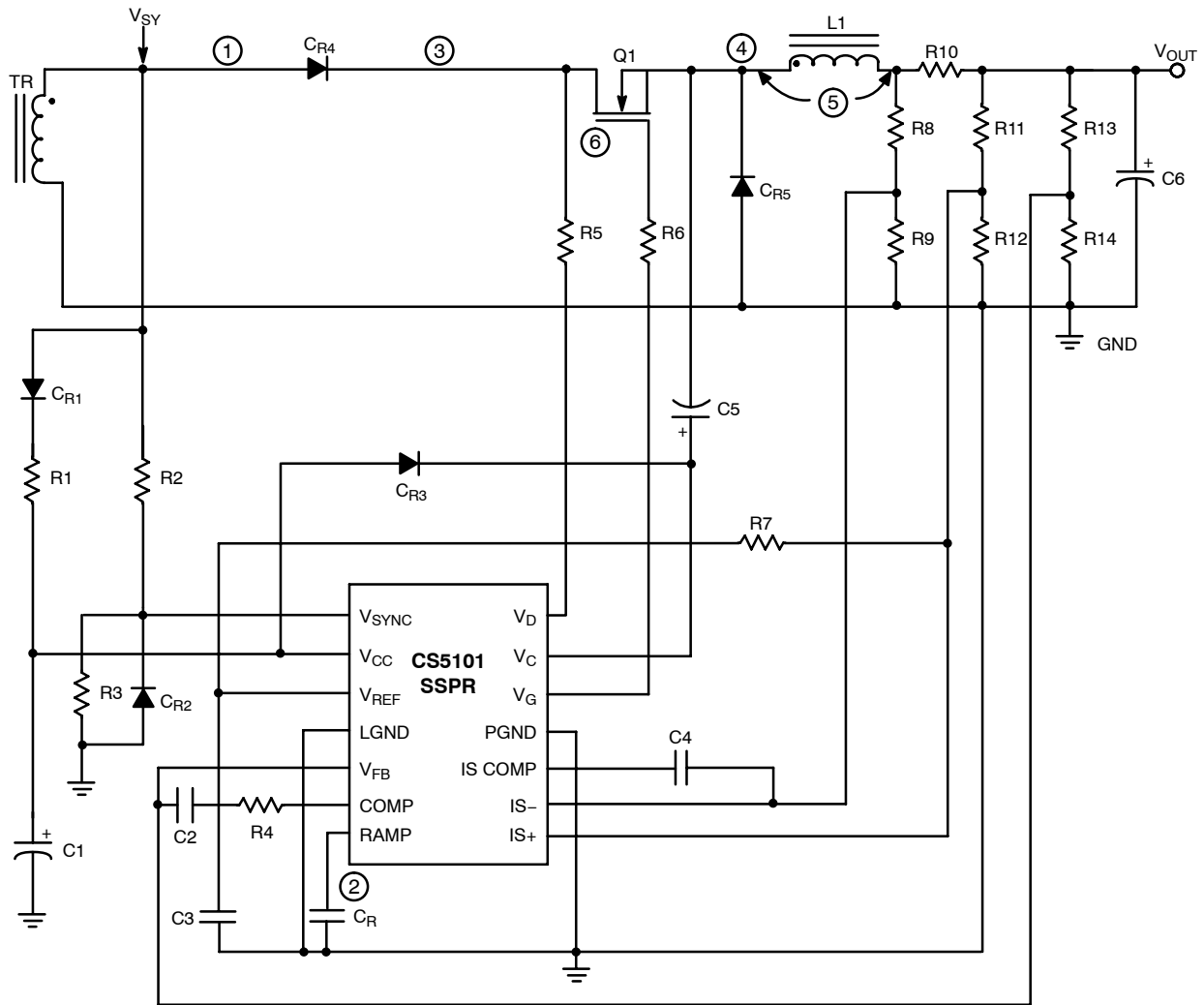


Figure 1. Application Diagram

## MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage, $V_{CC}$	-0.3 to 45	V
$V_{SYNC}$ and Output Supply Voltages, $V_C$ , $V_G$ , $V_{SYNC}$ , $V_D$	-0.3 to 75	V
$V_{IS+}$ , $V_{IS-}$ ( $V_{CC} - 4.0$ V, up to 24 V)	-0.3 to 24	V
$V_{REF}$ , $V_{FB}$ , $V_{COMP}$ , $V_{RAMP}$ , $V_{ISCOMP}$	-0.3 to 10	V
Operating Junction Temperature, $T_J$	-40 to +150	°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Output Energy (Capacitive Load Per Cycle)	5.0	μJ
ESD Human Body	2.0	kV
Lead Temperature Soldering	Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak
		°C °C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 10 second maximum

2. 60 second maximum above 183°C

# CS5101

**ELECTRICAL CHARACTERISTICS** ( $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $10\text{ V} < V_{CC} < 45\text{ V}$ ,  $8.0\text{ V} < V_C < 75\text{ V}$ ; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>Error Amplifier</b>					
Input Voltage Initial Accuracy	$V_{FB} = V_{COMP}$ , $V_{CC} = 15\text{ V}$ , $T = 25^{\circ}\text{C}$ , Note 3	1.98	2.00	2.02	V
Input Voltage	$V_{FB} = V_{COMP}$ , includes line and temp	1.94	2.00	2.06	V
Input Bias Current	$V_{FB} = 0\text{ V}$ , $I_{V_{FB}}$ flows out of pin	–	–	500	nA
Open Loop Gain	$1.5\text{ V} < V_{COMP} < 3.0\text{ V}$	60	70	–	dB
Unity Gain Bandwidth	$1.5\text{ V} < V_{COMP} < 3.0\text{ V}$ , Note 3	0.7	1.0	–	MHz
Output Sink Current	$V_{COMP} = 2.0\text{ V}$ , $V_{FB} = 2.2\text{ V}$	2.0	8.0	–	mA
Output Source Current	$V_{COMP} = 2.0\text{ V}$ , $V_{FB} = 1.8\text{ V}$	2.0	6.0	–	mA
$V_{COMP}$ High	$V_{FB} = 1.8\text{ V}$	3.3	3.5	3.7	V
$V_{COMP}$ Low	$V_{FB} = 2.2\text{ V}$	0.85	1.0	1.15	V
PSRR	$10\text{ V} < V_{CC} < 45\text{ V}$ , $V_{FB} = V_{COMP}$ , Note 3	60	70	–	dB

## Voltage Reference

Output Voltage Initial Accuracy	$V_{CC} = 15\text{ V}$ , $T = 25^{\circ}\text{C}$ , Note 3	4.9	5.0	5.1	V
Output Voltage	$0\text{ A} < I_{REF} < 8.0\text{ mA}$	4.8	5.0	5.2	V
Line Regulation	$10\text{ V} < V_{CC} < 45\text{ V}$ , $I_{REF} = 0\text{ A}$	–	10	60	mV
Load Regulation	$0\text{ A} < I_{REF} < 8.0\text{ mA}$	–	20	60	mV
Current Limit	$V_{REF} = 4.8\text{ V}$	10	50	–	mA
$V_{REF\_OK}$ FAULT V	$V_{SYNC} = 5.0\text{ V}$ , $V_{REF} = V_{LOAD}$	4.10	4.40	4.60	V
$V_{REF\_OK}$ V	$V_{SYNC} = 5.0\text{ V}$ , $V_{REF} = V_{LOAD}$	4.30	4.50	4.80	V
$V_{REF\_OK}$ Hysteresis	–	40	100	250	mV

## Current Sense Amplifier

IS COMP High V	$IS+ = 5.0\text{ V}$ , $IS- = IS\text{ COMP}$	4.7	5.0	5.3	V
IS COMP Low V	$IS+ = 0\text{ V}$ , $IS- = IS\text{ COMP}$	0.5	1.0	1.3	V
Source Current	$IS+ = 5.0\text{ V}$ , $IS- = 0\text{ V}$	2.0	10	–	mA
Sink Current	$IS- = 5.0\text{ V}$ , $IS+ = 0\text{ V}$	10	20	–	mA
Open Loop Gain	$1.5\text{ V} \leq V_{COMP} \leq 4.5\text{ V}$ , $R_L = 4.0\text{ k}\Omega$	60	80	–	dB
CMRR	Note 3	60	80	–	dB
PSRR	$10\text{ V} < V_{CC} < 45\text{ V}$ , Note 3	60	80	–	dB
Unity Gain Bandwidth	$1.5\text{ V} \leq V_{COMP} \leq 4.5\text{ V}$ , $R_L = 4.0\text{ k}\Omega$ , Note 3	0.5	0.8	–	MHz
Input Offset Voltage	$V_{IS+} = 2.5\text{ V}$ , $V_{IS-} = V_{ISCOMP}$	–8.0	0	8.0	mV
Input Bias Currents	$V_{IS+} = V_{IS-} = 0\text{ V}$ , $I_{IS}$ flows out of pins	–	20	250	nA
Input Offset Current ( $IS+$ , $IS-$ )	–	–250	0	250	nA
Input Signal Voltage Range	Note 3	–0.3	–	$V_{CC} - 4.0$	V

## RAMP/SYNC Generator

RAMP Source Current Initial Accuracy	$V_{SYNC} = 5.0\text{ V}$ , $V_{RAMP} = 2.5\text{ V}$ , $T = 25^{\circ}\text{C}$ , Note 3	0.18	0.20	0.22	mA
RAMP Source Current	$V_{SYNC} = 5.0\text{ V}$ , $V_{RAMP} = 2.5\text{ V}$	0.16	0.20	0.24	mA
RAMP Sink Current	$V_{SYNC} = 0\text{ V}$ , $V_{RAMP} = 2.5\text{ V}$	1.0	4.0	–	mA
RAMP Peak Voltage	$V_{SYNC} = 5.0\text{ V}$	3.3	3.5	3.7	V
RAMP Valley Voltage	$V_{SYNC} = 0\text{ V}$	1.4	1.5	1.6	V
RAMP Dynamic Range	$V_{RAMPDR} = V_{RAMP PK} - V_{RAMP VY}$	1.7	2.0	2.3	V
RAMP Sleep Threshold Voltage	$V_{RAMP}$ @ $V_{REF} < 2.0\text{ V}$	0.3	0.6	1.0	V
SYNC Threshold	$V_{SYNC}$ @ $V_{RAMP} > 2.5\text{ V}$	2.3	2.5	2.7	V
SYNC Input Bias Current	$V_{SYNC} = 0\text{ V}$ , $I_{SYNC}$ flows out of pin	–	1.0	20	$\mu\text{A}$

3. Guaranteed by design. Not 100% tested in production.

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**ELECTRICAL CHARACTERISTICS** ( $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $10\text{ V} < V_{CC} < 45\text{ V}$ ,  $8.0\text{ V} < V_C < 75\text{ V}$ ; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>Output Stage</b>					
$V_G$ , High	$V_{SYNC} = 5.0\text{ V}$ , $I_{VG} = 200\text{ mA}$ , $V_C - V_G$	–	1.6	2.5	V
$V_G$ , Low	$V_{SYNC} = 0\text{ V}$ , $I_{VG} = 200\text{ mA}$	–	0.9	1.5	V
$V_G$ Rise Time	Switch $V_{SYNC}$ High, $C_G = 1.0\text{ nF}$ , $V_{CC} = 15\text{ V}$ , measure 2.0 V to 8.0 V	–	30	75	ns
$V_G$ Fall Time	Switch $V_{SYNC}$ Low, $C_G = 1.0\text{ nF}$ , $V_{CC} = 15\text{ V}$ , measure 8.0 V to 2.0 V	–	40	100	ns
$V_G$ Resistance to GND	Remove supplies, $V_G = 10\text{ V}$	–	50	100	k $\Omega$
$V_D$ Resistance to GND	Remove supplies, $V_D = 10\text{ V}$	500	1500	–	$\Omega$

## General

$I_{CC}$ , Operating	$V_{SYNC} = 5.0\text{ V}$	–	12	18	mA
$I_{CC}$ in UVL	$V_{CC} = 6.0\text{ V}$	–	300	500	$\mu\text{A}$
$I_{CC}$ in Sleep Mode High	$V_{RAMP} = 0\text{ V}$ , $V_{CC} = 45\text{ V}$	–	80	200	$\mu\text{A}$
$I_{CC}$ in Sleep Mode Low	$V_{RAMP} = 0\text{ V}$ , $V_{CC} = 10\text{ V}$	–	20	50	$\mu\text{A}$
$I_C$ , Operating High	$V_{SYNC} = 5.0\text{ V}$ , $V_{FB} = V_{IS-} = 0\text{ V}$ , $V_C = 75\text{ V}$	–	4.0	8.0	mA
$I_C$ , Operating Low	$V_{SYNC} = 5.0\text{ V}$ , $V_{FB} = V_{IS-} = 0\text{ V}$ , $V_C = 8.0\text{ V}$	–	3.0	6.0	mA
UVLO Start Voltage	–	7.4	8.0	9.2	V
UVLO Stop Voltage	–	6.4	7.0	8.3	V
UVLO Hysteresis	–	0.8	1.0	1.2	V
Leading Edge, $t_{DELAY}$	$V_{SYNC} = 2.5\text{ V}$ to $V_G = 8.0\text{ V}$	–	280	–	ns
Trailing Edge, $t_{DELAY}$	$V_{SYNC} = 2.5\text{ V}$ to $V_G = 2.0\text{ V}$	–	750	–	ns

## PACKAGE PIN DESCRIPTION

PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
PDIP-14	SO-16WB		
1	1	SYNC	Synchronization input.
2	2	$V_{CC}$	Logic supply (10 V to 45 V).
3	3	$V_{REF}$	5.0 V voltage reference.
4	–	LGND	Logic level ground (analog and digital ground tied).
5	6	$V_{FB}$	Error amplifier inverting input.
6	7	COMP	Error amplifier output and compensation.
7	8	RAMP	RAMP programmable with the external capacitor.
8	9	IS+	Current sense amplifier non-inverting input.
9	10	IS–	Current sense amplifier inverting input.
10	11	IS COMP	Current sense amplifier compensation and output.
11	12, 13	PGND	Power ground.
12	14	$V_G$	External power switch gate drive.
13	15	$V_C$	Output power stage supply voltage (8.0 V to 75 V).
14	16	$V_D$	External FET DRAIN voltage monitor.
–	5	AGND	Analog ground.
–	4	DGND	Digital ground.

# CS5101

## ORDERING INFORMATION

Device	Package	Shipping†
CS5101EN14	PDIP-14	25 Units / Rail
CS5101EN14G	PDIP-14 (Pb-Free)	
CS5101EDW16	SOIC-16WB	47 Units / Rail
CS5101EDW16G	SOIC-16WB (Pb-Free)	
CS5101EDWR16	SOIC-16WB	1000 / Tape & Reel
CS5101EDWR16G	SOIC-16WB (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## CIRCUIT DESCRIPTION

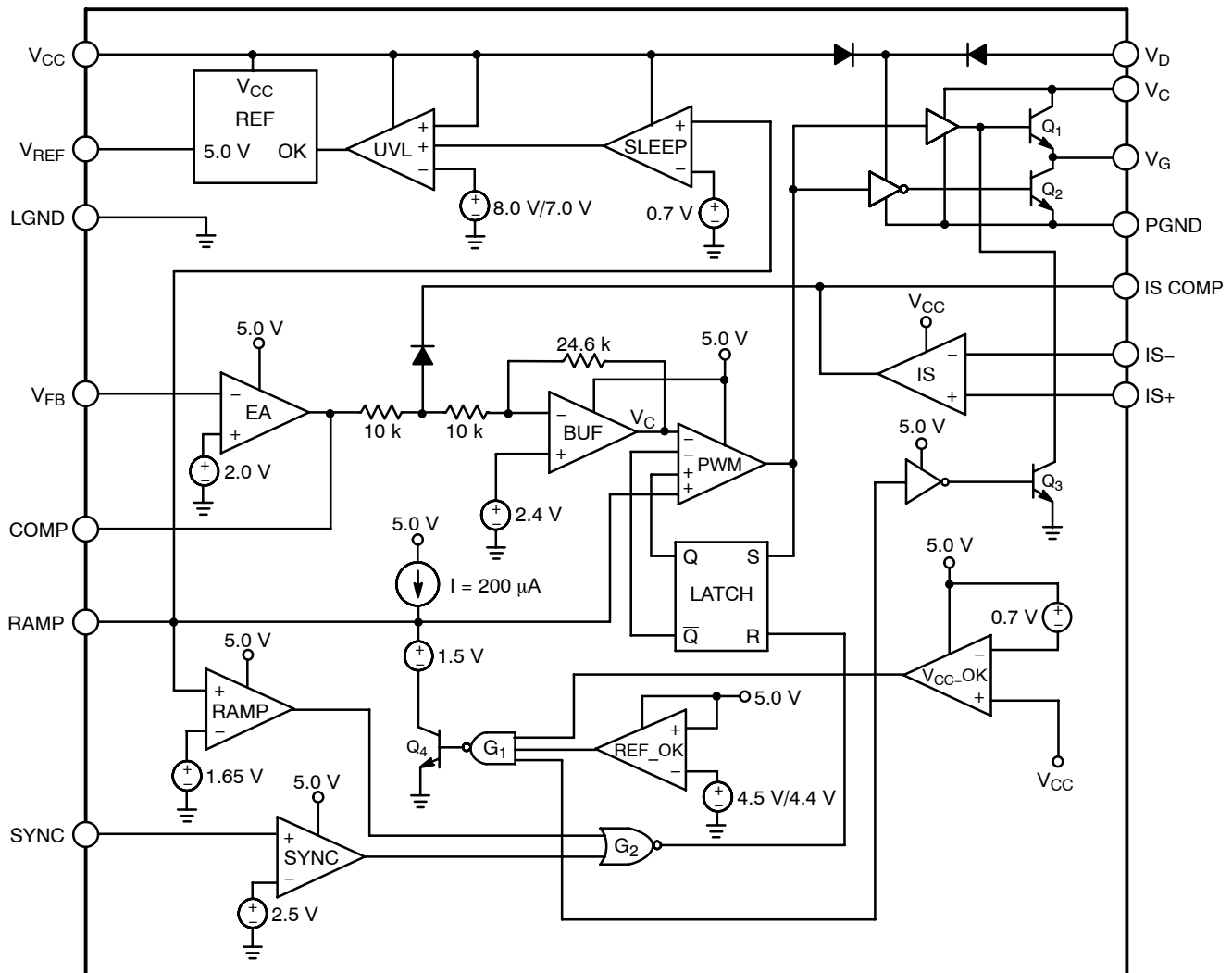


Figure 2. Block Diagram

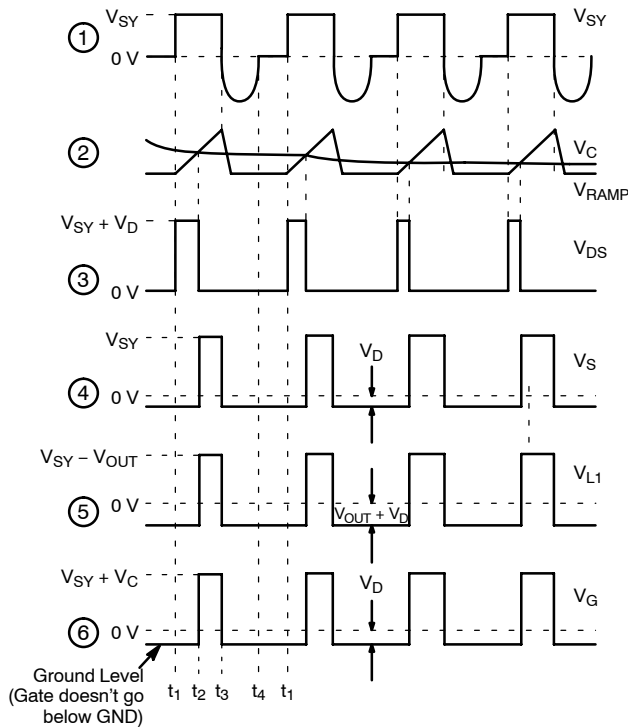
### Theory of Operation

The CS5101 is designed to regulate voltages in multiple output power supplies. Functionally, it is similar to a magnetic amplifier, operating as a switch with a delayed turn-on. It can be used with both single ended and dual ended topologies.

The  $V_{FB}$  voltage is monitored by the error amplifier EA. It is compared to an internal reference voltage and the amplified differential signal is fed through an inverting amplifier into the buffer, BUF. The buffered signal is compared at the PWM comparator with the ramp voltage generated by capacitor  $C_R$ . When the ramp voltage  $V_R$  exceeds the control voltage  $V_C$ , the output of the PWM comparator goes high, latching its state through the LATCH, the output stage transistor  $Q_1$  turns on, and the external power switch, usually an N-FET, turns on.

### SYNC Function

The SYNC circuit is activated at time  $t_1$  (Figure 3) when the voltage at the SYNC pin exceeds the threshold level (2.5V) of the SYNC comparator. The external ramp capacitor  $C_R$  is allowed to charge through the internal current source  $I$  (200  $\mu$ A). At time  $t_2$ , the ramp voltage intersects with the control voltage  $V_C$  and the output of the PWM comparator goes high, turning on the output stage and the external power switch. At the same time, the PWM comparator is latched by the RS latch, LATCH.



**Figure 3. Waveforms for CS5101. The Number to the Left of Each Curve Refers to a Node On the Application Diagram on Page 2.**

The logic state of the LATCH can be changed only when both the voltage level of the trailing edge of the power pulse at the SYNC pin is less than the threshold voltage of the SYNC comparator (2.5 V) and the RAMP voltage is less than the threshold voltage of the RAMP comparator (1.65 V). On the negative going transition of the secondary side pulse  $V_{SY}$ , gate  $G_2$  output goes high, resetting the latch at time  $t_3$ . Capacitor  $C_R$  is discharged through transistor  $Q_4$ .  $C_R$ 's output goes low disabling the output stage, and the external power switch (an N-FET) is turned off.

### RAMP Function

The value of the ramp capacitor  $C_R$  is based on the switching frequency of the regulator and the maximum duty cycle of the secondary pulse  $V_{SY}$ .

If the RAMP pin is pulled externally to 0.3 V or below, the SSPR is disabled. Current drawn by the IC is reduced to less than 100  $\mu$ A, and the IC is in SLEEP mode.

### FAULT Function

The voltage at the  $V_{CC}$  pin is monitored by the undervoltage lockout comparator with hysteresis. When  $V_{CC}$  falls below the UVL threshold, the 5.0 V reference and all the circuitry running off of it is disabled. Under this condition the supply current is reduced to less than 500  $\mu$ A.

The  $V_{CC}$  supply voltage is further monitored by the  $V_{CC\_OK}$  comparator. When  $V_{CC}$  is reduced below  $V_{REF} - 0.7$  V, a fault signal is sent to gate  $G_1$ . This fault signal, which determines if  $V_{CC}$  is absent, works in conjunction with the ramp signal to disable the output, but only after the current cycle has finished and the RS latch is reset. Therefore this fault will not cause the output to turn off during the middle of an on pulse, but rather will utilize lossless turn-off. This feature protects the FET from overvoltage stress. This is accomplished through gate  $G_1$  by driving transistor  $Q_4$  on.

An additional fault signal is derived from the  $REF\_OK$  comparator.  $V_{REF}$  is monitored so to disable the output through gate  $G_1$  when the  $V_{REF}$  voltage falls below the OK threshold. As in the  $V_{CC\_OK}$  fault, the  $REF\_OK$  fault disables the output after the current cycle has been completed. The fault logic will operate normally only when  $V_{REF}$  voltage is within the specification limits of  $REF\_OK$ .

### DRAIN Function

The drain pin,  $V_D$  monitors the voltage on the drain of the power switch and derives energy from it to keep the output stage in an off state when  $V_C$  or  $V_{CC}$  is below the minimum specified voltage.

## CS5101

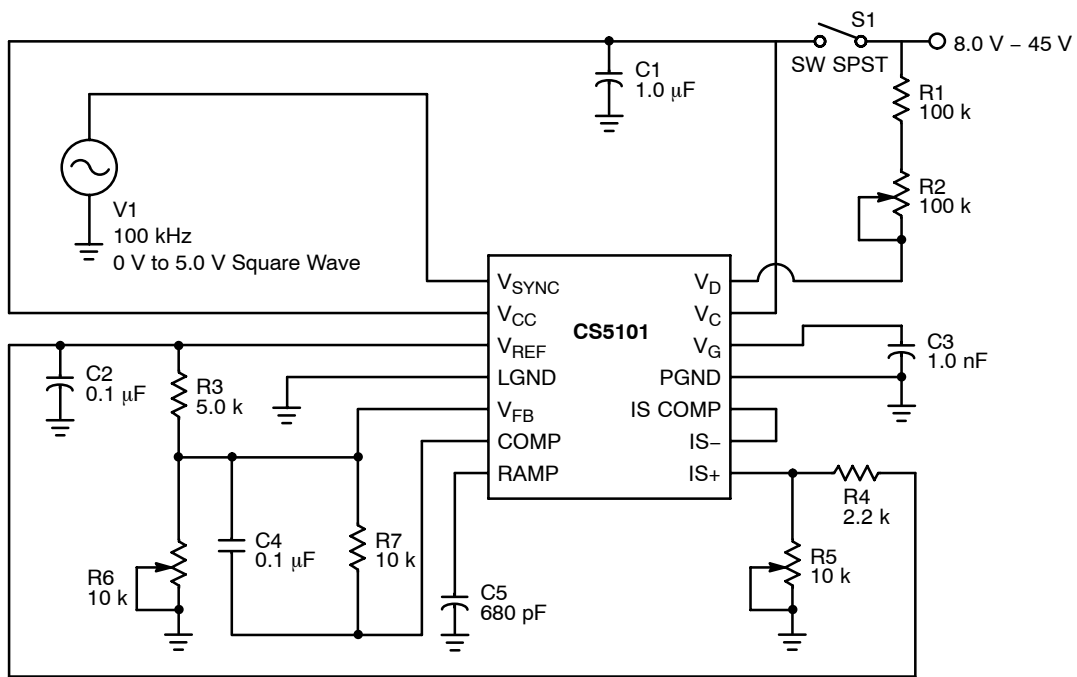
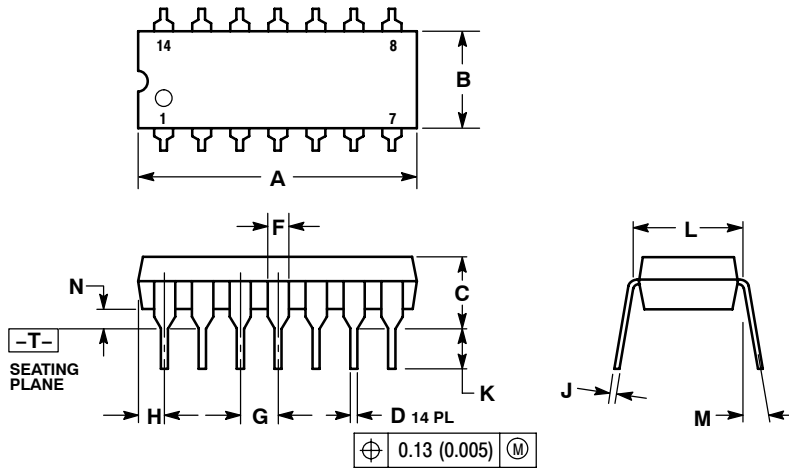


Figure 4. CS5101 Bench Test on DIP-14 Package

# CS5101

## PACKAGE DIMENSIONS

**PDIP-14**  
CASE 646-06  
ISSUE P



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

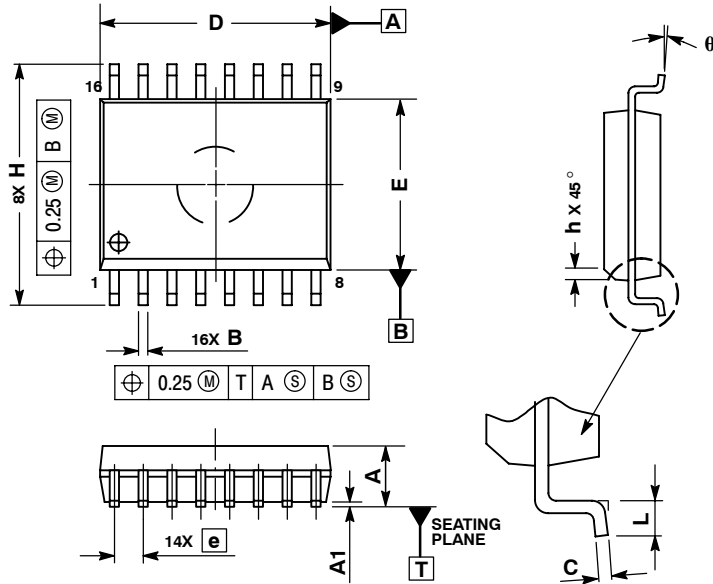
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10 °	---	10 °
N	0.015	0.039	0.38	1.01



# CS5101

## PACKAGE DIMENSIONS

### SOIC-16WB CASE 751G-03 ISSUE C




#### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27	BSC
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

#### PACKAGE THERMAL DATA

Parameter		PDIP-14	SOIC-16WB	Unit
R <sub>θJC</sub>	Typical	23	48	°C/W
R <sub>θJA</sub>	Typical	105	85	°C/W

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