490μA, 2MHz, rail-to-rail I/O CMOS op-amp

1 Features

- Single-Supply Operation from +2.1V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product:2MHz (Typ)
- Low Input Bias Current: 100pA (Typ)
- Low Offset Voltage: 3.5mV (Max)
- Quiescent Current:490μA per Amplifier (Typ)
- Operating Temperature:-40°C~125°C
- Small Package:
  LMV321B-VR Available in SOT23-5, SOP-8 Packages
  LMV358B-VR Available in SOP-8 and MSOP-8 Packages
  LMV324B-VR Available in SOP-14 and TSSOP-14 Packages

2 Applications

- Sensors
- Active Filters
- Cellular and Cordless Phones
- Audio
- Handheld Test Equipment
- Battery-Powered Instrumentation
- A/D Converters

3 General Description

The LMV3**B-VR series have a high gain-bandwidth product of 2MHz, a slew rate of 4.2V/μs, and a quiescent current of 490μA per amplifier at 5V. The LMV3**B-VR series are designed to provide optimal performance in low voltage and low noise systems. They provide rail-to-rail output swing into heavy loads. The input common mode voltage range includes ground, and the maximum input offset voltage is 3.5mV for LMV3**B-VR series. They are specified over the extended industrial temperature range (-40°C to +125°C). The operating range is from 2.1V to 5.5V.

4 Pin Configuration

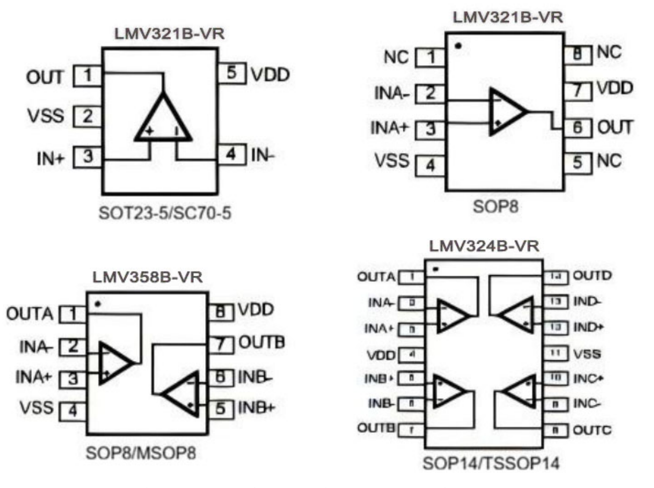


Figure 1. Pin Assignment Diagram

Table of Contents

5 Specifications

5.1 Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage (VDD to Vss)	-0.5V	+7.5V
Analog Input Voltage (IN+ or IN-)	Vss-0.5V	VDD+0.5V
PDB Input Voltage	Vss-0.5V	+7V
Operating Temperature Range	-40°C	+125°C
Junction Temperature	+160°C	
Storage Temperature Range	-55°C	+150°C
Lead Temperature (soldering, 10sec)	+260°C	
Package Thermal Resistance (TA=+25°C)		
SOP-8, θ_{JA}	125°C/W	
MSOP-8, θ_{JA}	216°C/W	
SOT23-5, θ_{JA}	190°C/W	
SC70-5, θ_{JA}	333°C/W	
ESD Susceptibility		
HBM	6.5kV	
CDM	1kV	

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.2 Package/Ordering Information

MODEL	CHANNEL	PACKAGE DESCRIPTION	MARKING INFORMATION
LMV321B-VR	Single	SOT23-5	LMV321-S
		SOP-8	LMV321-S
LMV358B-VR	Dual	SOP-8	LMV358-S
		MSOP-8	LMV358-S
LMV324B-VR	Quad	TSSOP-14	LMV324-S
		SOP-14	LMV324-S

5.3 Electrical Characteristics

(At Vs=5V, T_A = +25°C , V_{CM} = V_S/2, R_L = 600 Ω , unless otherwise noted.)

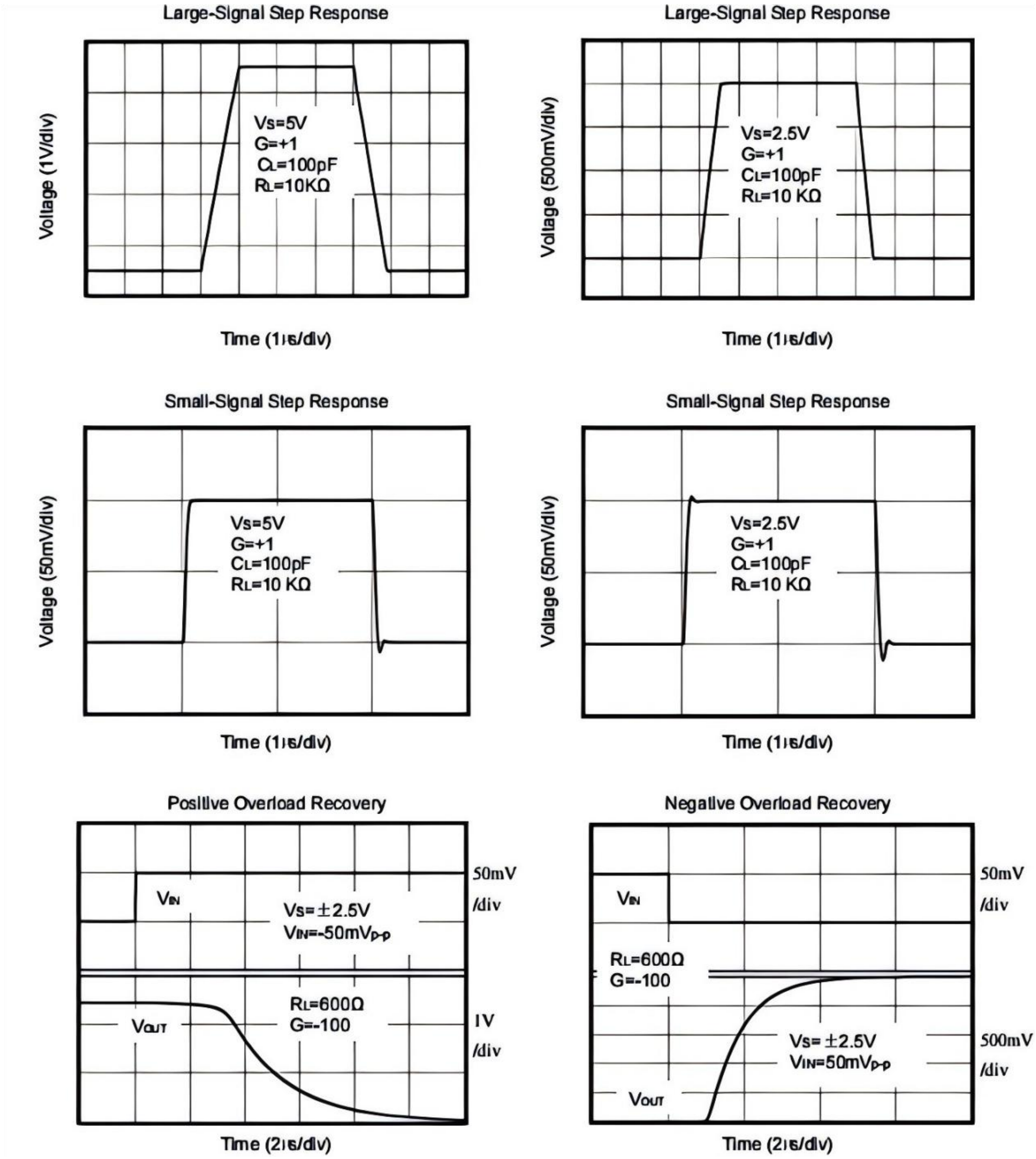
PARAMETER	CONDITIONS	LMV3**B-VR series

		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input Offset Voltage (V_{OS})			1.2	4	mV
Input Bias Current(I_B)			100		pA
Input Ofset Current (I_{OS})			100		pA
Input Common Mode Voltage Range(V_{CM})	Vs=5.5V		-0.1 to +5.6		V
Common Mode Rejection Ratio(CMRR)	Vs=5.5V, V_{CM}= -0.1V to 4V	60	75		dB
	Vs=5.5V, V_{CM}= -0.1V to 5.6V		83		dB
Open-Loop Voltage Gain(AaL)	R_L=600Ω,V_O= 0.15V to 4.85V	79	97		dB
	R_L=10kΩ,V_O= 0.05V to 4.95V		108		dB
Input Offset Voltage Drift (△V_{OS}/△T)			2.4		µV/ °C
OUTPUT CHARACTERISTICS					
Output Voltage Swing from Rail	R_L=600Ω		0.1		V
	R_L=10kΩ		0.015		V
Output Current(I_{OUT})		20	40		mA
Closed-Loop Output Impedance	f=200kHz, G=1		3		Ω
POWER-DOWN DISABLE					
Tum-On Time			4		µs
Tum-Off Time			1.2		µs
POWER SUPPLY					
Operating Voltage Range			2.1 to 5.5		V
Power Supply Rejection Ratio (PSRR)	Vs=+2.5Vto +5.5V, V_{CM}=(-Vs)+0.5V	60	70		dB
Quiescent Current/ Amplifier (I_Q)	I_{OUT}=0		490	620	µA
Dynamic Performance					
Gain-Bandwidth	R_L = 10kΩ, C_L = 100pF		2		MHz

PARAMETER	CONDITIONS	LMV3**B-VR series			
		MIN	TYP	MAX	UNIT
Product (GBP)					
Phase Margin (φ_O)	R_L = 10kΩ, C_L = 100pF		53		°
Slew Rate (SR)	G = +1, 2V Step, R_L = 10kΩ		2		V/μs
Settling Time to 0.1% (t_S)	G = +1, 2V Step, R_L = 600Ω		0.4		μs
Overload Recovery Time	V_{IN}*G= V_S, R_L = 600Ω				μs
Voltage Noise Density (en)	f = 1kHz		30		$nV/\sqrt{Hz}$
	f = 10kHz		20		

5.4 Typical Performance Characteristics

(At V_S=5V, TA = +25℃ , V_{CM} = V_S/2, R_L = 600Ω, unless otherwise noted.)



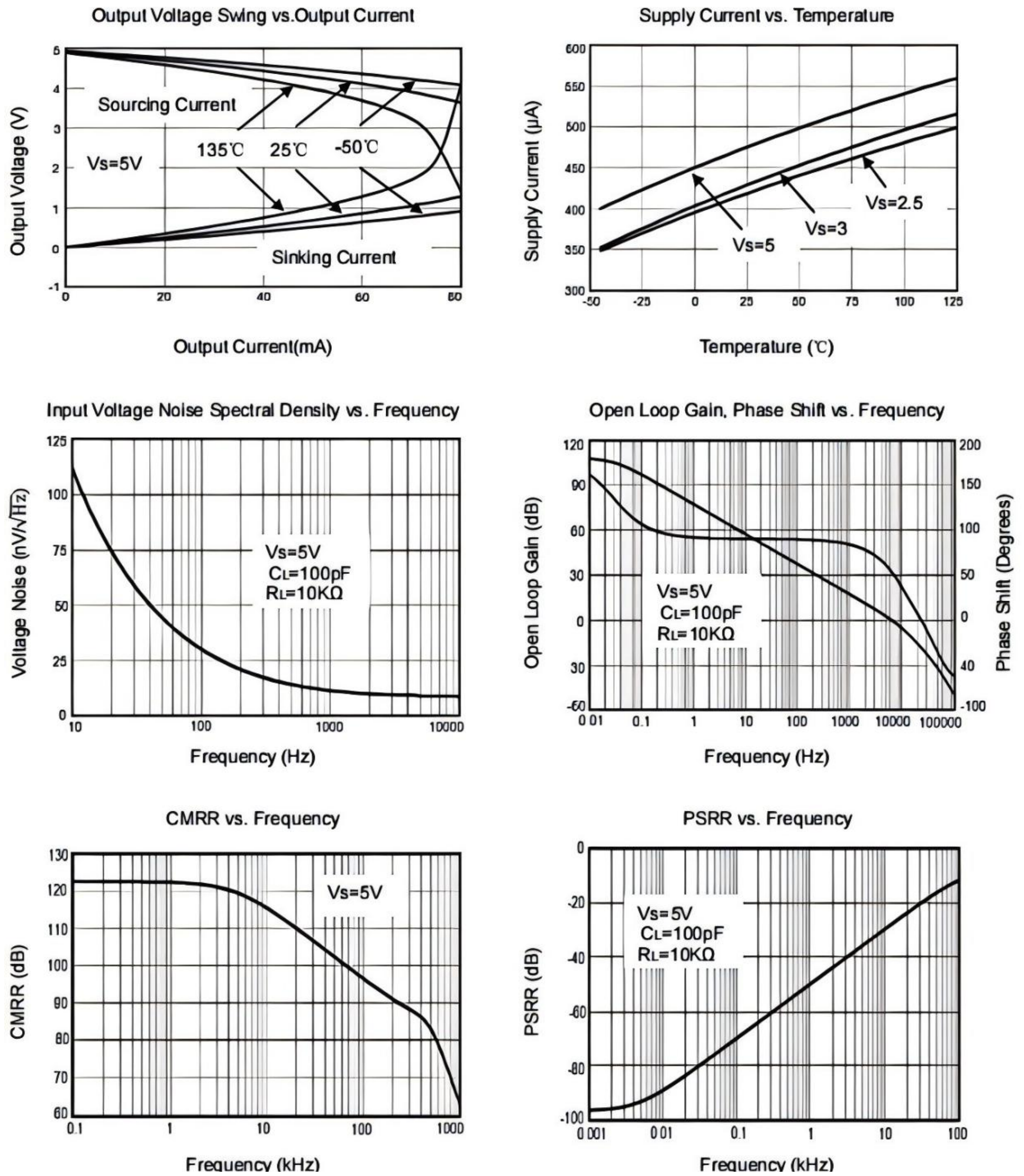


Figure 2. Typical Performance Characteristics

6 Application Note

6.1 Size

LMV3**B-VR series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the LMV3**B-VR series packages save space on printed circuit boards and enable the design of smaller electronic products.

6.2 Power Supply Bypassing and Board Layout

LMV3**B-VR series operates from a single 2.1V to 5.5V supply or dual ±1.05V to ±2. 75V supplies. For best performance, a 0.1µF ceramic capacitor should be placed close to the VDD pin in single supply operation. For dual supply operation, both VDD and VSS supplies should be bypassed to ground with separate 0.1µF ceramic capacitors.

6.3 Low Supply Current

The low supply current (typical 490µA per channel) of LMV3**B-VR series will help to maximize battery life. They are ideal for battery powered systems.

6.4 Operating Voltage

LMV3**B-VR series operate under wide input supply voltage (2.1V to 5.5V). In addition, all temperature specifications apply from -40°C to +125°C. Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime.

6.5 Rail-to-Rail Input

The input common-mode range of LMV3**B-VR series extends 100mV beyond the supply rails (VSS-0.1V to VDD+0.1V). This is achieved by using complementary input stage .For normal operation, inputs should be limited to this range.

6.6 Rail-to-Rail Output

Rail-to-Rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating in low supply voltages. The output voltage of LMV3**B-VR series can typically swing to less than 2mV from supply rail in light resistive loads (>100kΩ), and 60mV of supply rail in moderate resistive loads (10kΩ).

6.7 Capacitive Load Tolerance

The LMV3**B-VR series is optimized for bandwidth and speed, not for driving capacitive loads. Output capacitance will create a pole in the amplifier's feedback path, leading to excessive peaking and potential oscillation. If dealing with load capacitance is a requirement of the application, the two strategies to consider are :

(1) using a small resistor in series with the amplifier's output and the load capacitance;
(2) reducing the bandwidth of the amplifier's feedback loop by increasing the overall noise gain.

Figure 3. shows a unity gain follower using the series resistor strategy. The resistor isolates the output from the capacitance and, more importantly, creates a zero in the feedback path that compensates for the pole created by the output capacitance.

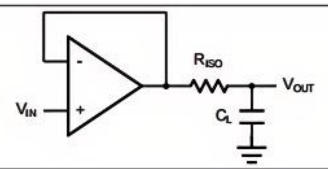


Figure 3. Indirectly Driving a Capacitive Load Using Isolation Resistor

The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. However, if there is a resistive load R_L in parallel with the capacitive load, a voltage divider (proportional to R_{ISO}/R_L) is formed, this will result in a gain error.

The circuit in Figure 4 is an improvement to the one in Figure 3. R_F provides the DC accuracy by feed-forward the V_{IN} to R_L. CF and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased by increasing the value of CF. This in turn will slow down the pulse response.

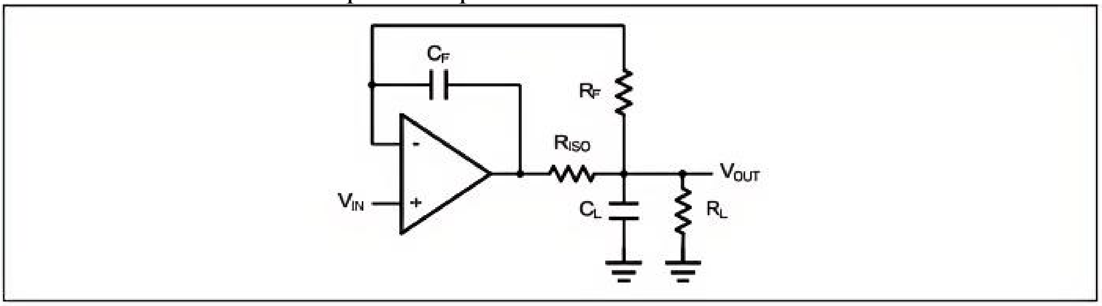


Figure 4. Indirectly Driving a Capacitive Load with DC Accuracy

7 Typical Application Circuits

7.1 Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common the two inputs. It is useful as a computational amplifier in making a differential to single-end conversion or in rejecting a common mode signal. Figure 4. shown the differential amplifier using LMV3**B-VR series.

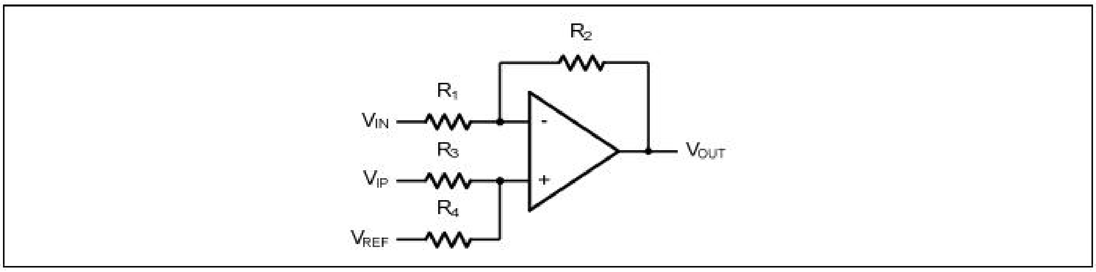


Figure 5. Differential Amplifier

$$V_{OUT}=\frac{(R_1+R_2)}{(R_3+R_4)}\frac{R_4}{R_1}V_{IN}-\frac{R_2}{R_1}V_{IP}+\left(\frac{R_1+R_2}{R_3+R_4}\right)\frac{R_{03}}{R_1}V_{REF}$$

If the resistor ratios are equal (i.e. $R_1=R_3$ and $R_2=R_4$), then

$$V_{OUT}=\frac{R_2}{R_1}(V_{IP}-V_{IN})+V_{REF}$$

7.2 Low Pass Active Filter

The low pass active filter is shown in Figure 6. The DC gain is defined by –R2/R1. The filter has a -20dB/decade roll-off after its corner frequency $f_C=1/(2\pi R_3C_1)$.

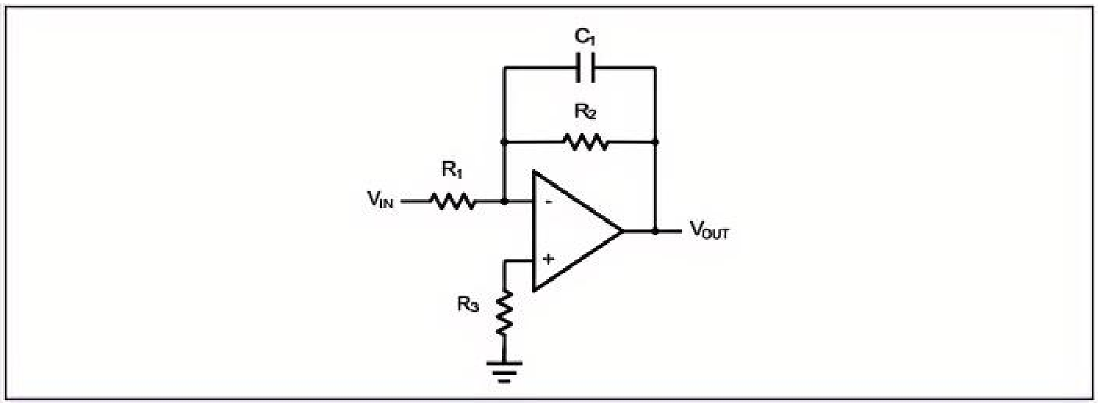


Figure 6. Low Pass Active Filter

7.3 Instrumentation Amplifier

The triple LMV3**B-VR series can be used to build a three-op-mp instrumentation amplifier asshown in Figure 6.

The amplifier in Figure 7 is a high input impedance differential amplifier with gain of R2/R1. The two differential voltage followers assure the high input impedance of the amplifier.

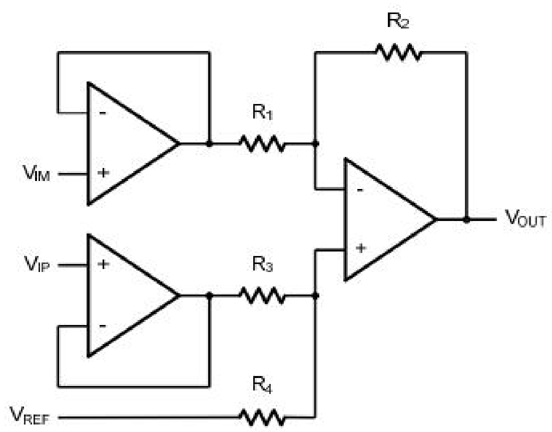


Figure 7. Instrument Amplifier

8 Package Information

8.1 MSOP-8

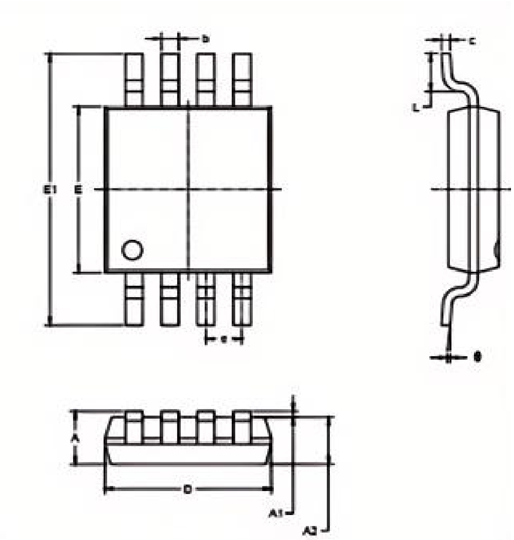


Figure 8. MSOP8 Package

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.850	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.850 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	8	0°	6°

8.2 SOP-8

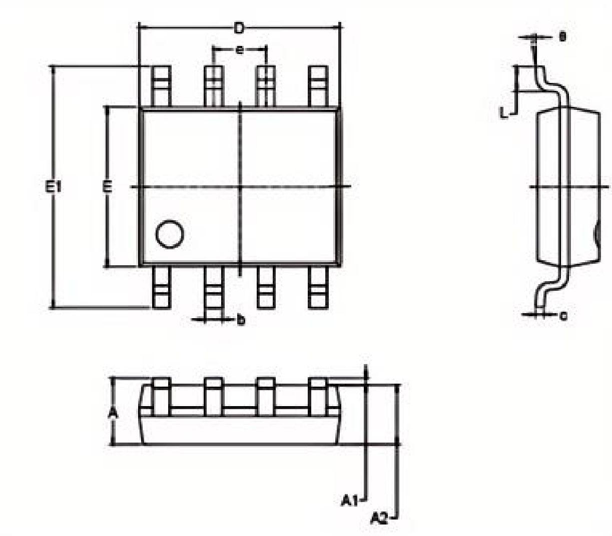


Figure 9. SOP8 Package

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

8.3 SOT23-5

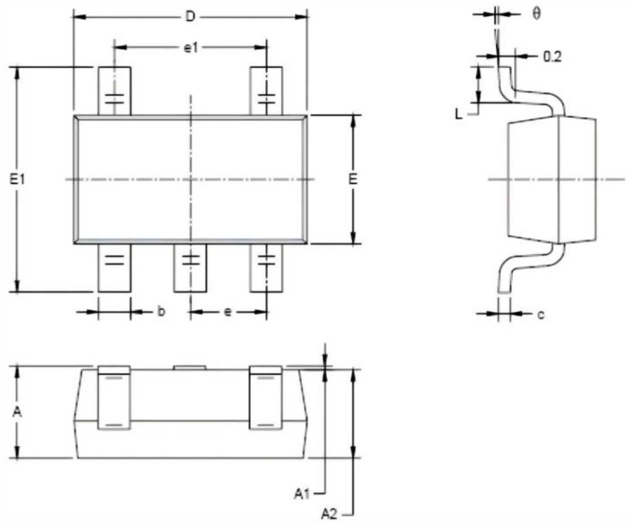


Figure 10. SOT23-5 Package

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

8.4 SC70-5

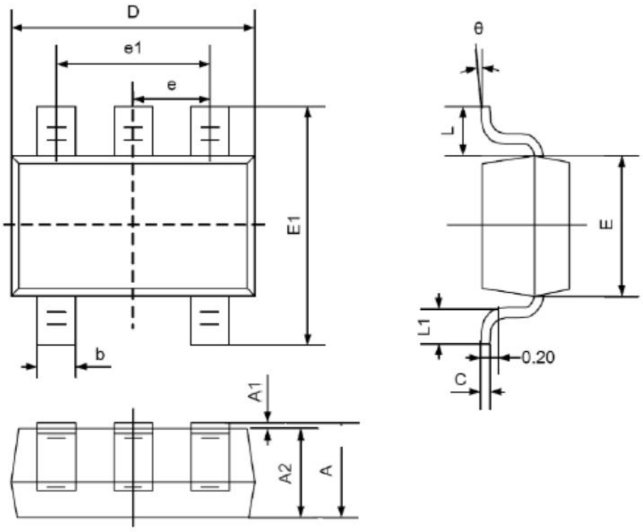


Figure 11. SC70-5 Package

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	**Max.**	**Min.**	**Max.**
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.525 REF.		0.021 REF.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

8.5 TSSOP-14

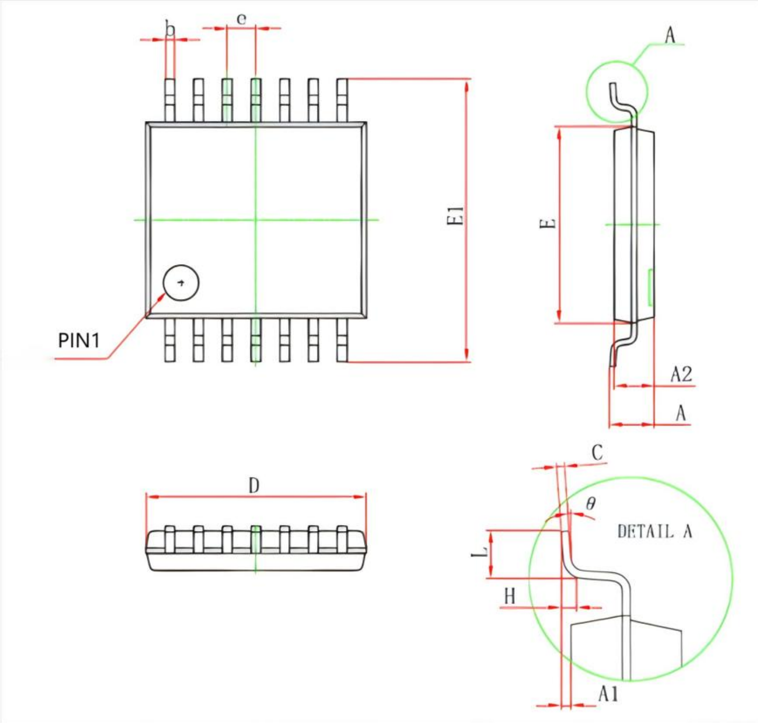


Figure 12. TSSOP-14 Package

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

8.6 SOP-14

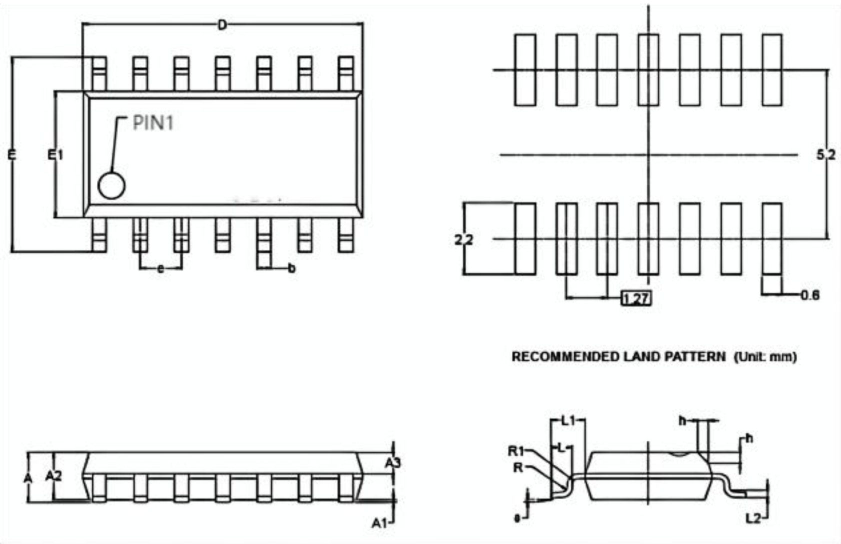


Figure 13. SOP14 Package

Symbol	Dimensions In Millimeters			Dimensions In Inches		
	MIN	MOD	MAX	MIN	MOD	MAX
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.25		1.65	0.049		0.065
A3	0.55		0.75	0.022		0.030
b	0.36		0.49	0.014		0.019
D	8.53		8.73	0.336		0.344
E	5.80		6.20	0.228		0.244
E1	3.80		4.00	0.150		0.157
e	1.27 BSC			0.050 BSC		
L	0.45		0.80	0.018		0.032
L1	1.04 REF			0.040 REF		
L2	0.25 BSC			0.01 BSC		
R	0.07			0.003		
R1	0.07			0.003		
h	0.30		0.50	0.012		0.020
θ	0°		8°	0°		8°