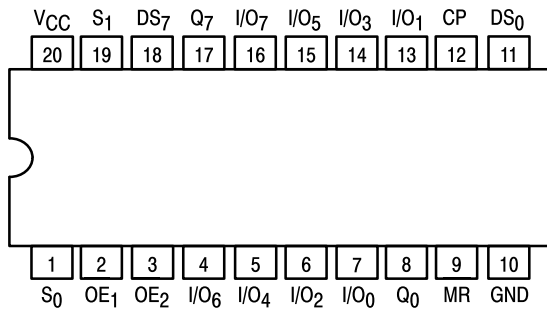# MOTOROLA

8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS

The MC74F299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
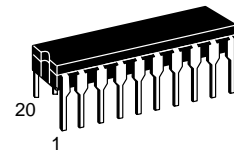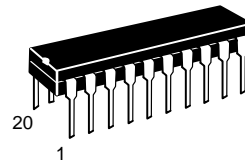- Input Clamp Diodes Limit High-Speed Termination Effects

MC74F299

8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS

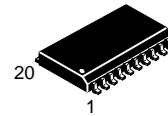### FAST™ SCHOTTKY TTL

J SUFFIX
CERAMIC
CASE 732-03

N SUFFIX
PLASTIC
CASE 738-03

DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

CONNECTION DIAGRAM

V_{CC}	S_1	DS_7	Q_7	I/O_7	I/O_5	I/O_3	I/O_1	CP	DS_0
20	19	18	17	16	15	14	13	12	11

1	2	3	4	5	6	7	8	9	10
S_0	OE_1	OE_2	I/O_6	I/O_4	I/O_2	I/O_0	Q_0	MR	GND

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−1.0/−3.0	mA
I_{OL}	Output Current — Low	74			20/24	mA

MC74F299

FUNCTION TABLE

Inputs				Response
MR	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset: Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load: I/O_n Q_n
H	L	H	↑	Shift Right: DS_0 Q_0, Q_0 Q_1, etc.
H	H	L	↑	Shift Left: DS_7 Q_7, Q_7 Q_6, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH clock transition.

FUNCTIONAL DESCRIPTION

The MC74F299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-LOW Master Reset is used to reset the register.

The MC74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on MR overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter			Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage					0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage					−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	Q_0/Q_7	74	2.5			V	I_{OH} = −1.0 mA	V_{CC} = 4.5 V
			74	2.7					V_{CC} = 4.75 V
		I/O	74	2.7	3.4		V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
			74	2.4					V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	Q_0/Q_7				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
		I/O				0.5		I_{OL} = 24 mA	
I_{IH}	Input HIGH Current	Q_0/Q_7				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		I/O				70			
		Q_0/Q_7				0.1	mA	V_{CC} = MAX	V_{IN} = 7.0 V
		I/O				1.0			V_{IN} = 5.5 V
I_{IL}	Input LOW Current	S_0, S_1				−1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
		Other Inputs				−0.6			
I_{OZH}	Off-State Output Current, High-Level Voltage Applied					70	μA	V_{CC} = MAX	V_{OUT} = 2.7 V
						1.0	mA		V_{OUT} = 5.5 V
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied					−0.6	mA	V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)			−60		−150	mA	V_{CC} = MAX	V_{OUT} = 0 V
I_{CC}	Total Supply Current					95	mA		OE = HIGH, CP = HIGH

NOTES:
1. For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at one time, nor for more than 1 second.

MC74F299

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF		74F $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0$ V $\pm 10\%$ $C_L = 50$ pF		Unit
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	70		70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	3.5 4.5	7.5 8.0	3.5 4.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O$_n$	3.5 4.0	9.0 9.0	3.5 4.0	10 10	ns
t_{PHL}	Propagation Delay MR to Q_0 or Q_7	5.5	9.5	5.5	10.5	ns
t_{PHL}	Propagation Delay MR to I/O$_n$	5.5	10	5.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH or LOW Level	3.5 4.0	8.0 10	3.5 4.0	9.0 11	ns
t_{PHZ} t_{PLZ}	Output Disable Time to HIGH or LOW Level	2.0 1.0	7.0 5.5	2.0 1.0	8.0 6.5	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			74F $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0$ V $\pm 10\%$ $C_L = 50$ pF		Unit
		Min	Typ	Max	Min	Max	
$t_{s(H)}$ $t_{s(L)}$	Set-Up Time, HIGH or LOW S_0 or S_1 to CP	6.5 6.5			7.5 7.5		ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0			0 0		ns
$t_{s(H)}$ $t_{s(L)}$	Set-Up Time, HIGH or LOW I/O$_n$, DS$_0$, DS$_7$ to CP	3.5 3.5			4.0 4.0		ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW I/O$_n$, DS$_0$, DS$_7$ to CP	0 1.0			0 1.0		ns
$t_{w(H)}$ $t_{w(L)}$	CP Pulse Width, HIGH or LOW	5.0 4.5			5.0 4.5		ns
$t_{w(L)}$	MR Pulse Width LOW	4.5			4.5		ns
t_{rec}	Recovery Time MR to CP	4.0			4.0		ns

Case 751D-03 DW Suffix
20-Pin Plastic
SO-20 (WIDE)
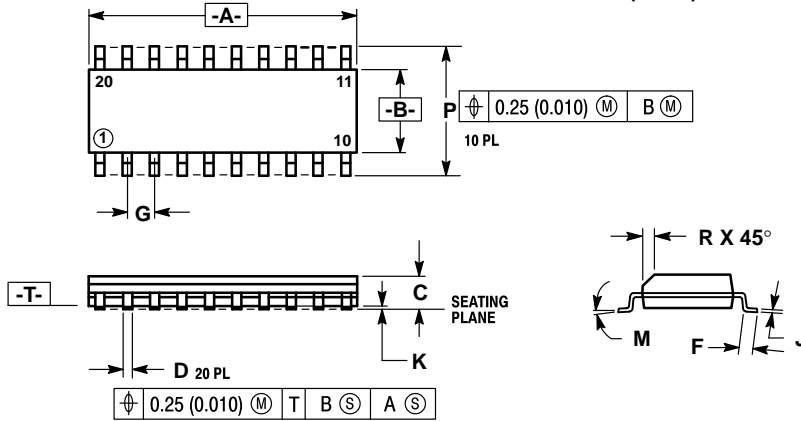
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Case 732-03 J Suffix
20-Pin Ceramic Dual In-Line
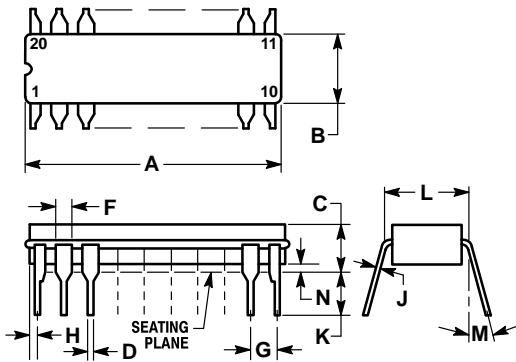
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

Case 738-03 N Suffix
20-Pin Plastic
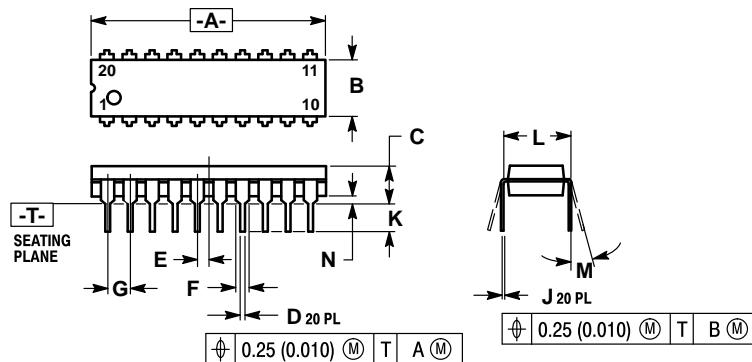
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

MOTOROLA

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