REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	I_{OZBH} parameter removed from Table I, C_{DP} added to Table I. Other typos corrected in Table I. ksr	00-12-01	Raymond Monnin
B	Boilerplate update and part of five year review. tcr	06-01-05	Raymond Monnin
C	Boilerplate update for five year review. lhl	12-02-06	Charles F. Saffle
D	Correct 1.2.4. Correct 1.3 and 3.10 to include Tuse = +55 degrees C for Data Retention. Update 3.9 and 3.10 to include sampling 20(0) for Endurance and Data Retention. Update boilerplate to current MIL-PRF-38535 requirements. Remove all Class M references. - lhl	14-04-10	Charles F. Saffle

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D												
SHEET	15	16	17	18	19	20	21	22												

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
00 – 02 – 29

REVISION LEVEL
D

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ELECTRICALLY ALTERABLE (IN-SYS REPROGRAMMABLE), 128 MACROCELL, PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

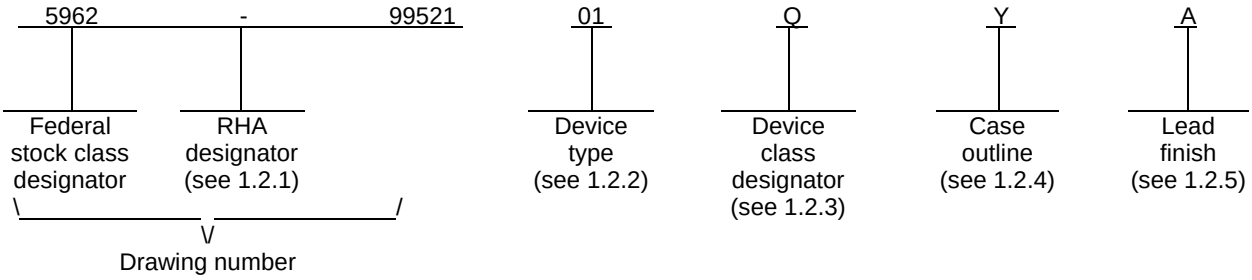
SIZE	CAGE CODE	
A	**67268**	**5962-99521**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Toggle Speed (MHz)
01	CY37128	128 Macrocell CPLD	100
02	CY37128	128 Macrocell CPLD	125

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	GQCC1-J84	84	J-leaded chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Programming supply voltage range (V_{PP})	4.5 V dc to 5.5 V dc
DC input voltage range	-0.5 V dc to +7.0 V dc
Maximum power dissipation	1.0 W 2/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline Y	See MIL-STD-1835
Junction temperature (T_J)	+150°C 3/
Storage temperature range	-65°C to +150°C
Endurance	25 erase/write cycles (minimum)
Data retention (at Tuse = +55ºC)	10 years (minimum)

1.4 Recommended operating conditions. 4/

Case operating temperature Range (T_C)	-55°C to +125°C
Supply voltage relative to ground (V_{CC})	+4.5V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ All voltage values in this drawing are with respect to V_{SS}

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the JEDEC Solid State Technology Association 2011, 3103 North 10th Street, Suite 240 South, Arlington, VA 22201-2107; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Processing CPLDs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.8.1 Erasure of CPLDs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6 herein.

3.8.2 Programmability of CPLDs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7 herein.

3.8.3 Verification of erasure or programmed CPLDs. When specified, devices shall be verified as either programmed (see 4.7 herein) to the specified pattern or erased (see 4.6 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.9 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device using 20(0) sampling. The methods and procedures may be vendor specific, but shall be under document control and shall be made available upon request.

3.10 Data Retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention using 20(0) sampling. The methods and procedures may be vendor specific, but shall guarantee 10 years minimum at Tuse = +55ºC. The vendor's procedure shall be kept under document control and shall be made available upon request by the preparing or acquiring activity, along with the test data.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8V I_{OH} = -2.0 mA, V_{IH} = 2.0 V 1/	1, 2, 3	All	2.4		V
High Level output voltage with Output Disabled 2/	V_{OHZ}	V_{CC} = 5.5 V, V_{IL} = 0.8 V I_{OH} = 0 µA, V_{IH} = 2.0 V 3/				4.5	V
		V_{CC} = 5.5 V, V_{IL} = 0.8 V I_{OH} = -150 µA, V_{IH} = 2.0 V 3/				3.6	V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 12.0 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V 1/				0.5	V
High level input voltage 4/	V_{IH}				2	V_{CC} + 0.5 V	V
Low level input voltage 4/	V_{IL}				-0.5	0.8	V
Input load current	I_{IX}	V_{IN} = 0 V or V_{CC}, with Busshold off			-10	+10	µA
Output leakage current	I_{OZ}	V_O = GND or V_{CC} = 5.5 V, Output disabled, Busshold off			-50	+50	µA
Output short circuit current 2/ 5/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V			-30	-160	mA
Power supply current 6/	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 V and 5.5 V f = 1.0 MHz				150	mA
Input bus hold low sustained current 2/	I_{BHL}	V_{CC} = 4.5 V,V_{IL} = 0.8 V			+75		µA
Input bus hold high sustained current 2/	I_{BHH}	V_{CC} = 4.5 V,V_{IH} = 2.0 V			-75		µA
Input bus hold low sustained overdrive current 2/	I_{BHLO}	V_{CC} = 5.5 V				+500	µA
Input bus hold high sustained overdrive current 2/	I_{BHHO}	V_{CC} = 5.5 V				-500	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V < V_{CC} < 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance 2/	C_{IN}	See 4.4.1e, V_{IN} = 5.0 V, f = 1 MHz, T_A = 25°C	4	All		10	pF
Output capacitance 2/	C_{OUT}					12	
Dual functional pin capacitance 2/	C_{DP}					16	
Functional test		See 4.4.1c	7,8A,8B				
Input to combinatorial output 7/ 8/ 9/ 10/	t_{PD}	See figures 2 and 3 (circuit A)	9, 10, 11	01		12	ns
				02		10	
Input to output through transparent input or output latch 2/ 7/ 8/ 9/ 10/	t_{PDL}			01		17	
				02		16.5	
Input to output through transparent input and output latch 2/ 7/ 8/ 9/ 10/	t_{PDLL}			01		18	
				02		17.5	
Input to output enable see figure 3 test waveforms 2/ 7/ 8/ 9/ 10/	t_{EA}	See figures 2 and 3 (circuit B)		01		16	
				02		14	
Input to output disable see figure 3 test waveforms 2/ 7/ 8/	t_{ER}			01		16	
				02		14	
Clock or Latch enable input High time 2/ 7/	t_{WH}	See figures 2 and 3 (circuit A)		01	3		
				02	3		
Clock or latch enable input low time 2/ 7/	t_{WL}			01	3		
				02	3		
Input register or latch set-up time 2/ 7/	t_{IS}			01	2.5		
				02	2		
Input register or latch hold time 2/ 7/	t_{IH}			01	2.5		
				02	2		
Input register clock or latch enable to combinatorial output 2/ 7/ 8/ 9/ 10/	t_{ICO}			01		16	
				02		12.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V < V_{CC} < 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
Input register clock or latch enable to output through transparent output latch 2/ 6/ 7/ 8/ 9/ 10/	t_{ICOL}	See figures 2 and 3 (circuit A)	9, 10, 11	01		18	ns
				02		16	
Synchronous clock or latch enable to output 7/ 9/ 10/	t_{CO}			01		6.5	ns
				02		6.5	
Register or latch data hold time 7/	t_H			All	0		ns
Set-up time from input to synchronous clock or latch enable 7/ 8/	t_S			01	6		ns
				02	5.5		
Set-up time from input through transparent latch to output register Synchronous clock or latch enable 2/ 7/ 8/	t_{SL}			01	12		ns
				02	10		
Output Synchronous clock or latch enable to combinatorial output delay (through memory array) 2/ 7/ 8/ 9/ 10/	t_{CO2}			01		16	ns
				02		14	
Output Synchronous clock or latch enable to output synchronous clock or latch enable (through logic array) 7/ 8/	t_{SCS}			01	10		ns
				02	8		
Hold time for input through transparent latch from output register Synchronous clock or latch enable 2/ 7/	t_{HL}			All	0		ns
Maximum frequency with internal feedback (lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$) 2/ 7/	f_{MAX1}			01	100		MHz
				02	125		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V < V_{CC} < 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Maximum frequency data path in output register/latched mode (lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$) 2/ 7/	f_{MAX2}	See figures 2 and 3 (circuit A)	9, 10, 11	01	153		MHz
				02	154		
Maximum frequency with external feedback (lesser of $1/(t_{CO} + t_S)$,or $1/(t_{WL} + t_{WH})$ 2/ 7/	f_{MAX3}			01	80		
				02	83		
Maximum frequency in pipelined mode (lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$,or $1/t_{SCS}$ 2/ 7/	f_{MAX4}			01	100		
				02	118		
Input register Synchronous clock to output register clock 2/ 7/ 8/	t_{ICS}			01	10		ns
				02	8		
Asynchronous preset width 2/ 7/	t_{PW}			01	12		
				02	10		
Asynchronous preset recovery time 2/ 7/ 8/	t_{PR}			01	14		
				02	12		
Asynchronous preset to output 2/ 7/ 8/ 9/ 10/	t_{PO}			01		18	
				02		15	
Asynchronous reset width 2/ 7/	t_{RW}			01	12		
				02	10		
Asynchronous reset recovery time 2/ 7/ 8/	t_{RR}			01	14		
				02	12		
Asynchronous reset to output 2/ 7/ 8/ 9/ 10/	t_{RO}			01		18	
				02		15	
Product term clock or latch enable (PTCLK) to output 2/ 7/ 8/ 9/ 10/	t_{COPT}			All		13	
Register or latch data hold time 2/ 7/	t_{HPT}			01	5.5		
				02	5.0		
Set-up time from input to product term clock or latch enable (PTCLK) 2/ 7/	t_{SPT}			01	5.5		
				02	5.0		
Set-up time for buried register used as an input register from input to product term clock or latch enable (PTCLK) 2/ 7/ 8/	t_{ISPT}			All	0		

See footnotes at the end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V < V_{CC} < 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Buried register used as an input register or latch data hold time 2/ 7/	t_{IHPT}	See figures 2 and 3 (circuit A)	9, 10, 11	01	11		ns
				02	9		
Product term clock or latch enable (PTCLK) to output delay (through logic array) 2/ 7/ 8/ 9/ 10/	t_{CO2PT}			01		21	
				02		19	
Low power adder 2/ 7/	t_{LP}			All		2.5	
Slow output slew rate adder 2/ 7/	t_{SLEW}			All		3.0	
3.3 V I/O mode timing adder 2/ 7/	$t_{3.3IO}$			All		0.3	
Set-up time from TDI and TMS to TCK 2/ 7/	$t_{S\ JTAG}$			All	0		
Hold time on TDI and TMS 2/ 7/	$t_{H\ JTAG}$			All	20		
Falling edge of TCK to TDO 2/ 7/	$t_{CO\ JTAG}$			All		20	
Maximum JTAG tap controller frequency 2/ 7/	f_{JTAG}			All		20	MHz

1/ I_{OH} = -2 mA, I_{OL} = +2 mA for TDO.

2/ Tested initially and after any design or process changes that affect this parameter.

3/ When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to a maximum of 3.6 V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are output disabled during ISR programming. Contact manufacturer for additional information.

4/ These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

5/ Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

6/ Measured under AC conditions. Program pattern using 16-bit counter per logic block or equivalent.

7/ All AC parameters are measured with 2 outputs switching, and 35 pF AC test load, unless otherwise specified.

8/ Logic blocks operating in low power mode, add t_{LP} to this spec.

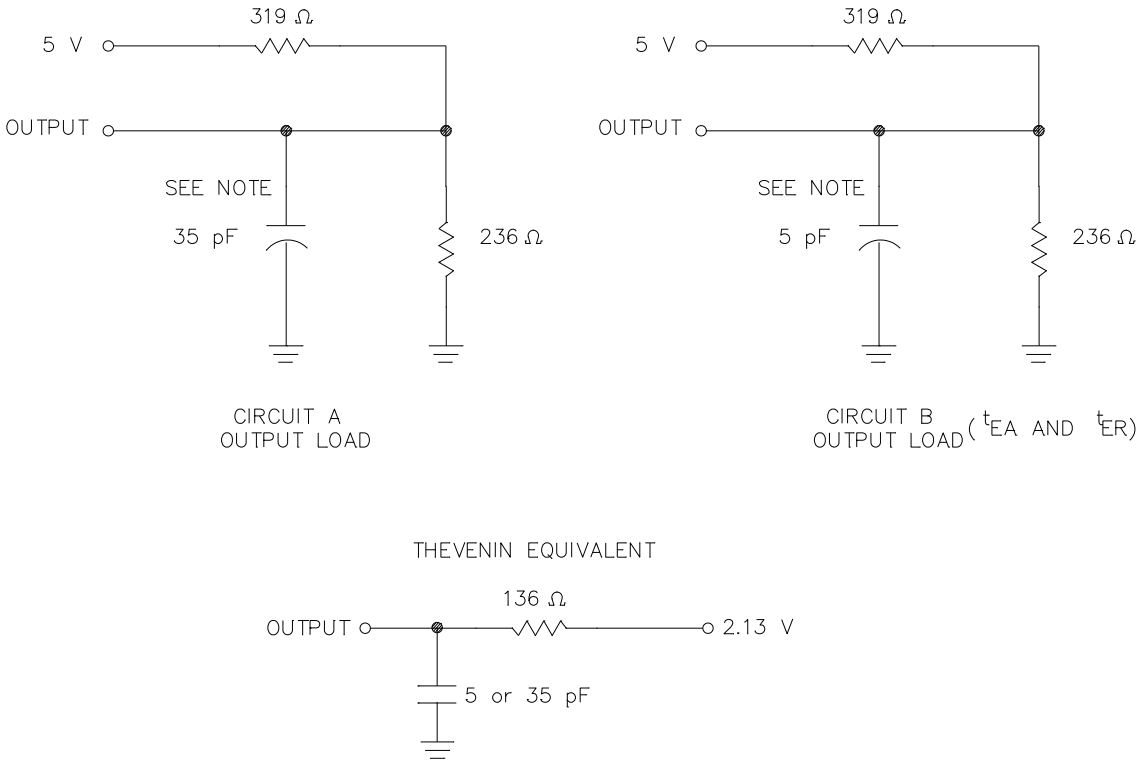
9/ Outputs using slow output slew rate, add t_{SLEW} to this spec.

10/ When V_{CCO} = 3.3 V add $t_{3.3IO}$ to this spec.

Case outline Y

Device Type	All		Device Type	All		Device Type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	GND		29	I/O		57	I/O
2	V_{CCO}		30	I/O		58	I/O
3	I/O		31	I/O		59	I/O
4	I/O		32	GND		60	I/O
5	I/O		33	I/O		61	I/O
6	I/O		34	I/O		62	CLK/I
7	I/O		35	I/O/TMS		63	V_{CCO}
8	I/O		36	I/O		64	GND
9	I/O		37	I/O		65	CLK/I
10	I/O		38	I/O		66	I/O
11	GND		39	I/O		67	I/O
12	I/O		40	I/O		68	I/O
13	I/O		41	I		69	I/O
14	I/O/TCK		42	V_{CCO}		70	I/O
15	I/O		43	GND		71	I/O
16	I/O		44	V_{CC}		72	I/O/TDI
17	I/O		45	I/O		73	I/O
18	I/O		46	I/O		74	GND
19	I/O		47	I/O		75	I/O
20	CLK/I		48	I/O		76	I/O
21	V_{CCO}		49	I/O		77	I/O
22	GND		50	I/O		78	I/O
23	CLK/I		51	I/O/TDO		79	I/O
24	I/O		52	I/O		80	I/O
25	I/O		53	GND		81	I/O
26	I/O		54	I/O		82	I/O
27	I/O		55	I/O		83	$JTAG_{EN}$
28	I/O		56	I/O		84	V_{CC}

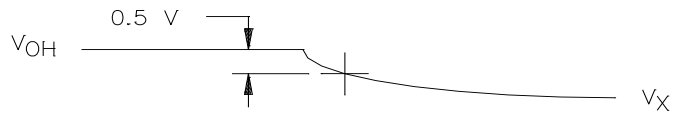
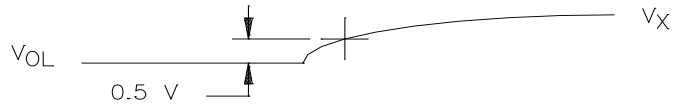
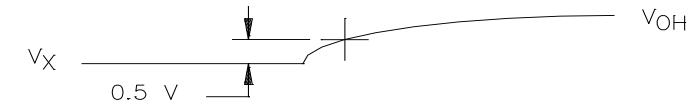
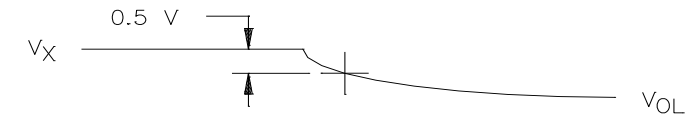
FIGURE 1. Terminal connections.



NOTE: INCLUDING SCOPE AND JIG (MINIMUM VALUES).

FIGURE 2. Output load circuits and test conditions.

TEST WAVEFORMS

PARAMETER	V_X	OUTPUT WAVEFORM - MEASUREMENT LEVEL
$t_{ER(-)}$	1.5 V	
$t_{ER(+)}$	2.6 V	
$t_{EA(+)}$	1.5 V	
$t_{EA(-)}$	V_{thc}	

INPUT PULSES

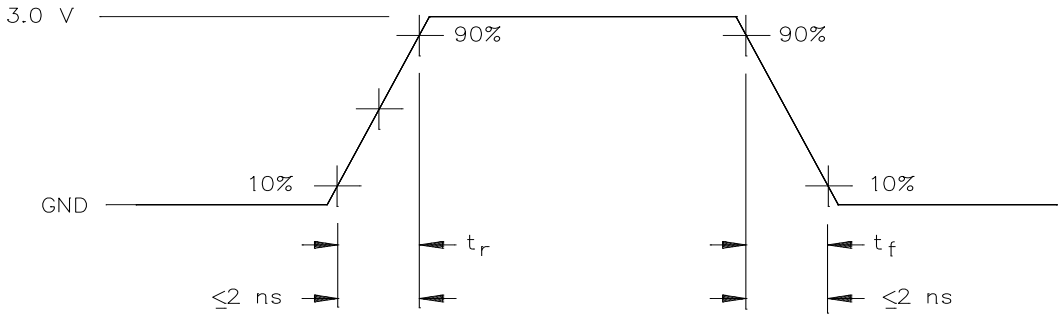


FIGURE 2. Output load circuits and test conditions – Continued.

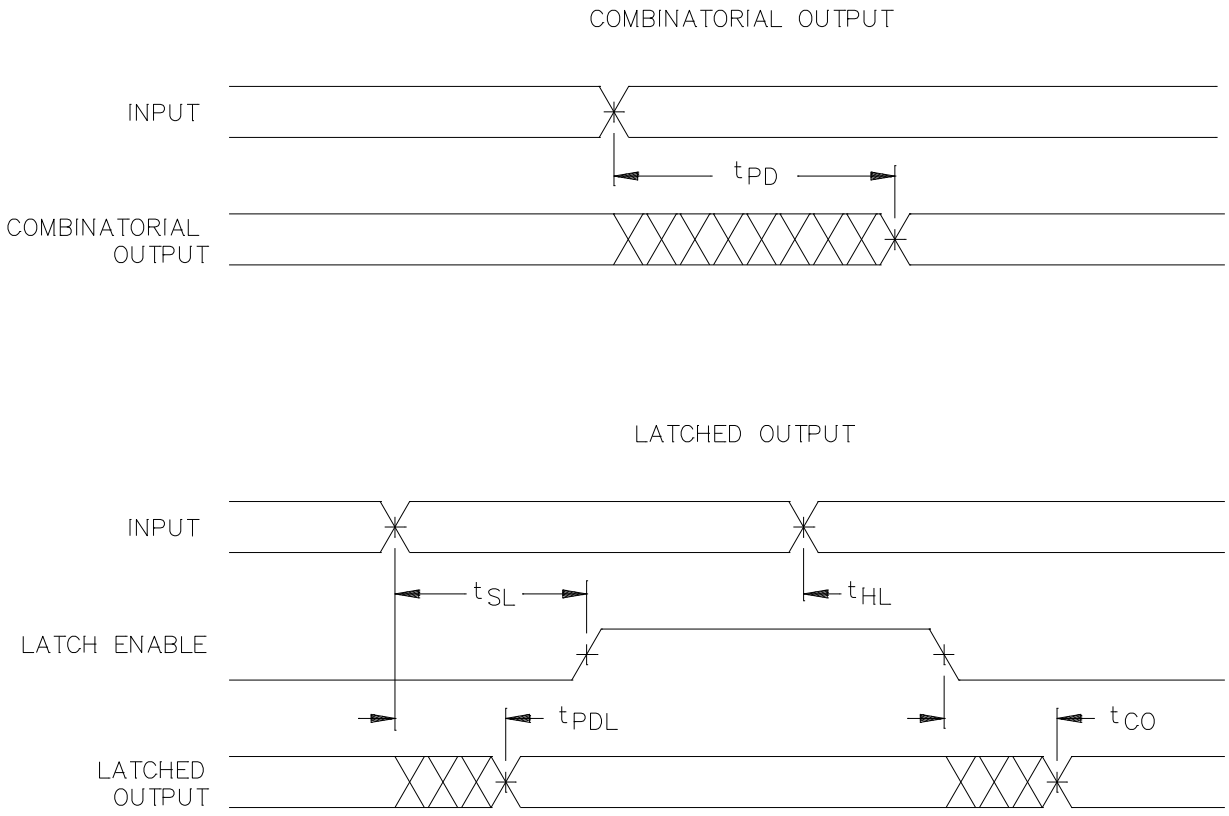


FIGURE 3. Switching waveforms.

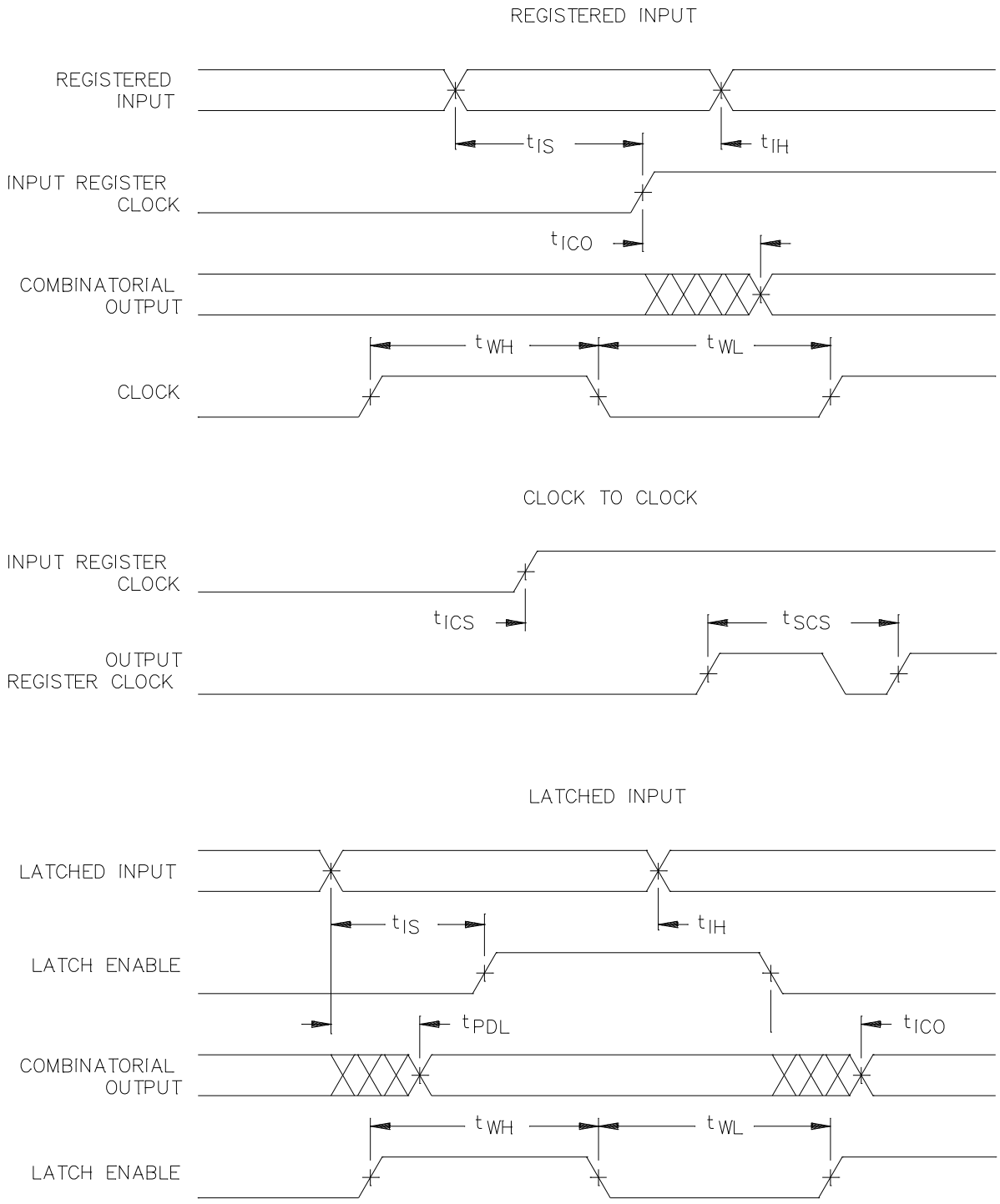


FIGURE 3. Switching waveforms – Continued.

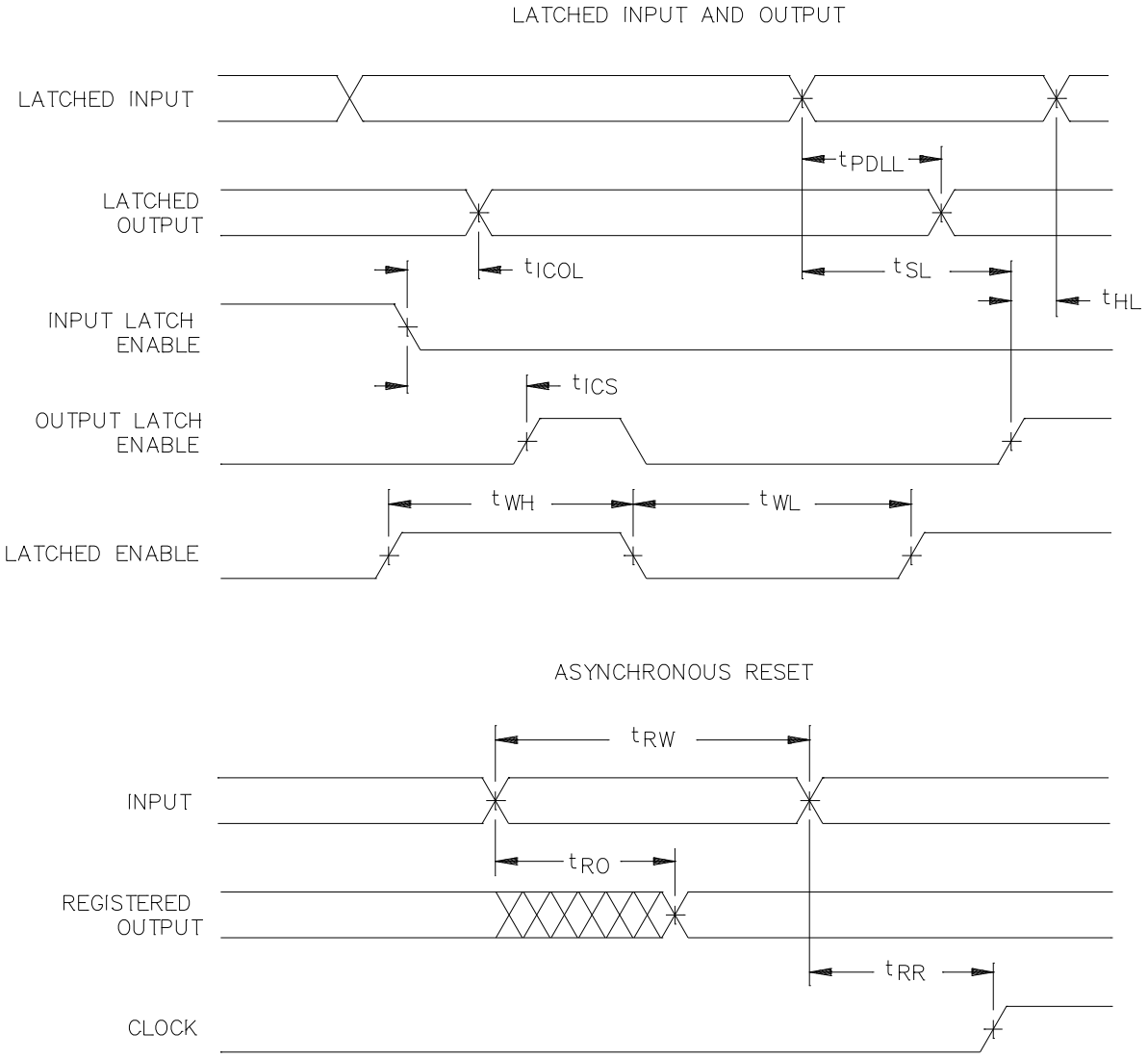


FIGURE 3. Switching waveforms – Continued.

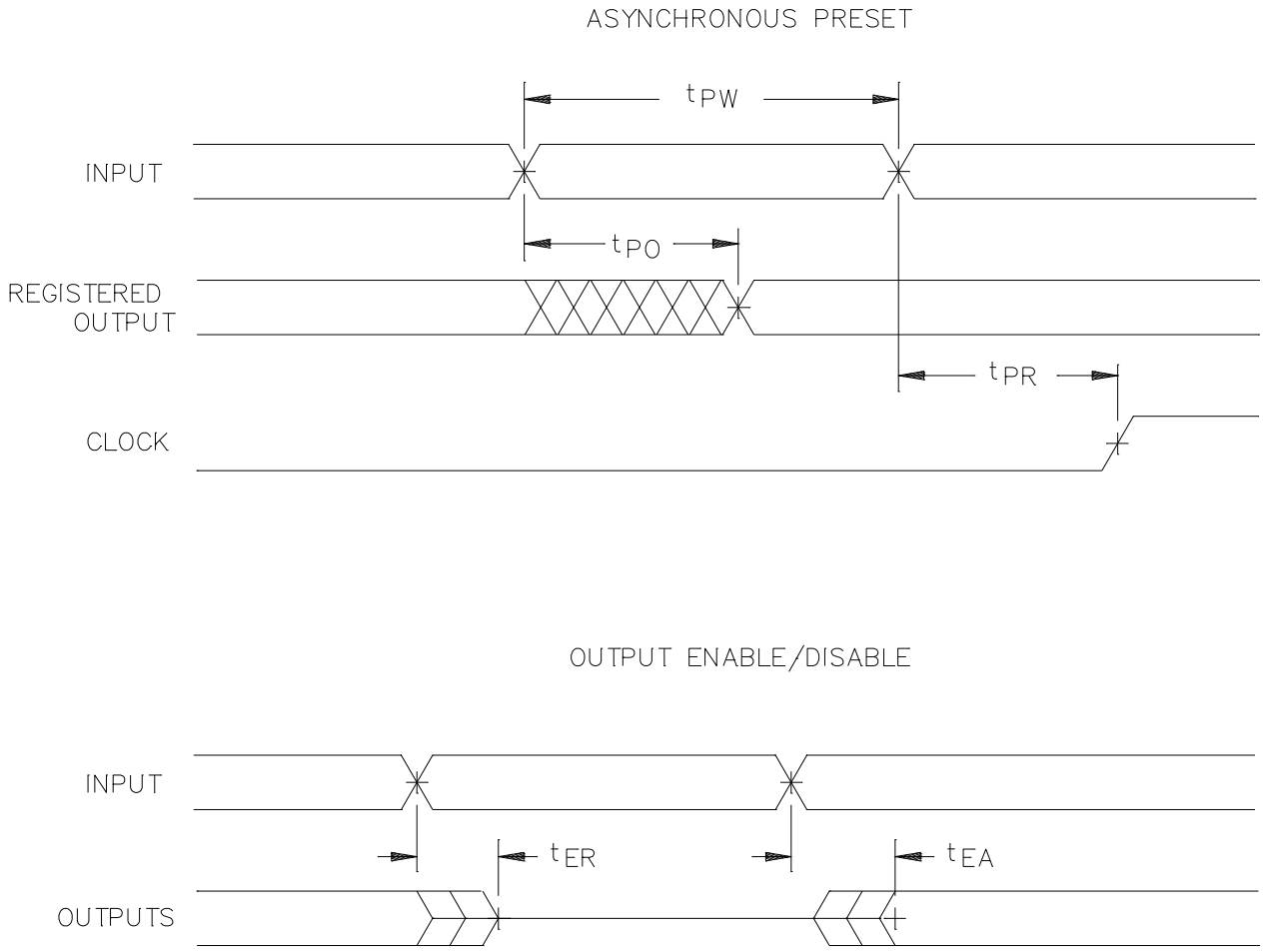


FIGURE 3. Switching waveforms – Continued.

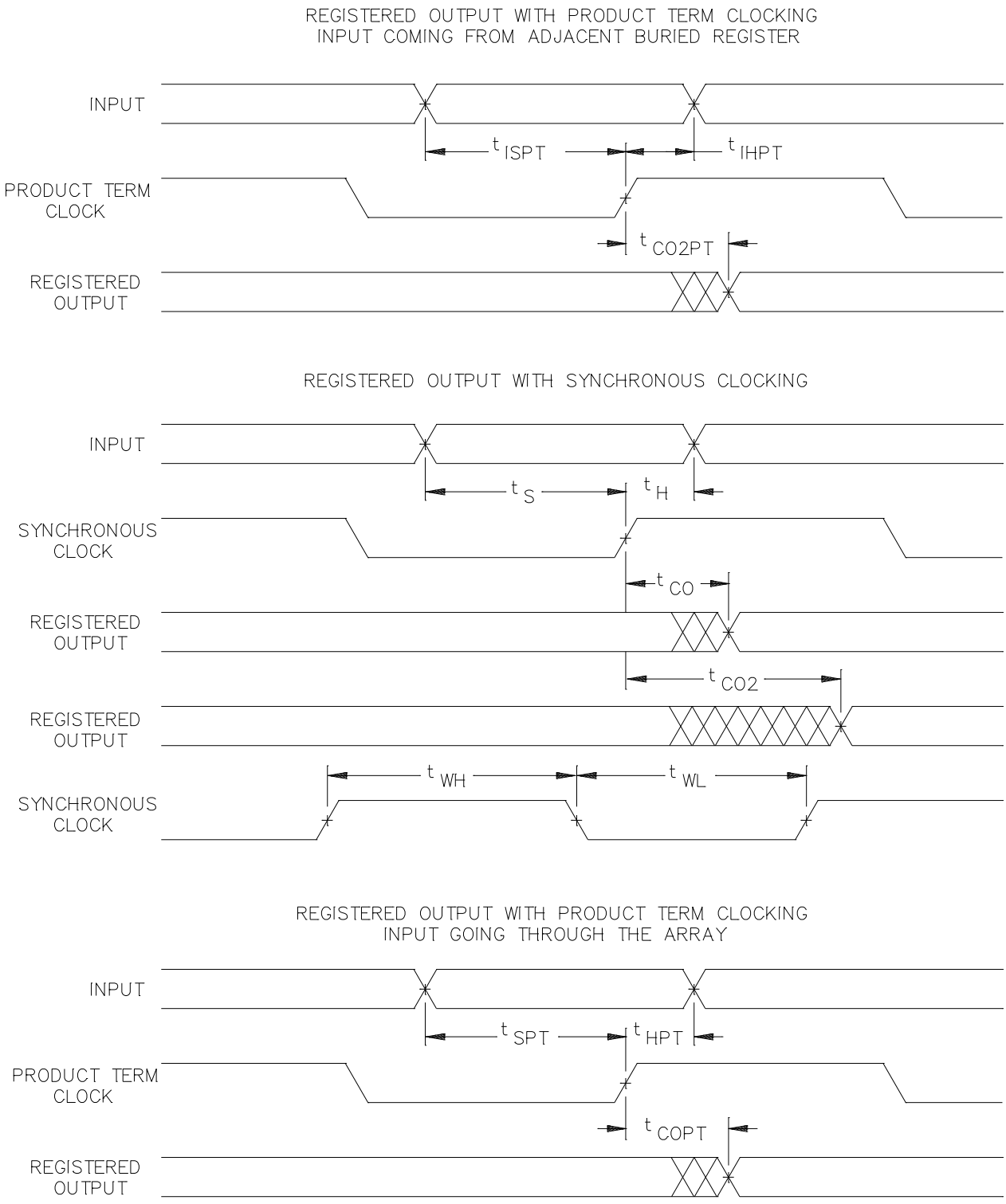
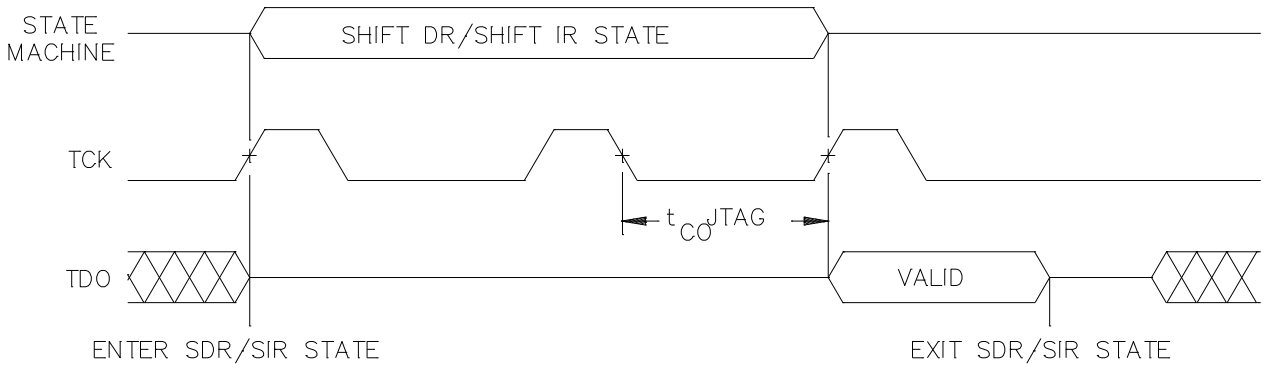


FIGURE 3. Switching waveforms – Continued.

JTAG TDO VALID DELAY TIMING DIAGRAM



JTAG TMS/TDI SETUP AND HOLD DIAGRAMS

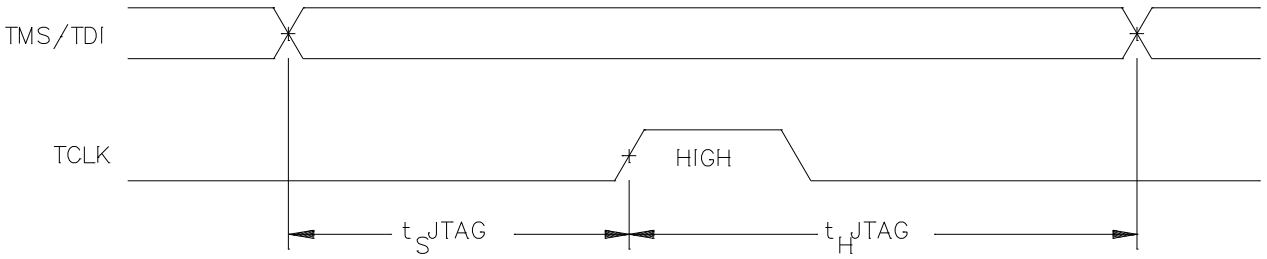


FIGURE 3. Switching waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V subgroups 7, 8A and 8B shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC JESD78 may be used for reference.

e. Subgroup 4 (C_{IN}, C_{OUT} , and C_{DP} measurements) shall be measured only for initial qualification and after any process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is three devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III	
		Device Class Q	Device Class V
1	Interim electrical parameters (see 4.2)		1, 7, 9 or 2, 8A, 10
2	Static burn-in (Method 1015)	Not Required	Required
3	Same as line 1		1*, 7* Δ
4	Dynamic burn-in (Method 1015)	Required	Required
5	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
6	Group A test requirements	1*,2,3,4**,7, 8A,8B,9,10, 11	1*,2,3,4**,7, 8A,8B,9,10, 11
7	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
8	Group D end-point Electrical Parameters	2,3, 8A,8B	2,3, 8A,8B
9	Group E end-point electrical parameters	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{OZ}	± 10% of the specified value in table I
I_{IX}	± 10% of the specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25ºC ±5ºC, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Erasure procedures. Erasure procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-04-10

Approved sources of supply for SMD 5962-99521 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9952101QYA	0C7V7 65786	CY37128P84-100YMB CY37128P84-100YMB
5962-9952102QYA	0C7V7	CY37128P84-125YMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	e2v aerospace and defense, inc. dba QP Semiconductor, Inc. 765 Sycamore Drive Milpitas, CA 95035
65786	Cypress Semiconductor 198 Champion Court San Jose, CA 95134-1709

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.