

## N-channel Enhancement Mode Power MOSFET

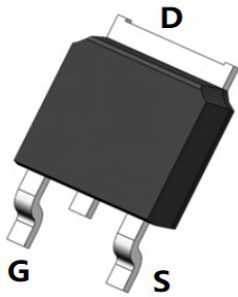
### Features

- $V_{DS} = 60V$ ,  $I_D = 30A$   
 $R_{DS(ON)} < 27\ m\Omega$  @  $V_{GS} = 10V$   
 $R_{DS(ON)} < 33\ m\Omega$  @  $V_{GS} = 4.5V$

### General Features

- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free and Green Available

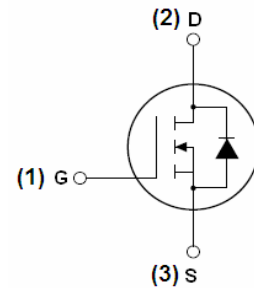
100% UIS TESTED!  
 100%  $\Delta V_{ds}$  TESTED!



TO-252-2L Top View



Pin Assignment



Schematic Diagram

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	30	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	20	A
Pulsed Drain Current	$I_{DM}$	74	A
Maximum Power Dissipation	$P_D$	50	W
Derating factor		0.33	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	144	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	3	$^\circ C/W$
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**Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		3.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	27		mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	-	30	-	S
<b>Dynamic Characteristics</b> (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, F=1.0MHz	-	1900	-	PF
Output Capacitance	C <sub>OSS</sub>		-	130	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	95	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> =30V, R <sub>L</sub> =1.5Ω V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω	-	5	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	2.6	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	16.1	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	2.3	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	30		nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.5		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	7.5		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-		1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	30	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =20A di/dt = 100A/μs (Note3)	-	35	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	53	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, L=0.5mH, R<sub>g</sub>=25Ω

Typical Electrical and Thermal Characteristics (Curves)

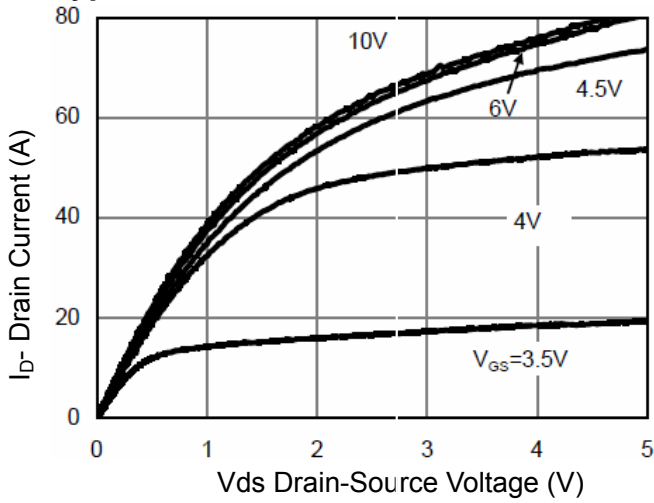


Figure 1 Output Characteristics

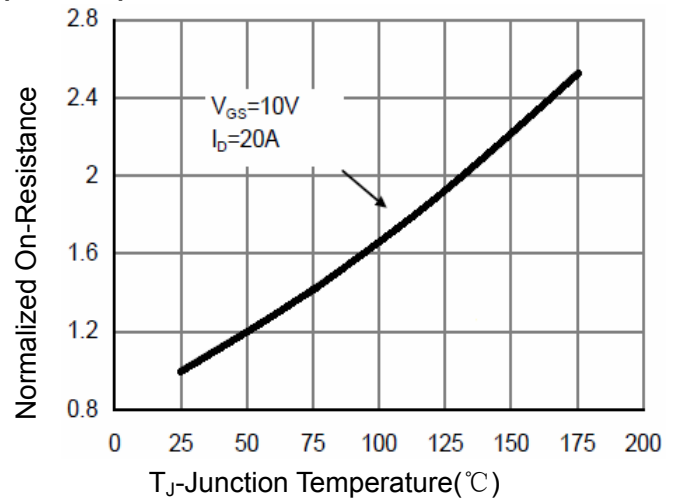


Figure 4  $R_{ds(on)}$ -Junction Temperature

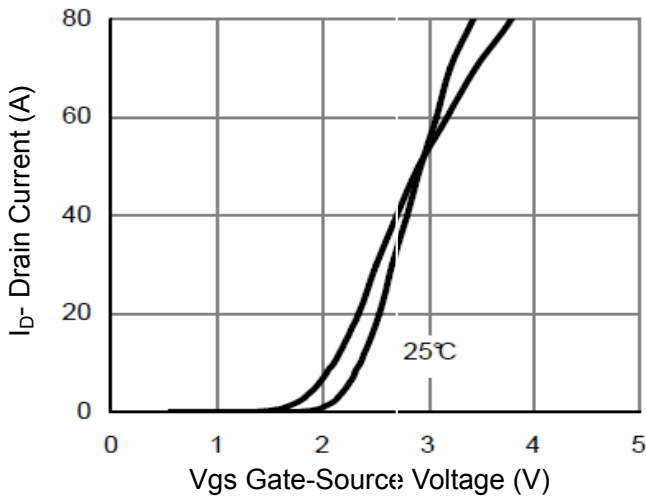


Figure 2 Transfer Characteristics

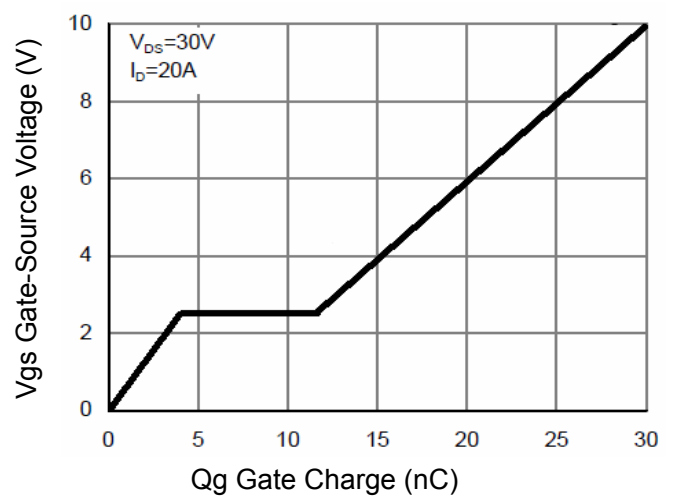


Figure 5 Gate Charge

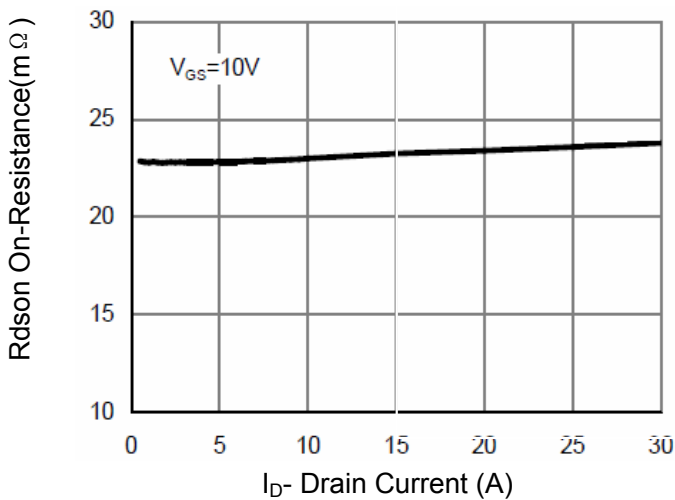


Figure 3  $R_{ds(on)}$ - Drain Current

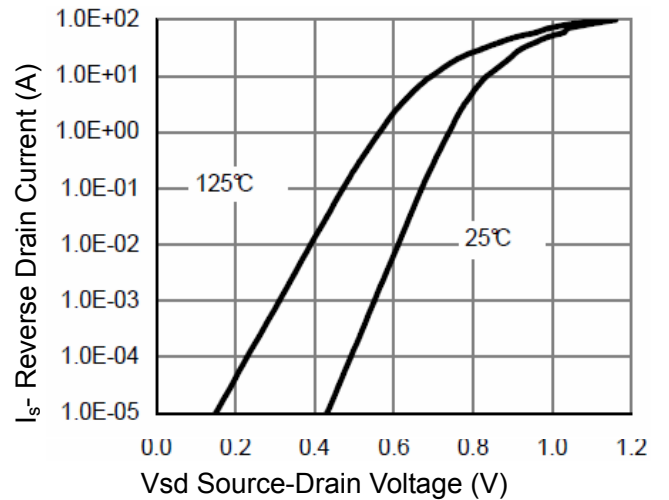


Figure 6 Source- Drain Diode Forward

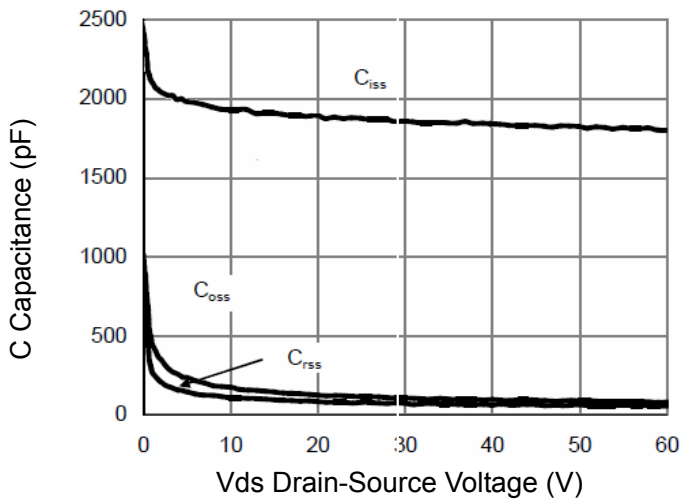


Figure 7 Capacitance vs Vds

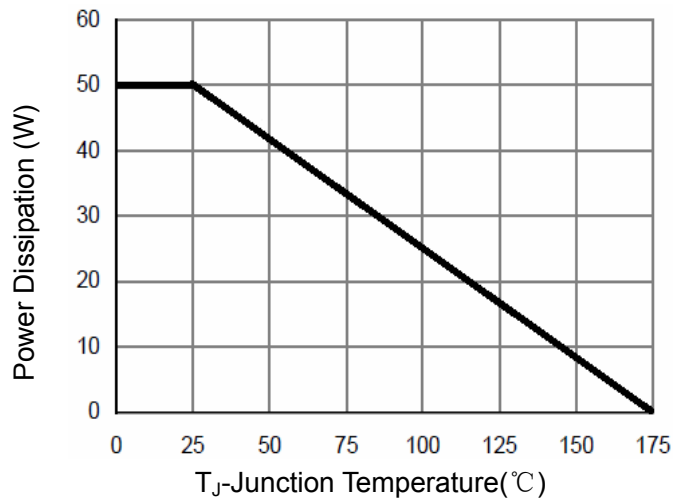


Figure 9 Power De-rating

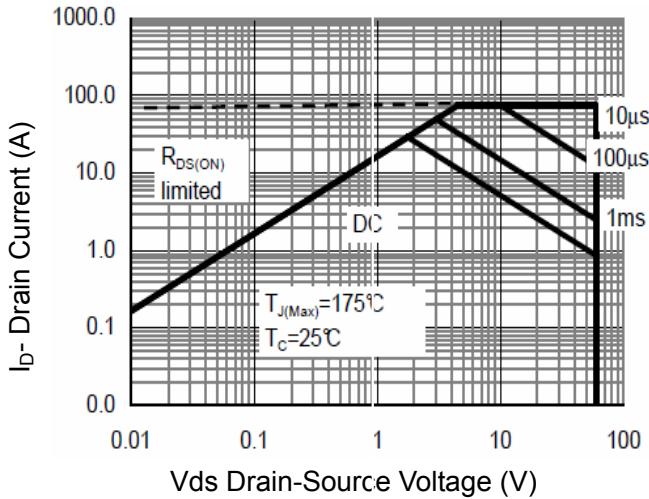


Figure 8 Safe Operation Area

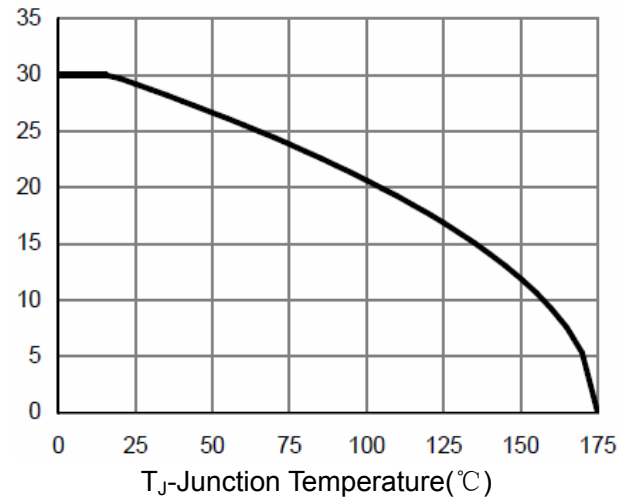


Figure 10  $V_{GS(th)}$  vs Junction Temperature

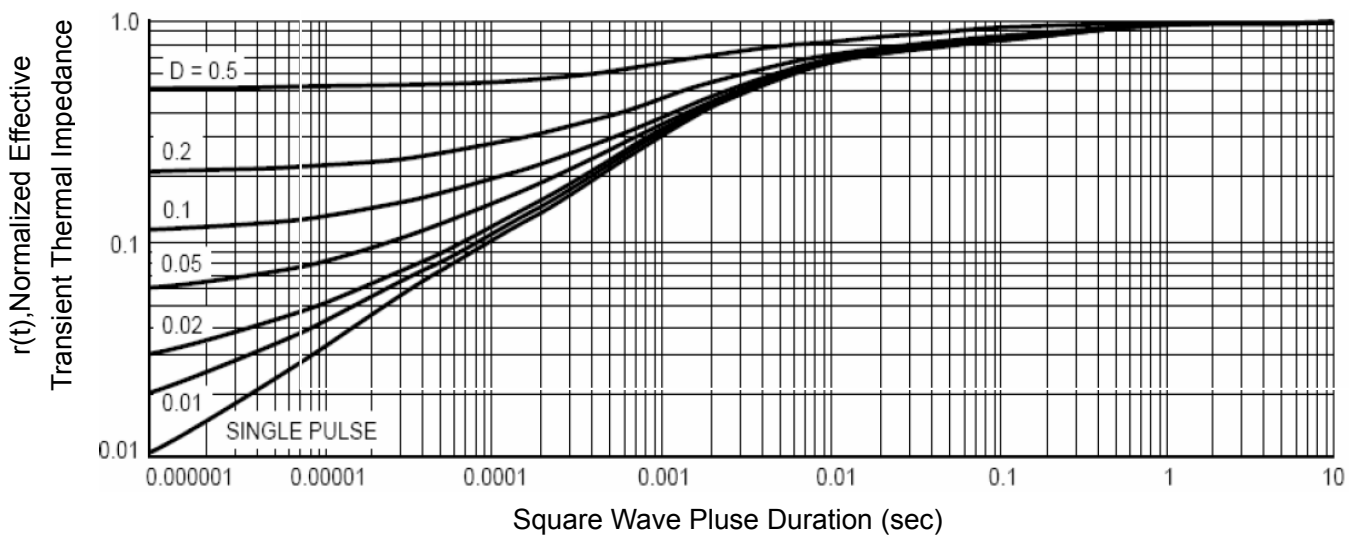


Figure 11 Normalized Maximum Transient Thermal Impedance