CT455

XtremeSense™ TMR Coreless Current Sensor with 1 MHz Bandwidth and Programmable Gain

FEATURES AND BENEFITS

- User-programmable field range:
  - 6 to 8 mT
  - 12 to 48 mT
- Preset magnetic field ranges:
  - ±6 mT
  - ±48 mT
- AEC-Q100 Grade 1 [1] automotive qualified (A variants only)
- Optimized for high dV/dt applications
- Linear analog output voltage
- 1 MHz bandwidth
- Response time: < 300 ns
- Supply voltage: 3.3 or 5 V
- Low-noise performance
- Package options:
  - 8-lead SOIC
  - 8-lead TSSOP

APPLICATIONS

- Solar/power inverters
- Battery management systems
- Industrial equipment
- Power utility meters
- Power conditioner
- DC-DC converters

DESCRIPTION

The CT455 is a high-bandwidth and low-noise integrated contactless current sensor that uses Allegro patented XtremeSense tunnel magnetoresistance (TMR) technology to enable high-accuracy current measurements for many consumer, enterprise, and industrial applications. The device supports two standard field ranges where the CT455 senses and translates the magnetic field into a linear analog output voltage.

The CT455 is also available in a user-programmable variant, which enables end-of-line calibration of gain and offset. While the sensor is preprogrammed to compensate for gain and offset temperature drift, the ability to adjust offset and gain relaxes mechanical tolerances during sensor mounting.

The device has less than 300 ns output response time while the current consumption is ~6 mA.

The CT455 is assembled in two package options—an eight-lead small-outline integrated-circuit (SOIC) package and a low-profile, industry-standard eight-lead thin-shrink small-outline package (TSSOP). Both are green and RoHS compliant.

PACKAGES:

8-lead SOIC

8-lead TSSOP

Not to scale

FUNCTIONAL BLOCK DIAGRAMS

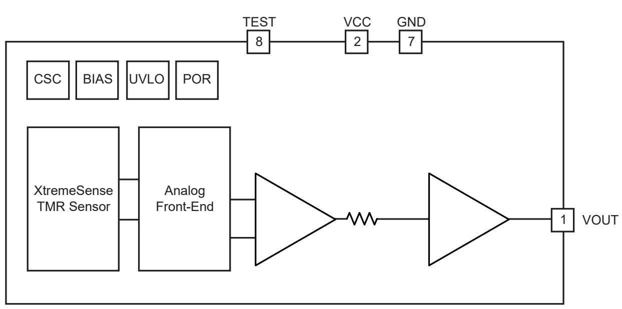

Figure 1: CT455 Functional Block Diagram for TSSOP-8

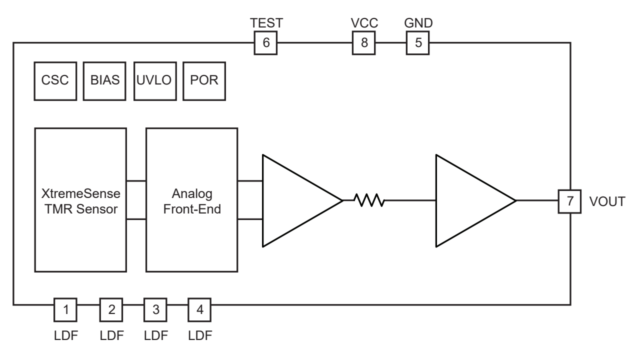

Figure 2: CT455 Functional Block Diagram for SOIC-8

[1] For more details, see the Testing and Quality Assurance section.

Table of Contents

SELECTION GUIDE

Part Number	Qualification	Polarity	Range (mT)	Supply Voltage (V)	Operating Temperature Range (°C)	Package
FACTORY-CALIBRATED SENSORS						
CT455-A06B5-TS08	AEC-Q100 Grade 1	Bipolar	±6	5	–40 to 125	8-lead TSSOP 3 mm × 6.4 mm × 1.1 mm
CT455-H06B5-TS08	–					
CT455-A48B5-TS08	AEC-Q100 Grade 1	Bipolar	±48			
CT455-H48B5-TS08	–					
PROGRAMMABLE SENSORS						
CT455-A00B3-TS08	AEC-Q100 Grade 1	Bipolar	±6 to ±8 and ±12 to ±48	3.3	–40 to 125	8-lead TSSOP 3 mm × 6.4 mm × 1.1 mm
CT455-H00B3-TS08	–					
CT455-A00B5-TS08	AEC-Q100 Grade 1	Bipolar	±6 to ±8 and ±12 to ±48	5		
CT455-H00B5-TS08	–					
CT455-A00U5-TS08	AEC-Q100 Grade 1	Unipolar				
CT455-H00U5-TS08	–					
CT455-A00B5-SN08	AEC-Q100 Grade 1	Bipolar	±6 to ±8 and ±12 to ±48	5	–40 to 125	8-lead SOIC 4.89 mm × 6 mm × 1.62 mm
CT455-H00B5-SN08	–					

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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		–0.3 to 6	V
Analog Input/Output Pins, Maximum Voltage	$V_{I/O}$		–0.3 to (V_{CC} + 0.3) [2]	V
Electrostatic Discharge Protection Level	ESD	Human Body Model (HBM) per JESD22-A114	±2 (min)	kV
		Charged Device Model (CDM) per JESD22-C101	±0.5 (min)	kV
Junction Temperature	T_J		–40 to 150	°C
Storage Temperature	T_{STG}		–65 to 155	°C
Lead Soldering Temperature	T_L	10 seconds	260	°C

[1] Stresses exceeding the absolute maximum ratings may damage the CT455: The CT455 may not function or be operable at levels that exceed the recommended operating conditions, and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses that exceed the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

[2] The lower of (V_{CC} + 0.3 V) or 6 V.

RECOMMENDED OPERATING CONDITIONS [1]

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Supply Voltage Range	V_{CC}	5 V_{CC} variant (-x5)	4.75	5	5.5	V
		3.3 V_{CC} variant (-x3)	3	3.3	3.6	V
Output Voltage Range	V_{OUT}		0	–	V_{CC}	V
Output Current	I_{OUT}		–	–	±1	mA
Operating Ambient Temperature	T_A	Extended Industrial	–40	25	125	°C

[1] The Recommended Operating Conditions table defines the conditions for actual operation of the CT455. Recommended operating conditions are specified to ensure optimal performance to the specifications. Allegro does not recommend exceeding them or designing to absolute maximum ratings.

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APPLICATION DIAGRAMS

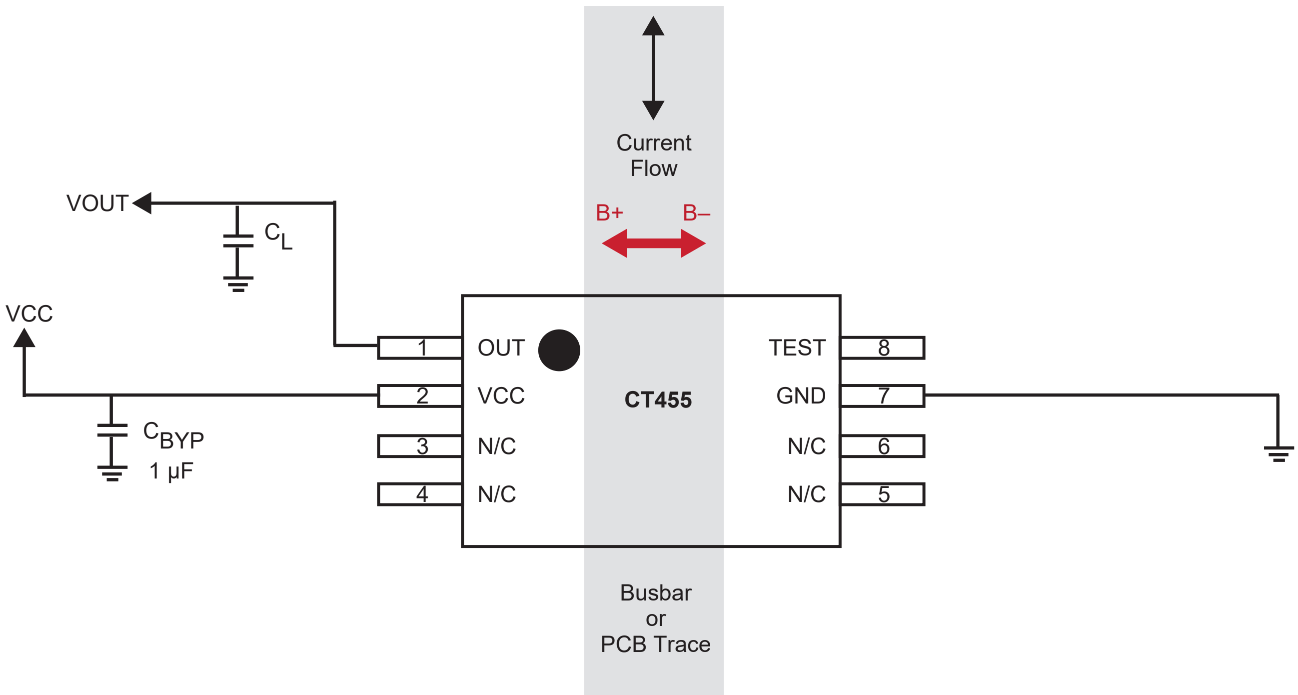

Figure 3: CT455 Application Diagram for Measuring Uniform Magnetic Field for TSSOP-8

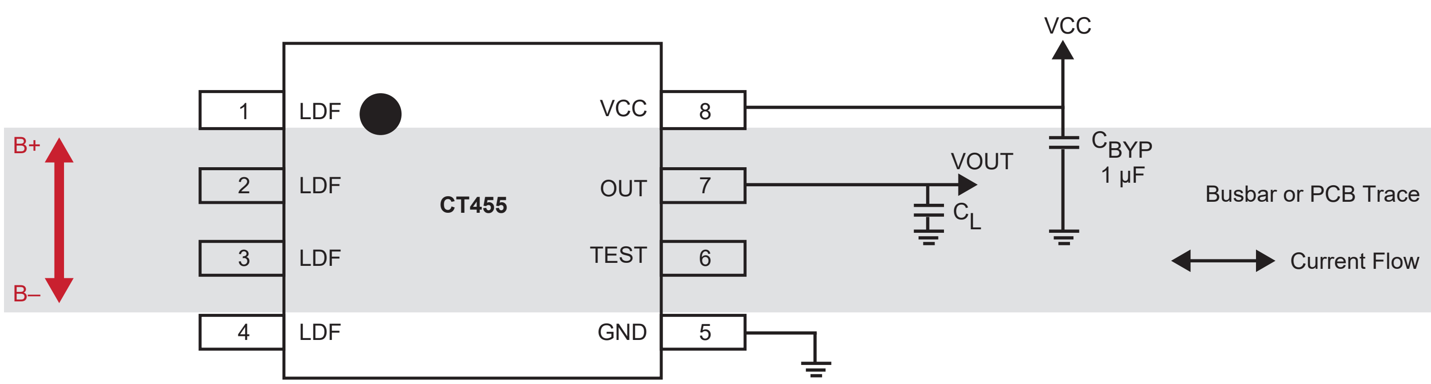

Figure 4: CT455 Application Diagram for SOIC-8

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PINOUT DIAGRAMS AND TERMINAL LISTS

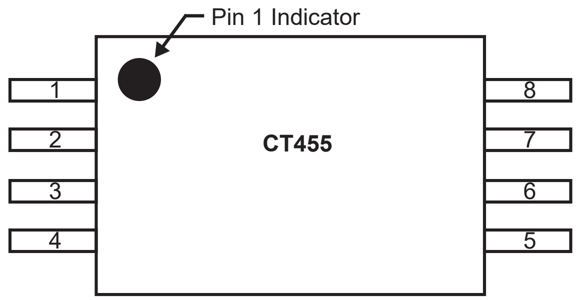

Figure 5: CT455 Pinout Diagram for Eight-Lead TSSOP (Top-Down View)

Terminal List

Number	Name	Function
1	OUT	Analog output voltage that represents the measured current/field.
2	VCC	Supply voltage.
3, 4, 5, 6	NC	No connect (leave floating).
7	GND	Ground.
8	TEST	Pin used for calibration. Connect to ground if not used.

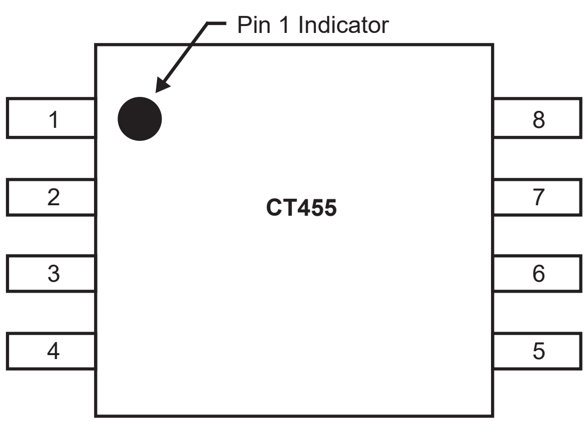

Figure 6: CT455 Pinout Diagram for Eight-Lead SOIC Package (Top-Down View)

Terminal List

Number	Name	Function
1, 2, 3, 4	LDF	Leadframe pin—A single (1) LDF pin should be connected to GND. The other three (3) LDF pins should remain unconnected to avoid ground loops through the leadframe.
5	GND	Ground.
6	TEST	Pin used for calibration. Connect to ground if not used.
7	OUT	Analog output voltage that represents the measured current/field.
8	VCC	Supply voltage.

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ELECTRICAL CHARACTERISTICS: V_{CC} = 3 to 3.6 V or 4.75 to 5.5 V, T_A = –40°C to 125°C, C_{BYP} = 1 µF, unless otherwise specified; typical values are V_{CC} = 3.3 or 5 V and T_A = 25°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
Supply Current	I_{CC}	f_{BW} = 1 MHz, no load, B_{OP} = 0 mT	–	6	9	mA
OUT Maximum Drive Capability	I_{OUT}	OUT covers 10% to 90% of V_{CC} span	–1	–	1	mA
OUT Capacitive Load	C_L		–	–	100	pF
OUT Resistive Load	R_L		–	100	–	kΩ
Power Supply Rejection Ratio [1]	PSRR		–	35	–	dB
Sensitivity Power Supply Rejection Ratio [1]	SPSRR		–	35	–	dB
Offset Power Supply Rejection Ratio [1]	OPSRR		–	40	–	dB
Bandwidth [1]	f_{BW}	Small signal = –3 dB	–	1	–	MHz
ANALOG OUTPUT (OUT)						
OUT Voltage Linear Range	V_{OUT}	5 V_{CC} variant (-x5)	0.5	–	4.5	V
		3.3 V_{CC} variant (-x3)	0.65	–	2.65	V
Output High Saturation Voltage	V_{OUT_SAT}	T_A = 25°C	V_{CC} – 0.3	V_{CC} – 0.25	–	V
TIMINGS						
Power-On Time	t_{ON}	V_{CC} ≥ 4 V variant (-x5), V_{CC} ≥ 2.5 V variant (-x3)	–	100	200	µs
Rise Time [1]	t_{RISE}	B_{OP} = $B_{RNG(MAX)}$, T_A = 25°C, C_L = 100 pF	–	200	–	ns
Response Time [1]	$t_{RESPONSE}$	B_{OP} = $B_{RNG(MAX)}$, T_A = 25°C, C_L = 100 pF	–	300	–	ns
Propagation Delay [1]	t_{DELAY}	B_{OP} = $B_{RNG(MAX)}$, T_A = 25°C, C_L = 100 pF	–	250	–	ns
PROTECTION						
Undervoltage Lockout	V_{UVLO}	Rising V_{CC}	–	2.5	–	V
		Falling V_{CC}	–	2.45	–	V
UVLO Hysteresis	V_{UV_HYS}		–	50	–	mV

[1] Guaranteed by design and characterization; not tested in production.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3 or 5 V, T_A = 25°C, and C_{BYP} = 1 µF (unless otherwise specified)

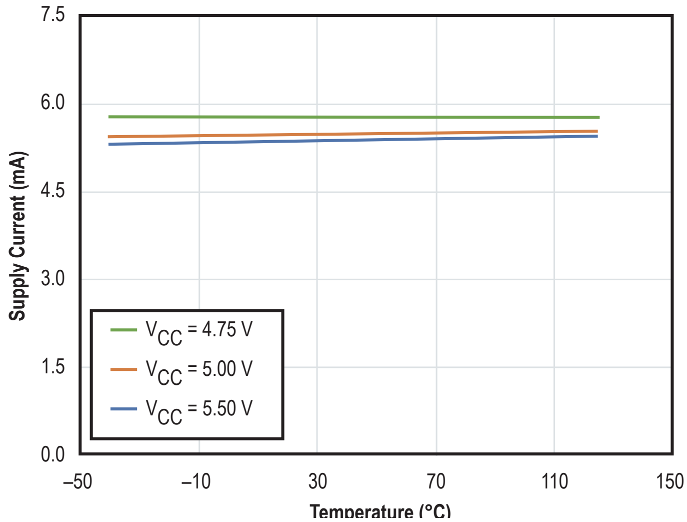

Figure 7: 5 V_{CC} Variant (-x5)
Supply Current vs. Temperature vs. Supply Voltage

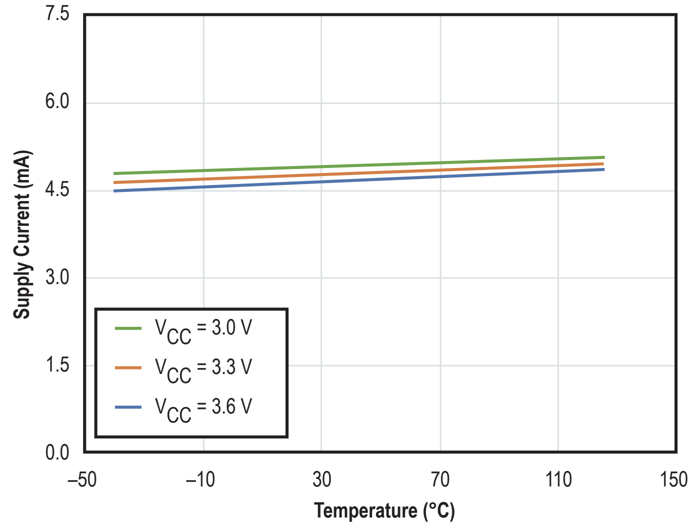

Figure 8: 3.3 V_{CC} Variant (-x3)
Supply Current vs. Temperature vs. Supply Voltage

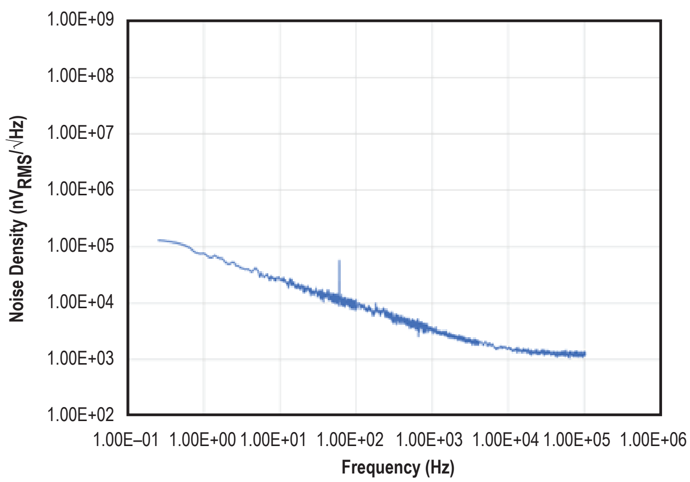

Figure 9: Noise Density vs. Frequency

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CT455-x06B5: ±6 mT – ELECTRICAL CHARACTERISTICS: [1][2] V_{CC} = 4.75 to 5.5 V, T_A = –40°C to 125°C, C_{BYP} = 1 µF, unless otherwise specified; typical values are V_{CC} = 5 V and T_A = 25°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Magnetic Field Range	B_{RNG}		–6	–	6	mT
Voltage Output Quiescent	V_{OQ}			2.5		V
Sensitivity	S		–	333.3	–	mV/mT
Bandwidth [3]	f_{BW}	Small signal = –3 dB	–	1	–	MHz
Noise	e_N	T_A = 25°C, f_{BW} = 100 kHz	–	2.77	–	μT_{RMS}
OUT ACCURACY PERFORMANCE						
Linearity Error	E_{LIN}	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±0.1	–	% FS
Sensitivity Temperature Drift	E_{SENS_Tdrift}	B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to 125°C	–	±1.4	–	%
		B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to –40°C	–	±1.6	–	%
Offset Voltage Error	V_{OE}	B_{OP} = 0 mT, T_A = 25°C	–	±4	–	mV
Offset Voltage Temperature Drift	V_{OE_Tdrift}	B_{OP} = 0 mT, T_A = 25°C to 125°C	–	±15	–	mV
		B_{OP} = 0 mT, T_A = 25°C to –40°C	–	±26	–	mV
LIFETIME DRIFT						
Sensitivity Error Including Lifetime Drift	$E_{SENS(DRIFT)}$	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±3	–	%
Offset Voltage Error Including Lifetime Drift	$V_{OE(DRIFT)}$	B_{OP} = 0 mT, T_A = –40°C to 125°C	–	±34	–	mV

[1] Typical (typ) values are the mean ±3 sigma of a test sample population. These are formatted as mean ±3 sigma.
[2] Lifetime drift characteristics are based on a statistical combination of production distributions and the worst-case distribution of parametric drift of individuals observed during AEC-Q100 qualification.
[3] Guaranteed by design and characterization. Not tested in production.

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CT455-x48B5: ±48 mT – ELECTRICAL CHARACTERISTICS: [1][2] V_{CC} = 4.75 to 5.5 V, T_A = –40°C to 125°C, C_{BYP} = 1 µF, unless otherwise specified; typical values are V_{CC} = 5 V and T_A = 25°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Magnetic Field Range	B_{RNG}		–48	–	48	mT
Voltage Output Quiescent	V_{OQ}			2.5		V
Sensitivity	S		–	41.7	–	mV/mT
Bandwidth [3]	f_{BW}	Small signal = –3 dB	–	1	–	MHz
Noise	e_N	T_A = 25°C, f_{BW} = 100 kHz	–	6.44	–	μT_{RMS}
OUT ACCURACY PERFORMANCE						
Linearity Error	E_{LIN}	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±0.3	–	% FS
Sensitivity Temperature Drift	E_{SENS_Tdrift}	B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to 125°C	–	±1.4	–	%
		B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to –40°C	–	±2.2	–	%
Offset Voltage Error	V_{OE}	B_{OP} = 0 mT, T_A = 25°C	–	±4	–	mV
Offset Voltage Temperature Drift	V_{OE_Tdrift}	B_{OP} = 0 mT, T_A = 25°C to 125°C	–	±15	–	mV
		B_{OP} = 0 mT, T_A = 25°C to –40°C	–	±26	–	mV
LIFETIME DRIFT						
Sensitivity Error Including Lifetime Drift	$E_{SENS(DRIFT)}$	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±3	–	%
Offset Voltage Error Including Lifetime Drift	$V_{OE(DRIFT)}$	B_{OP} = 0 mT, T_A = –40°C to 125°C	–	±34	–	mV

[1] Typical (typ) values are the mean ±3 sigma of a test sample population. These are formatted as mean ±3 sigma.
[2] Lifetime drift characteristics are based on a statistical combination of production distributions and the worst-case distribution of parametric drift of individuals observed during AEC-Q100 qualification.
[3] Guaranteed by design and characterization. Not tested in production.

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CT455-x00B5: Programmable Gain – ELECTRICAL CHARACTERISTICS: [1][2][3] V_{CC} = 4.75 to 5.5 V, T_A = –40°C to 125°C, C_{BYP} = 1 µF, unless otherwise specified; typical values are V_{CC} = 5 V and T_A = 25°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Programmable Magnetic Field Range	B_{PRNG}		±6	–	±8	mT
			±12	–	±48	mT
Voltage Output Quiescent	V_{OQ}		–	2.5	–	V
Maximum Programmable Sensitivity	S_{PMAX}		–	333.3	–	mV/mT
Minimum Programmable Sensitivity	S_{PMIN}		–	41.7	–	mV/mT
Bandwidth [4]	f_{BW}	Small signal = –3 dB	–	1	–	MHz
Noise	e_N	T_A = 25°C, f_{BW} = 100 kHz, S = 41.7 mV/mT	–	6.44	–	μT_{RMS}
OUT ACCURACY PERFORMANCE [5]						
Linearity Error	E_{LIN}	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±0.3	–	% FS
Sensitivity Temperature Drift	E_{SENS_Tdrift}	B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to 125°C	–	±1.4	–	%
		B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to –40°C	–	±2.2	–	%
Offset Voltage Error	V_{OE}	B_{OP} = 0 mT, T_A = 25°C	–	±4	–	mV
Offset Voltage Temperature Drift	V_{OE_Tdrift}	B_{OP} = 0 mT, T_A = 25°C to 125°C	–	±15	–	mV
		B_{OP} = 0 mT, T_A = 25°C to –40°C	–	±26	–	mV
LIFETIME DRIFT [5]						
Sensitivity Error Including Lifetime Drift	$E_{SENS(DRIFT)}$	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±3	–	%
Offset Voltage Error Including Lifetime Drift	$V_{OE(DRIFT)}$	B_{OP} = 0 mT, T_A = –40°C to 125°C	–	±34	–	mV

[1] Tested on TSSOP package.
[2] Typical (typ) values are the mean ±3 sigma of a test sample population. These are formatted as mean ±3 sigma.
[3] Lifetime drift characteristics are based on a statistical combination of production distributions and the worst-case distribution of parametric drift of individuals observed during AEC-Q100 qualification.
[4] Guaranteed by design and characterization. Not tested in production.
[5] Linearity and sensitivity temperature drift performance vary as a function of the sensitivity programmed. Errors are smaller when sensitivity is closer to the 6 mT version.

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CT455-x00B3: Programmable Gain – ELECTRICAL CHARACTERISTICS: [1][2] V_{CC} = 3 to 3.6 V, T_A = –40°C to 125°C, C_{BYP} = 1 μF, unless otherwise specified; typical values are V_{CC} = 3.3 V and T_A = 25°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Programmable Magnetic Field Range	B_{PRNG}		±6	–	±8	mT
			±12	–	±48	mT
Voltage Output Quiescent	V_{OQ}		–	1.65	–	V
Maximum Programmable Sensitivity	S_{PMAX}		–	166.7	–	mV/mT
Minimum Programmable Sensitivity	S_{PMIN}		–	20.8	–	mV/mT
Bandwidth [3]	f_{BW}	Small signal = –3 dB	–	1	–	MHz
Noise	e_N	T_A = 25°C, f_{BW} = 100 kHz, S = 166 mV/mT	–	14	–	$μT_{RMS}$
OUT ACCURACY PERFORMANCE [4]						
Linearity Error	E_{LIN}	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±0.3	–	% FS
Sensitivity Temperature Drift	E_{SENS_Tdrift}	B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to 125°C	–	±1.4	–	%
		B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to –40°C	–	±2.2	–	%
Offset Voltage Error	V_{OE}	B_{OP} = 0 mT, T_A = 25°C	–	±4	–	mV
Offset Voltage Temperature Drift	V_{OE_Tdrift}	B_{OP} = 0 mT, T_A = 25°C to 125°C	–	±13	–	mV
		B_{OP} = 0 mT, T_A = 25°C to –40°C	–	±15	–	mV
LIFETIME DRIFT [4]						
Sensitivity Error Including Lifetime Drift	$E_{SENS(DRIFT)}$	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±3	–	%
Offset Voltage Error Including Lifetime Drift	$V_{OE(DRIFT)}$	B_{OP} = 0 mT, T_A = –40°C to 125°C	–	±20	–	mV

[1] Typical values are the mean ±3 sigma of a test sample population. These are formatted as mean ±3 sigma.
[2] Lifetime drift characteristics are based on a statistical combination of production distributions and the worst-case distribution of parametric drift of individuals observed during AEC-Q100 qualification.
[3] Guaranteed by design and characterization. Not tested in production.
[4] Linearity and sensitivity temperature drift performance vary as a function of the sensitivity programmed. Errors are smaller when sensitivity is closer to the 6 mT version.

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CT455-x00U5: Programmable Gain – ELECTRICAL CHARACTERISTICS: [1][2] V_{CC} = 4.75 to 5.5 V, T_A = –40°C to 125°C, C_{BYP} = 1 µF, unless otherwise specified; typical values are V_{CC} = 5 V and T_A = 25°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Programmable Magnetic Field Range	B_{PRNG}		0 to 6	–	0 to 8	mT
			0 to 12	–	0 to 48	mT
Voltage Output Quiescent	V_{OQ}		–	0.5	–	V
Maximum Programmable Sensitivity	S_{PMAX}		–	666.7	–	mV/mT
Minimum Programmable Sensitivity	S_{PMIN}		–	83.3	–	mV/mT
Bandwidth [3]	f_{BW}	Small signal = –3 dB	–	1	–	MHz
Noise	e_N	T_A = 25°C, f_{BW} = 100 kHz, S = 83.3 mV/mT	–	4.56	–	$µT_{RMS}$
OUT ACCURACY PERFORMANCE [4]						
Linearity Error	E_{LIN}	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±0.3	–	% FS
Sensitivity Temperature Drift	E_{SENS_Tdrift}	B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to 125°C	–	±1.4	–	%
		B_{OP} = $B_{OP(MAX)}$, T_A = 25°C to –40°C	–	±2.2	–	%
Offset Voltage Error	V_{OE}	B_{OP} = 0 mT, T_A = 25°C	–	±7	–	mV
Offset Voltage Temperature Drift	V_{OE_Tdrift}	B_{OP} = 0 mT, T_A = 25°C to 125°C	–	±11	–	mV
		B_{OP} = 0 mT, T_A = 25°C to –40°C	–	±25	–	mV
LIFETIME DRIFT [4]						
Sensitivity Error Including Lifetime Drift	$E_{SENS(DRIFT)}$	B_{OP} = $B_{OP(MAX)}$, T_A = –40°C to 125°C	–	±3	–	%
Offset Voltage Error Including Lifetime Drift	$V_{OE(DRIFT)}$	B_{OP} = 0 mT, T_A = –40°C to 125°C	–	±32	–	mV

[1] Typical (typ) values are the mean ±3 sigma of a test sample population. These are formatted as mean ±3 sigma.
[2] Lifetime drift characteristics are based on a statistical combination of production distributions and the worst-case distribution of parametric drift of individuals observed during AEC-Q100 qualification.
[3] Guaranteed by design and characterization. Not tested in production.
[4] Linearity and sensitivity temperature drift performance vary as a function of the sensitivity programmed. Errors are smaller when sensitivity is closer to the 6 mT version.

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Calibration Description

The CT455-x00 is factory-trimmed for sensitivity and offset temperature drift. The sensor provides the ability to adjust gain to allow for all the mechanical tolerances during manufacturing. Gain calibration is recommended to be performed at room temperature (25°C) using the LabView and NI PXI solution.

Device Programming

COMMUNICATION

The programmable versions of the device allow customization of the sensitivity and offset voltage. These devices use a one-time programming (OTP) method, and parameters can be adjusted through test modes (volatile) before permanent programming.

The test mode allows an external controller to read, write, and program the device. The device enters test mode when the TEST pin is pulled to 1.4 V above the VCC level. VCC must be 3.3 V.

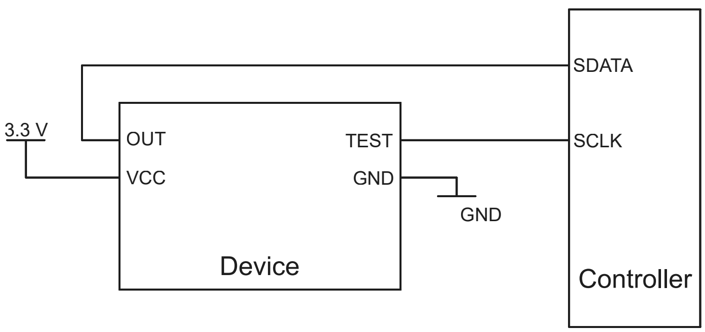

Figure 10: Programming Connections

Once the test mode is activated, the device expects 106 clock pulses on the TEST pin at the VCC voltage level or above, along with data on OUT. Those clock pulses should be separated by more than 1 µs and less than 100 µs. Data is read sequentially from the OUT pin upon each rising edge of TEST.

The fields for the data transmitted are:

- Key code (8 bits): should be 0b11110010; this prevents incorrect access
- OP code (2 bits):

OP Code	Description	OUT Operation	TEST Operation
0b00	Default operation	Analog output	Open drain digital output
0b01	Program (permanently burns fuses; cannot be undone)	Serial data input	SCLK input
0b10	Try (emulates a configuration without permanent change)	Serial data input	SCLK input
0b11	Read bits	Serial data output	SCLK output

- CTRL code (16 bits): controls the connections of multiplexers; leave at 0
- FBIT (80 bits): trimming bits for offset, sensitivity, and temperature compensation

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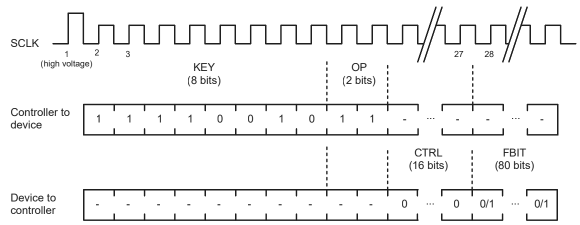
TIMING AND ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
SDATA Setup Time to SCLK	T_{SETUP}	15	–	–	ns
SDATA Hold Time to SCLK	T_{HOLD}	50	–	–	ns
SCLK Rise Time	T_{R1}	–	–	50	ns
SCLK Fall Time	T_{F1}	–	–	50	ns
SCLK High Time	T_{HIGH1}	500 [1]	–	–	ns
SCLK Low Time	T_{LOW1}	500 [1]	–	–	ns
SCLK High Voltage (typical pulse level for a test sequence)	V_{HIGH1}	0.7 × V_{DD}	–	V_{DD} + 1.5	V
SCLK High Voltage (the first pulse for a test sequence)	V_{HIGH1}	V_{DD} + 1.4	V_{DD} + 1.45	V_{DD} + 1.5	V
SCLK Low Voltage	V_{LOW1}	–0.3	–	0.3 × V_{DD}	V
SDATA Rise Time	T_{R2}	–	–	50	ns
SDATA Fall Time	T_{F2}	–	–	50	ns
SDATA High Time	T_{H2}	500	–	–	ns
SDATA Low Time	T_{LOW2}	500	–	–	ns
SDATA High Voltage	V_{HIGH2}	0.7 × V_{DD}	–	V_{DD}	V
SDATA Low Voltage	V_{LOW2}	–0.3	–	0.3 × V_{DD}	V
Supply Voltage	V_{DD}	2.97	3.3	4	V

[1] During programming, it should be greater than 2500 ns.

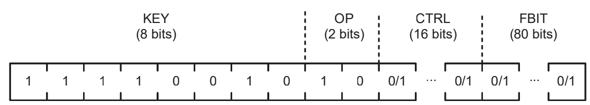
READ

After the device receives the correct KEY code and OP code = 0b11, it starts to output FBIT from the 28th SCLK pulse starting from FBIT[0].



WRITE (VOLATILE)

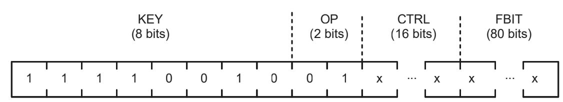
After the device receives the correct KEY code and OP code = 0b01, if FBIT[76] is not set, update CTRL and FBIT with the received data.



To update only a part of FBIT, all other bits must be written as well. It might be needed to first read FBIT, then write it back with the relevant bits updated.

WRITE (PERMANENT)

After the device receives the correct KEY code and OP code = 0b10, if FBIT[76] is not set, update CTRL and permanently fuse FBIT with the previously volatile programmed data. The CTRL and FBIT data sent along with the fuse command are discarded. Cannot be undone.



TIME OUT

After a high-voltage pulse, the device returns to typical operation (timeout event) if:

- An incorrect KEY code is received
- OP code = 0b00
- Two SCLK rising edges are separated by more than 100 µs.

Additional SCLK pulses after the 106 needed are discarded, but typical operation resumes only after timeout.

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BITS DESCRIPTION

Location	Name	Description	Bits	Factory Default
CTRL[0:16]	Control bits	Factory trimmed. Do not modify.	16	0x00
FBIT[0]	–	Factory trimmed. Do not modify.	1	0
FBIT[19:1]	–	Factory trimmed. Do not modify.	19	Trimmed
FBIT[27:20]	V_OS_MAG_LEFT	Trims the magnetic offset of the left AFE up/down.	8	0
FBIT[35:28]	V_OS_MAG_RIGHT	Trims the magnetic offset of the right AFE up/down.	8	0
FBIT[43:36]	V_OS_ELECT_LEFT	Trims the electronic offset of the left AFE up/down.	8	0
FBIT[51:44]	V_OS_ELECT_RIGHT	Trims the electronic offset of the right AFE up/down.	8	0
Bit[59:52]	GAIN_INSTR_AMPS_LEFT	Trims the gain of the left AFE up/down.	8	0
Bit[67:60]	GAIN_INSTR_AMPS_ RIGHT	Trims the gain of the right AFE up/down.	8	0
Bit[69:68]	–	Factory trimmed. Do not modify.	2	Trimmed
Bit[70]	GAIN_FOR_12MT	If Lo → 8 mT (20 A)/Hi → 12 mT (30 A) full-scale field.	1	0
Bit[79:71]	–	Factory trimmed. Do not modify.	9	Trimmed

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FUNCTIONAL DESCRIPTION

Overview

The CT455 is a very-high-accuracy, coreless, contactless current sensor that can sense magnetic fields from 6 to 48 mT. The device has high sensitivity and a wide dynamic range with excellent accuracy (low total output error) across temperature.

The CT455 is also available in a user-programmable variant that enables end-of-line calibration of gain. While the sensor is preprogrammed to adjust sensitivity and offset temperature drift, the ability to adjust gain relaxes mechanical tolerances during sensor mounting.

When current is flowing through a busbar above or below the CT455, the XtremeSense TMR sensor inside the chip senses the field and generates corresponding differential voltage signals that then pass through the analog front-end (AFE) to output a current measurement.

The chip is designed to enable a fast response time of 300 ns for the current measurement from the OUT pin, as the bandwidth for the CT455 is 1 MHz. Even with a high bandwidth, the chip consumes a minimal amount of power.

Testing and Quality Assurance

Testing of the CT455 was conducted following AEC-Q100 standards to ensure reliability and performance in automotive conditions. During qualification, only the offset voltage error was tested at –40°C, 25°C, and 125°C. Sensitivity error was not checked directly during qualification but is estimated from qualification of the same ASIC in an SOIC8 package with a different leadframe.

Linear Output Current Measurement

The CT455 provides a continuous linear analog output voltage that represents the magnetic field generated by the current flowing through the busbar.

For the 5 V variant, the output voltage range of OUT is from 0.5 to 4.5 V with a V_{OQ} of 0.5 and 2.5 V for unidirectional and bidirectional fields, respectively. The output voltage range of the OUT pin as a function of the measured field is illustrated in Figure 11.

For the 3.3 V variant, the output voltage range of OUT is from 0.65 to 2.65 V with a V_{OQ} of 0.65 and 1.65 V for unidirectional and bidirectional fields, respectively. The output voltage range of the OUT pin as a function of the measured field is illustrated in Figure 12.

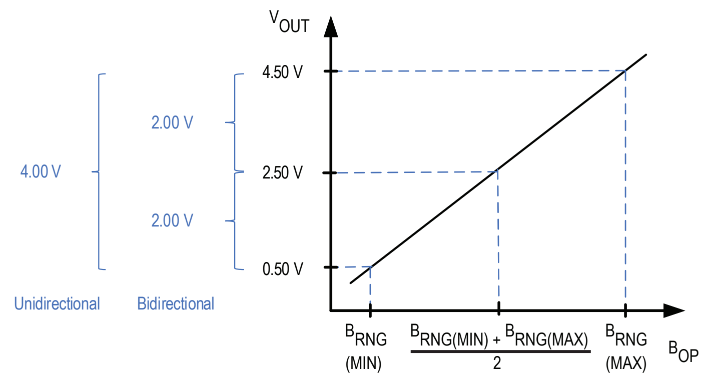

Figure 11: Linear Output Voltage Range (OUT) vs. Measured Magnetic Field (B_{OP})

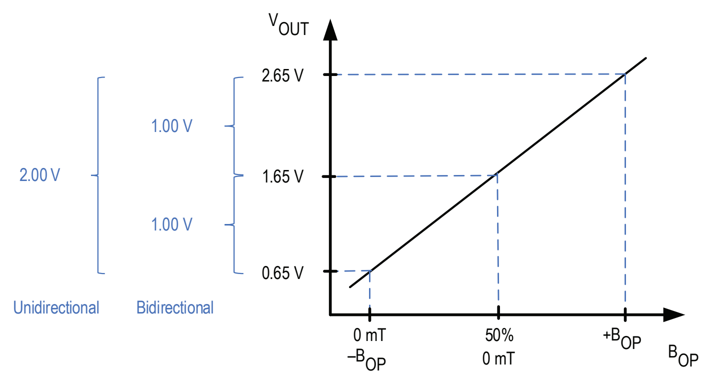

Figure 12: Linear Output Voltage Range (OUT) vs. Measured Magnetic Field (B_{OP})

Power-On Time (t_{ON})

Power-on time (t_{ON}) of 100 µs is the amount of time required by CT455 to start up, fully power the chip, and become fully operational from the moment the supply voltage is greater than the UVLO voltage. This time includes the ramp-up time and the settling time (within 10% of steady-state voltage under an applied magnetic field) after the power supply has reached the minimum V_{CC}.

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Response Time ($t_{RESPONSE}$)

Response time ($t_{RESPONSE}$) is the period of time between:

1. When the primary current signal reaches 90% of its final value, and
2. When the chip reaches 90% of its output corresponding to the applied current.

The CT455 has a response time of 300 ns.

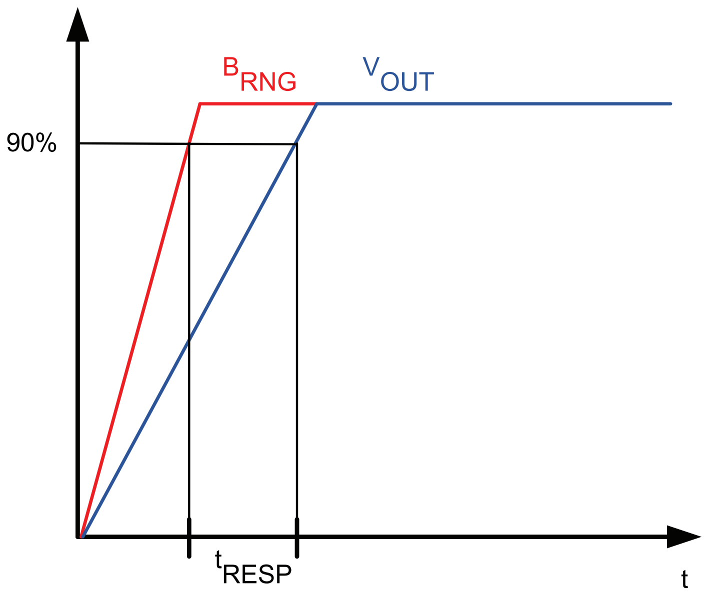

Figure 13: CT455 Response Time Curve

Rise Time (t_{RISE})

Rise time (t_{RISE}) is the period of time between when 10% and 90% of the full-scale output voltage is reached.

The CT455 has a rise time of 200 ns.

Propagation Delay (t_{DELAY})

Propagation delay (t_{DELAY}) is the period of time between:

1. When the primary current reaches 20% of its final value, and
2. When the chip reaches 20% of its output corresponding to the applied current.

The CT455 has a propagation delay of 250 ns.

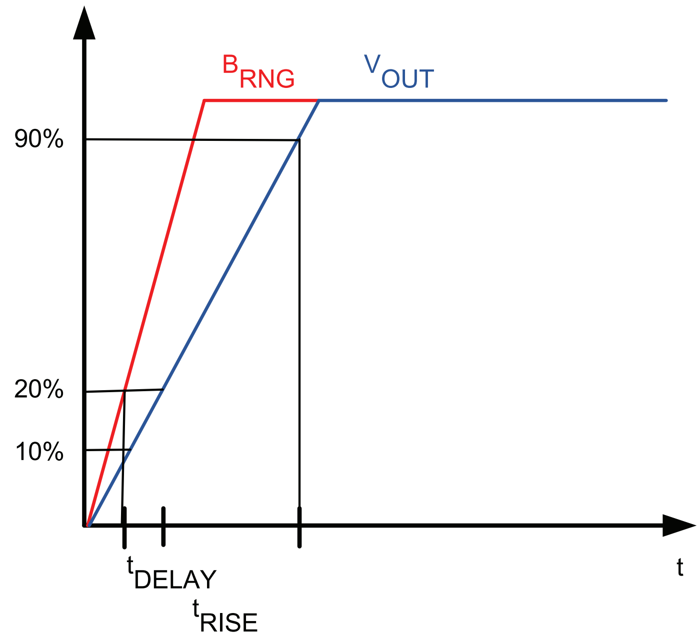

Figure 14: CT455 Propagation Delay and Rise Time Curve

Undervoltage Lockout (UVLO)

The undervoltage lockout protection circuitry of the CT455 is activated when the supply voltage (V_{CC}) reduces to less than 2.45 V. The CT455 remains in a low quiescent state until V_{CC} increases to greater than the UVLO threshold (2.5 V). In the condition where V_{CC} is less than 2.45 V and UVLO is triggered, the output from the CT455 is not valid. Once V_{CC} increases to greater than 2.5 V, the UVLO is cleared.

Current Sensing

The CT455 can sense and, therefore, measure the current by either placing a current-carrying busbar above or under the device. The chip is also sensitive enough to measure the current from a PCB trace that is routed beneath it.

Bypass Capacitor

A single 1 µF capacitor is needed for the VCC pin to reduce the noise from the power supply and other circuits. This capacitor should be placed as close as practical to the CT455 to minimize inductance and resistance between the two devices.

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XtremeSense TMR Current Sensor Location

The XtremeSense TMR current sensor location of the CT455 is shown in the figures that follow. All dimensions in the figures are nominal.

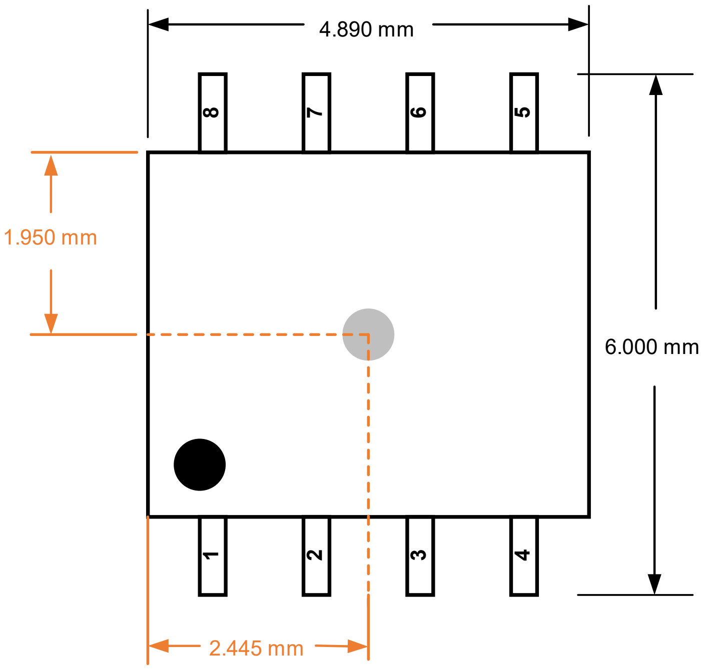

Figure 15: XtremeSense TMR Current Sensor Location in x-y Plane for CT455 in SOIC-8 Package

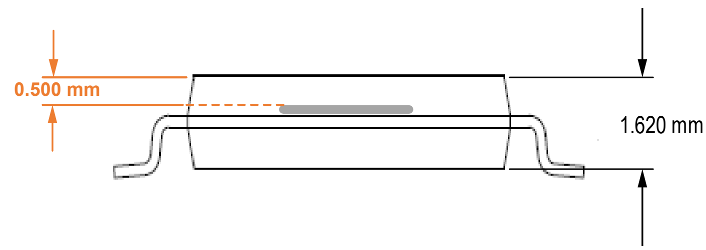

Figure 16: XtremeSense TMR Current Sensor Location in z Dimension for CT455 in SOIC-8 Package

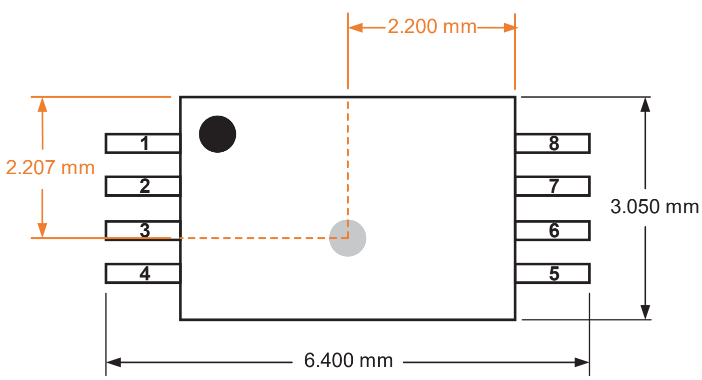

Figure 17: XtremeSense TMR Current Sensor Location in x-y Plane for CT455 in TSSOP-8 Package

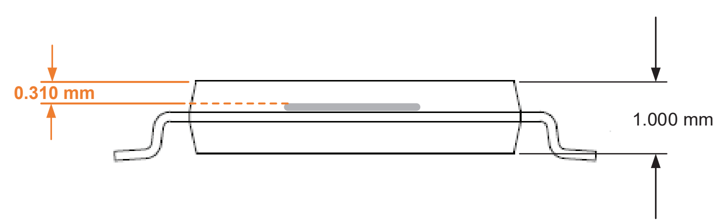

Figure 18: XtremeSense TMR Current Sensor Location in z Dimension for CT455 in TSSOP-8 Package

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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

Dimensions in millimeters – NOT TO SCALE

Dimensions exclusive of mold flash, gate burs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown

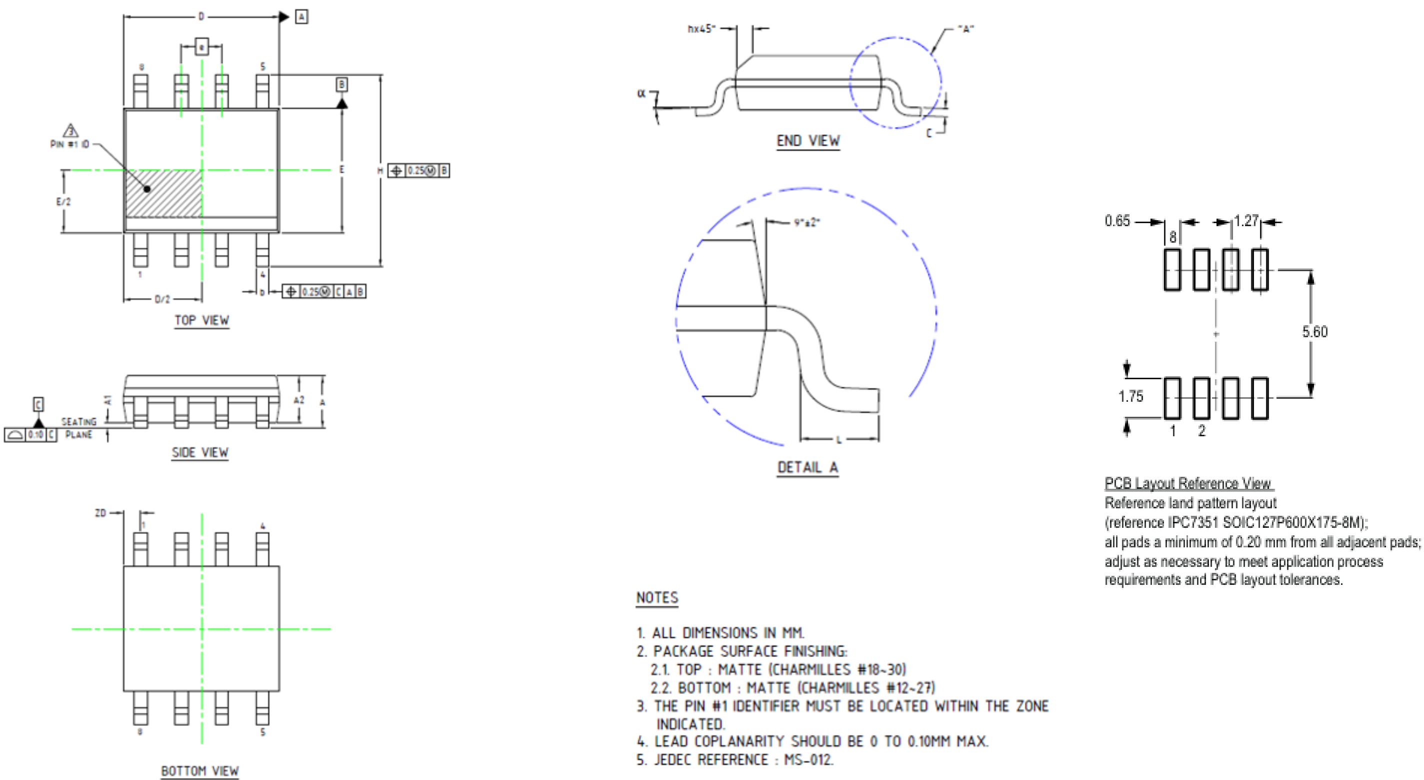

Figure 19: SOIC-8 Package Drawing and Dimensions

Table 1: CT455 SOIC-8 Package Dimensions

Symbol	Dimensions in Millimeters (mm)		
	Min.	Typ.	Max.
A1	0.10	0.18	0.25
b	0.36	0.41	0.46
C	0.19	0.22	0.25
D	4.80	4.89	4.98
E	3.81	3.90	3.99
e	1.27 BSC		
H	5.80	6.00	6.20
h	0.25	0.37	0.50
L	0.41	–	1.27
A	1.52	1.62	1.72
α	0°	–	8°
ZD	0.53 REF		
A2	1.37	1.47	1.57

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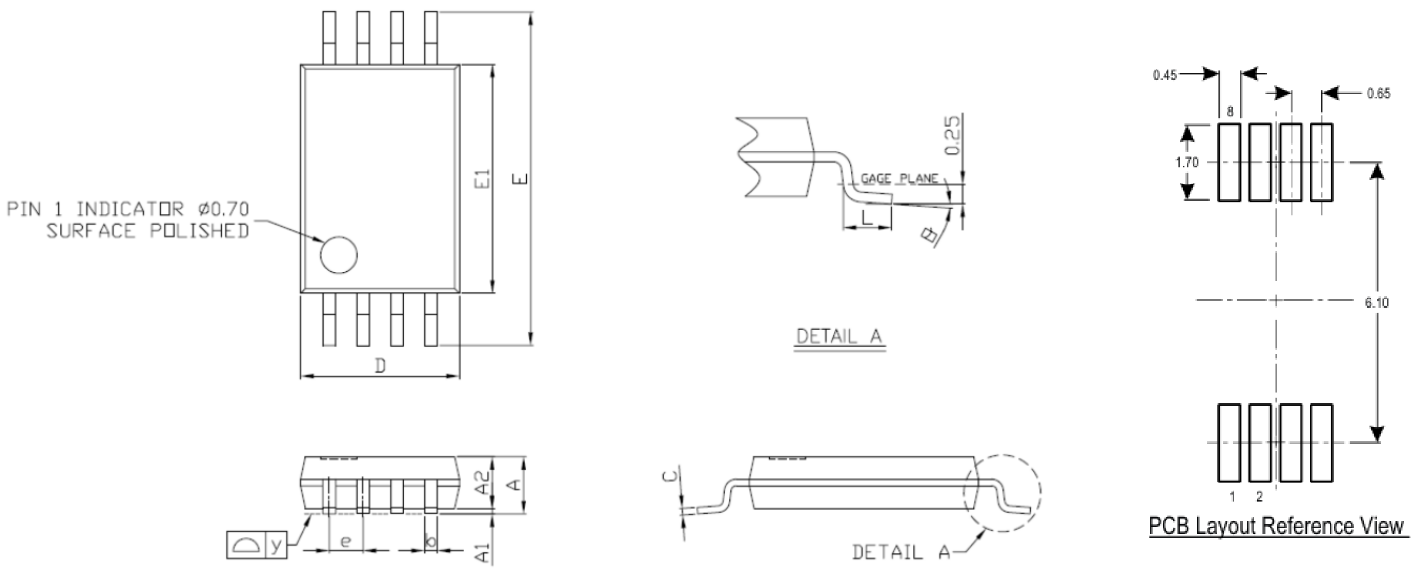

Figure 20: TSSOP-8 Package Drawing and Dimensions

Table 2: CT455 TSSOP-8 Package Dimensions

Symbol	Dimensions in Millimeters (mm)		
	Min.	**Typ.**	**Max.**
A	1.05	1.10	1.20
A1	0.05	0.10	0.15
A2	–	1.00	1.05
b	0.25	–	0.30
C	–	0.127	–
D	2.90	3.05	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	–	0.65	–
L	0.50	0.60	0.70
y	–	–	0.076
θ	0°	4°	8°

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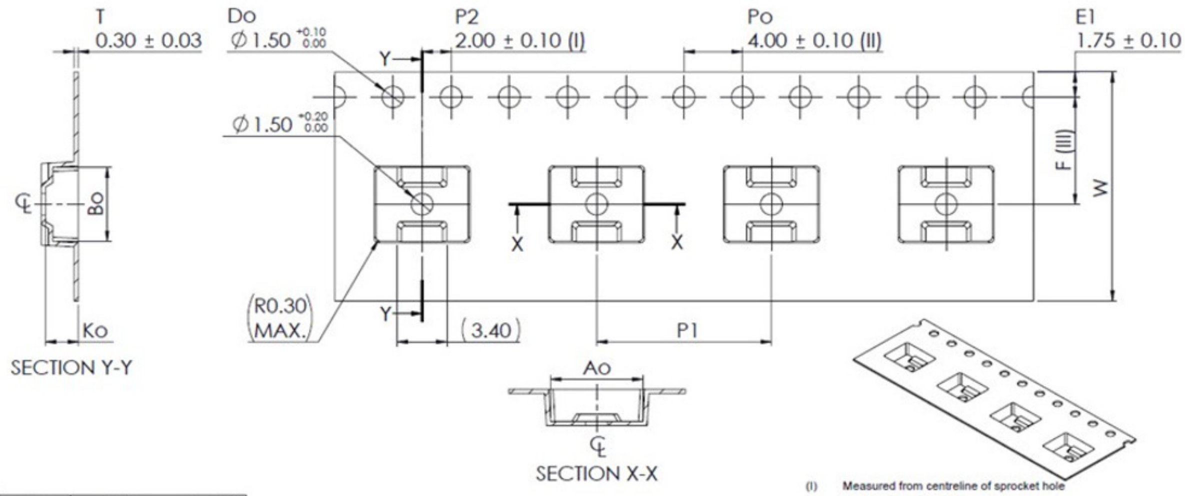
TAPE AND REEL POCKET DRAWINGS AND DIMENSIONS

For Reference Only – Not for Tooling Use

Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

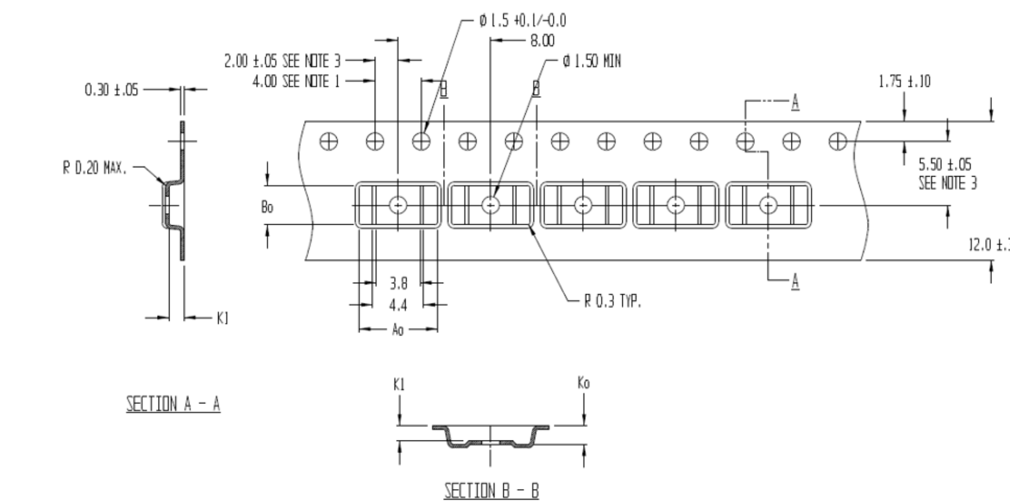


Ao	6.35	+/- 0.10
Bo	5.13	+/- 0.10
Ko	2.25	+/- 0.15
K1	1.75	+/- 0.10
F	7.50	+/- 0.10
P1	12.00	+/- 0.10
W	16.00	+0.30 / -0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension with ( ) is used for design reference purposes, No measurement required.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 21: Tape-and-Pocket Drawing for SOIC-8 Package



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Ao = 6.80
Bo = 3.40
Ko = 1.60
K1 = 1.30

Figure 22: Tape-and-Pocket Drawing for TSSOP-8 Package

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DEVICE MARKINGS

Figure 23: CT455 Device Marking for Eight-Lead TSSOP Package

Table 3: CT455 Device Marking Definition for Eight-Lead TSSOP Package

Row No.	Code	Definition
1	•	Pin 1 Indicator
2	CT455	Allegro Part Number
3	XX	Maximum Magnetic Field Rating
3	B	Sensing Polarity
3	V	Supply Voltage
4	YY	Calendar Year
4	WW	Work Week
4	LL	Lot Code

Figure 24: CT455 Device Marking for Eight-Lead SOIC Package

Table 4: CT455 Device Marking Definition for Eight-Lead SOIC Package

Row No.	Code	Definition
4	•	Pin 1 Indicator
1	CT455	Allegro Part Number
2	XX	Maximum Field Rating
2	B	Sensing Polarity
2	V	Supply Voltage
3	YY	Calendar Year
3	WW	Work Week
3	LL	Lot Code

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PART ORDERING NUMBER LEGEND

CT 4 5 5 - T FR X V - PKG

Package Type
SN08 = 8-lead SOIC
TS08 = 8-lead TSSOP

Voltage
5 = V_{CC} is 5 V
3 = V_{CC} is 3.3 V

Polarity
U = Unipolar Magnetic Field
B = Bipolar Magnetic Field

Field Range
00 = User Programmable
06 = 6 mT
48 = 48 mT

Temperature Range
A = AEC-Q100 Grade 1

Current Sensor Variant
5 = dV/dt Optimized Sensor

Current Sensor Type
5 = Contactless Current Sensor

Product Family
4 = Current Sensor

CT = Product Identifier

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Revision History

Number	Date	Description
2	November 2, 2023	Document rebranded and minor editorial updates
3	January 25, 2024	Corrected packaging column in Selection Guide table (page 3)
4	March 6, 2024	Removed AEC-Q100 (pages 1, 2, 19-20) Updated Offset Voltage (pages 8-11); removed Out Accuracy Performance (pages 8-11); updated Sensitivity and removed Noise (page 11)
5	March 20, 2024	Updated Features and Benefits (page 1), Figure 3 and 4 (page 4), Terminal Lists (page 5), and Device Markings (page 19)
6	July 29, 2024	Major overhaul to reflect automotive-qualified part per details provided in the new Testing and Quality Assurance section: changed preset magnetic field ranges (page 1) and all part numbers in the selection guide (page 2); removed evaluation board selection guide (page 3) and recommended external components tables (page 4); changed application diagrams (page 4) and electrical characteristics symbols for OUT capacitive load and OUT resistive load (page 6); removed voltage output quiescent and lifetime drift characteristics (page 6) and bandwidth performance plot (page 7); replaced device-specific electrical characteristic tables (pages 8 through 12); added Device Programming section (pages 13 through 15), Testing and Quality Assurance section (page 16), and 3.3 variant information in the Linear Output Current Measurement section (page 16); replaced current sensor position images (page 18); added PCB outlines to package drawings (pages 19-20); updated Device Markings section (page 22) and Part Ordering Number Legend section (page 23); and made minor editorial changes throughout (all pages), including removal of trailing zeros, reformatting of some images for readability (larger text), removal of archaic language (normal changed to typical), and minimization of the use of title case.
7	August 9, 2024	Updated Selection Guide (page 2); updated Device Programming Communication Table (page 13); updated Device Markings section (page 22)

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