# XTSDG/Q0xG

## 3.3V/1.8V 1/2/4/8G-bit
## SD NAND Flash Memory
## Datasheet

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# SD NAND Flash Memory

**3.3V/1.8V SD 2.0 Interface**

■ **1/2/4/8G-bit SD NAND Flash Memory**

- Based on Single-level cell (SLC) NAND technology
- Support 3.3V/1.8V voltage

■ **SD Interface**

- Compatible with SD 2.0
- Support 1bit/4bit SD mode, 1bit SPI mode
- Support default speed mode and high speed mode
- Support SD command class 0/2/4/5/6/7/8/10

■ **High Performance**

- 50MHz for high speed mode
- Write speed up to class 6

■ **Advanced NAND Management**

- Built-in 14bits/512Byte hardware ECC engine
- Advanced bad block management
- Advanced wear leveling algorithm

■ **Single Supply Voltage**

- XTSDG0xG series: 2.7V~3.6V
- XTSDQ0xG series: 1.7~1.95V

■ **High Reliability**

- Enhance power cycling support
- P/E cycles with ECC: 100K
- Data retention: 10 years

■ **Temperature Operating Range**

- Industrial grade temperature range: -40~85°C

■ **Package**

- 8-pin WSON (8x6mm)
- 8-pin LGA(6x5mm) for 1.8V 1Gb/2Gb
- All Packages are RoHS Compliant and Halogen-free

# CONTENTS

# 1. Introduction

XTX SD NAND is an embedded storage solution designed in a WSON8 package or a LGA8 package form. The operation of SD NAND is similar to a SD card which is an industry standard.

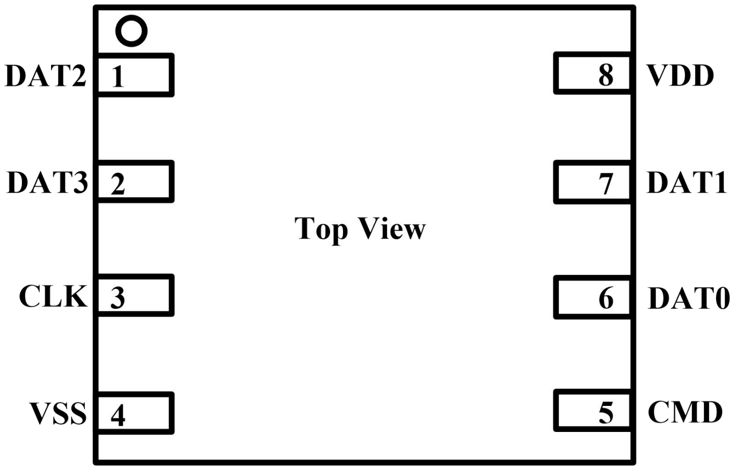
SD NAND consists of NAND flash and a high performance controller. Both 1.8V and 3.3V supply voltage series are supported.

XTX SD NAND is fully compliant with SD2.0 interface, which allows most of the embedded applications to easily adopt at a competitive cost with high reliability and low power consumption.

# 2. Ordering Part Number

| OPN | Voltage Range | Capacity | Package Type | Package Carrier |
|---|---|---|---|---|
| XTSDG01GWSIGA | 2.7-3.6V | 1Gbit | WSON8 8x6mm | Tray |
| XTSDG02GWSIGA | 2.7-3.6V | 2Gbit | WSON8 8x6mm | Tray |
| XTSDG04GWSIGA | 2.7-3.6V | 4Gbit | WSON8 8x6mm | Tray |
| XTSDG08GWSIGA | 2.7-3.6V | 8Gbit | WSON8 8x6mm | Tray |
| XTSDQ01GWSIGA | 1.7-1.95V | 1Gbit | WSON8 8x6mm | Tray |
| XTSDQ02GWSIGA | 1.7-1.95V | 2Gbit | WSON8 8x6mm | Tray |
| XTSDQ04GWSIGA | 1.7-1.95V | 4Gbit | WSON8 8x6mm | Tray |
| XTSDQ08GWSIGA | 1.7-1.95V | 8Gbit | WSON8 8x6mm | Tray |
| XTSDQ01GLAIGA | 1.7-1.95V | 1Gbit | LGA8 6x5mm | Tray |
| XTSDQ02GLAIGA | 1.7-1.95V | 2Gbit | LGA8 6x5mm | Tray |

# 3. Pin Assignments



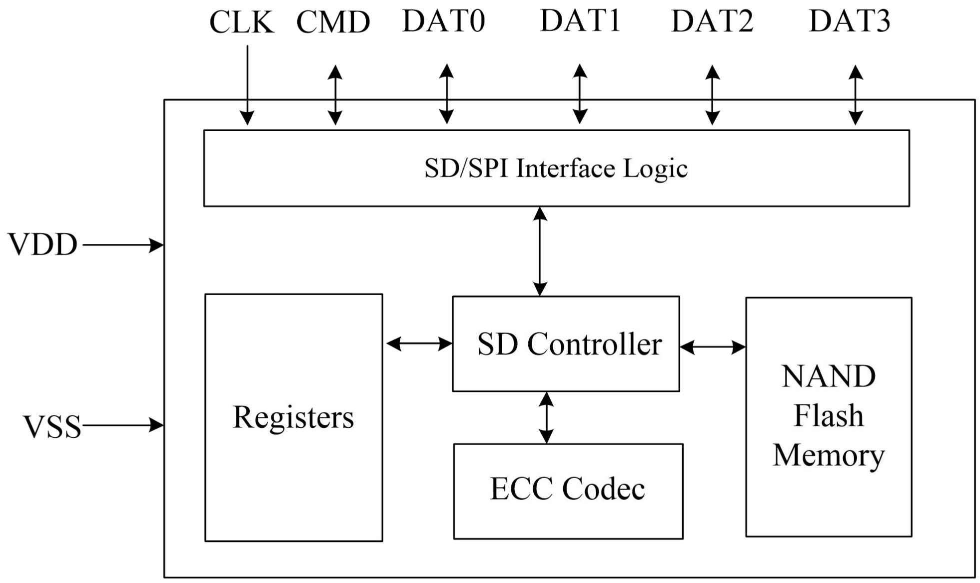

WSON8/LGA8

## 3.1 Pin Description

| Pin # | SD Interface | | | SPI Interface | | |
|---|---|---|---|---|---|---|
| | Pin Name | Type | Description | Pin Name | Type | Description |
| 1 | **DAT2** | I/O/PP | Data Line [bit2] | **Reserved** | Reserved | Reserved |
| 2 | **DAT3/CD** | I/O/PP | Data Line[bit3] / SD NAND Detection | **CS** | I | Chip Select |
| 3 | **CLK** | I | Clock | **CLK** | I | Clock |
| 4 | **VSS** | S | Ground | **VSS** | S | Ground |
| 5 | **CMD** | PP | Command/Response | **DI** | I | Data in |
| 6 | **DAT0** | I/O/PP | Data Line [bit0] | **DO** | O/PP | Data out |
| 7 | **DAT1** | I/O/PP | Data Line [bit1] | **Reserved** | Reserved | Reserved |
| 8 | **VDD** | S | Supply voltage | **VDD** | S | Supply voltage |

**Notes:**
1. S: power supply; I: input; O: output; PP: I/O using push-pull drivers.
2. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command.

# 4. Block Diagram



# 5. Product Specification

## 5.1 System Performance

| OPN | Voltage Range | Sequential Read Performance (MB/s) | Sequential Write Performance (MB/s) |
|---|---|---|---|
| XTSDG01GWSIGA | 2.7-3.6V | 20 | 4 |
| XTSDG02GWSIGA | 2.7-3.6V | 20 | 4 |
| XTSDG04GWSIGA | 2.7-3.6V | 20 | 6 |
| XTSDG08GWSIGA | 2.7-3.6V | 20 | 6 |
| XTSDQ01GWSIGA<br>XTSDQ01GLAIGA | 1.7-1.95V | 20 | 4 |
| XTSDQ02GWSIGA<br>XTSDQ02GLAIGA | 1.7-1.95V | 20 | 4 |
| XTSDQ04GWSIGA | 1.7-1.95V | 20 | 6 |
| XTSDQ08GWSIGA | 1.7-1.95V | 20 | 6 |

## 5.2 Timeout Error Conditions

| Timing | Max. Value |
|---|---|
| Block Read Access Timeout | 100ms |
| Block Write Access Timeout | 250ms |
| Initialization Timeout(ACMD 41)[1] | 1s |

**Notes:**
1.The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the SD NAND does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

## 5.3 Registers

Six registers are defined within the SD interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands.

The OCR, CID, CSD and SCR registers carry the specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. OCR Register, the 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits.

### 5.3.1 OCR Register

OCR Register Definition - 3.3V

| OCR bit | VDD Voltage Window | OCR Value |
|---|---|---|
| 0 - 6 | Reserved | All "0" |
| 7 | Reserved for low voltage range | 0 |
| 8 - 14 | Reserved | All "0" |
| 15 | 2.7 - 2.8 | 1 |
| 16 | 2.8 - 2.9 | 1 |
| 17 | 2.9 - 3.0 | 1 |
| 18 | 3.0 - 3.1 | 1 |
| 19 | 3.1 - 3.2 | 1 |
| 20 | 3.2 - 3.3 | 1 |
| 21 | 3.3 - 3.4 | 1 |
| 22 | 3.4 - 3.5 | 1 |
| 23 | 3.5 - 3.6 | 1 |
| 24 - 29 | Reserved | All "0" |
| 30 | Card Capacity status(CCS)[1] | 0 |
| 31 | Card power up status bit(busy)[2] | "0" = busy ,"1" = ready |

**Notes:**

1. This bit is valid only when the power up status bit is set.
2. This bit is set to LOW if the SD NAND has not finished the power up routine.

OCR Register Definition - 1.8V

| OCR bit | VDD Voltage Window | OCR Value |
|---|---|---|
| 0 - 6 | Reserved | All “0” |
| 7 | Reserved for low voltage range | 0 |
| 8 - 14 | Reserved | All “0” |
| 15 | 2.7 - 2.8 | 0 |
| 16 | 2.8 - 2.9 | 0 |
| 17 | 2.9 - 3.0 | 0 |
| 18 | 3.0 - 3.1 | 0 |
| 19 | 3.1 - 3.2 | 0 |
| 20 | 3.2 - 3.3 | 0 |
| 21 | 3.3 - 3.4 | 0 |
| 22 | 3.4 - 3.5 | 0 |
| 23 | 3.5 - 3.6 | 0 |
| 24 - 29 | Reserved | All “0” |
| 30 | Card Capacity status(CCS)[1] | 0 |
| 31 | Card power up status bit(busy)[2] | “0” = busy ,“1” = ready |

**Notes:**

1. This bit is valid only when the power up status bit is set.
2. This bit is set to LOW if the SD NAND has not finished the power up routine.

### 5.3.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. It is programmed during manufacturing and cannot be changed by hosts.

The structure of the CID register is defined in the following paragraphs:

CID Register Fields

| Name | Field | Type | Width | CID Value | | | |
|---|---|---|---|---|---|---|---|
| | | | | 1Gb | 2Gbit | 4Gb | 8Gb |
| Manufacturer ID | MID | Binary | 8 | TBD | | | |
| OEM/Application ID | OID | ASCII | 16 | TBD | | | |
| Product name | PNM | ASCII | 40 | TBD | | | |
| Product revision | PRV | BCD | 8 | TBD | | | |
| Product serial number | PSN | Binary | 32 | Controlled by Production Lot | | | |
| Reserved | - | - | 4 | All "0" | | | |
| Manufacturing date | MDT | BCD | 12 | Manufacture date | | | |
| CRC7 checksum | CRC | Binary | 7 | CRC | | | |
| not used, always '1' | - | - | 1 | 1b | | | |

### 5.3.3 CSD Register

The Card-Specific Data register provides information on how to access the SD NAND contents. The CSD defines the data format, error correction type, maxi- mum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register can be changed by CMD27. The type of the entries in the table below is coded as follows: R = readable, W=multiple writable.

The CSD Register Fields (CSD Version 1.0)

| Name | Field | Width | Cell Type | CSD-slice | CSD Value | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | 1Gb | 2Gb | 4Gb | 8Gb |
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] | 00b | | | |
| Reserved | - | 6 | R | [125:120] | 000000b | | | |
| Data read access-time 1 | TAAC | 8 | R | [119:112] | 7Fh | | | |
| Data read access-time 2<br>In CLK cycles(NSAC*100) | NSAC | 8 | R | [111:104] | 00h | | | |
| Max. data transfer rate | TRAN_SPEED | 8 | R | [103:96] | 32h | | | |
| Card command classes | CCC | 12 | R | [95:84] | 010110110101b | | | |
| Max. read data block length | READ_BL_LEN | 4 | R | [83:80] | 1001b | | | 1010b |
| Partial blocks for read allowed | READ_BL_PARTIAL | 1 | R | [79:79] | 1b | | | |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | [78:78] | 0b | | | |
| Read block misalignment | READ_BLK_MISALIGN | 1 | R | [77:77] | 0b | | | |
| DSR implemented | DSR_IMP | 1 | R | [[76:76] | 0b | | | |
| Reserved | - | 2 | R | [75:74] | 00b | | | |
| Device size | C_SIZE | 12 | R | [73:62] | TBD | TBD | TBD | TBD |
| Max. read current @ VDD min | VDD_R_CURR_MIN | 3 | R | [61:59] | 101b | | | |
| Max. read current @ VDD max | VDD_R_CURR_MAX | 3 | R | [58:56] | 110b | | | |
| Max. write current @ VDD min | VDD_W_CURR_MIN | 3 | R | [55:53] | 101b | | | |
| Max. write current @ $V_{DD}$ max | VDD_W_CURR_MAX | 3 | R | [52:50] | 110b | | | |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] | 110b | | | |
| Erase single block enable | ERASE_BLK_EN | 1 | R | [46:46] | 1b | | | |
| Erase sector size | SECTOR_SIZE | 7 | R | [45:39] | 1111111b | | | |
| Write protect group size | WP_GRP_SIZE | 7 | R | [38:32] | 0011111b | | | |
| Write protect group enable | WP_GRP_ENABLE | 1 | R | [31:31] | 1b | | | |
| Reserved | - | 2 | R | [30:29] | 00b | | | |
| Write speed factor | R2W_FACTOR | 3 | R | [28:26] | 101b | | | |
| Max. write data block length | WRITE_BL_LEN | 4 | R | [25:22] | 1001b | | | 1010b |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | R | [21:21] | 0b | | | |
| Reserved | - | 5 | R | [20:16] | 00000b | | | |
| File format group | FILE_FORMAT_GRP | 1 | R | [15:15] | 0b | | | |
| Copy flag (OTP) | COPY | 1 | R | [14:14] | 0b | | | |
| Permanent write protection | PERM_WRITE_PROTECT | 1 | R | [13:13] | 0b | | | |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W | [12:12] | 0b | | | |
| File format | FILE_FORMAT | 2 | R | [11:10] | 00b | | | |
| Reserved | - | 2 | R | [9:8] | 00b | | | |
| CRC | CRC | 7 | R | [7:1] | xxxxxxxb | | | |
| Not used, always '1' | - | 1 | - | [0:0] | 1b | | | |

### 5.3.4 RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

### 5.3.5 SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD NAND's special features. The following table describes the SCR register content.

The SCR Fields

| Name | Field | Width | Cell Type | CSD-slice | CSD Value | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | 1Gb | 2Gb | 4Gb | 8Gb |
| SCR structure | SCR_STRUCTURE | 4 | R | [63:60] | 000b | | | |
| SD Memory Card - Spec. Version | SD_SPEC | 4 | R | [59:56] | 0010b | | | |
| Data_Status_after_Erases | DATA_STAT_AFTER_ERASE | 1 | R | [55:55] | 1b | | | |
| SD Security Support | SD_SECURITY | 3 | R | [54:52] | 010b | | | |
| DAT Bus Widths Supported | SD_BUS_WIDTHS | 4 | R | [51:48] | 0101b | | | |
| Reserved | - | 16 | R | [46:34] | - | | | |
| Reserved for Manufacturer Usage | - | 32 | R | [31:0] | - | | | |

# 6. Command

## 6.1 SD Mode Command

SD Mode Command Set (+: Implemented -: Not Implemented)

| CMD | Abbreviation | Implementation | Notes |
|---|---|---|---|
| CMD0 | GO_IDLE_STATE | + | |
| CMD2 | ALL_SEND_CID | + | |
| CMD3 | SEND_RELATIVE_ADDR | + | |
| CMD4 | SET_DSR | - | DSR register is not implemented |
| CMD6 | SWITCH_FUNC | + | |
| CMD7 | SELECT/DESELECT_CARD | + | |
| CMD8 | SEND_IF_COND | + | |
| CMD9 | SEND_CSD | + | |
| CMD10 | SEND_CID | + | |
| CMD12 | STOP_TRANSMISSION | + | |
| CMD13 | SEND_STATUS | + | |
| CMD15 | GO_INACTIVE_STATE | + | |
| CMD16 | SET_BLOCKLEN | + | |
| CMD17 | READ_SINGLE_BLOCK | + | |
| CMD18 | READ_MULTIPLE_BLOCK | + | |
| CMD24 | WRITE_BLOCK | + | |
| CMD25 | WRITE_MULTIPLE_BLOCK | + | |
| CMD27 | PROGRAM_CSD | + | |
| CMD28 | SET_WRITE_PROT | + | |
| CMD29 | CLR_WRITE_PROT | + | |
| CMD30 | SEND_WRITE_PROT | + | |
| CMD32 | ERASE_WR_BLK_START | + | |
| CMD33 | ERASE_WR_BLK_END | + | |
| CMD38 | ERASE | + | |
| CMD42 | LOCK_UNLOCK | + | |
| CMD55 | APP_CMD | + | |
| CMD56 | GEN_CMD | - | This command is for vendor-specific |
| ACMD6 | SET_BUS_WIDTH | + | |
| ACMD13 | SD_STATUS | + | |
| ACMD22 | SEND_NUM_WR_BLOCKS | + | |
| ACMD23 | SET_WR_BLK_ERASE_COUNT | + | |
| ACMD41 | SD_APP_OP_COND | + | |
| ACMD42 | SET_CLR_CARD_DETECT | + | |
| ACMD51 | SEND_SCR | + | |
| ACMD18 | SECURE_READ_MULTI_BLOCK | - | |
| ACMD25 | SECURE_WRITE_MULTI_BLOC | - | |
| ACMD26 | SECURE_WRITE_MKB | - | |
| ACMD38 | SECURE_ERASE | - | |
| ACMD43 | GET_MKB | - | |
| ACMD44 | GET_MID | - | |
| ACMD45 | SET_CER_RN1 | - | |
| ACMD46 | SET_CER_RN2 | - | |
| ACMD47 | SET_CER_RES2 | - | |
| ACMD48 | SET_CER_RES1 | - | |
| ACMD49 | CHANGE_SECURE_AREA | - | |

## 6.2 SPI Mode Command

SPI Mode Command Set (+: Implemented -: Not Implemented)

| CMD | Abbreviation | Implementatio | Notes |
|---|---|---|---|
| CMD0 | GO_IDLE_STATE | + | |
| CMD1 | SEND_OP_CND | + | |
| CMD6 | SWITCH_FUNC | + | |
| CMD8 | SEND_IF_COND | + | |
| CMD9 | SEND_CSD | + | |
| CMD10 | SEND_CID | + | |
| CMD12 | STOP_TRANSMISSION | + | |
| CMD13 | SEND_STATUS | + | |
| CMD16 | SET_BLOCKLEN | + | |
| CMD17 | READ_SINGLE_BLOCK | + | |
| CMD18 | READ_MULTIPLE_BLOCK | + | |
| CMD24 | WRITE_BLOCK | + | |
| CMD25 | WRITE_MULTIPLE_BLOCK | + | |
| CMD27 | PROGRAM_CSD | + | |
| CMD28 | SET_WRITE_PROT | + | |
| CMD29 | CLR_WRITE_PROT | + | |
| CMD30 | SEND_WRITE_PROT | + | |
| CMD32 | ERASE_WR_BLK_START_ADD | + | |
| CMD33 | ERASE_WR_BLK_END_ADDR | + | |
| CMD38 | ERASE | + | |
| CMD42 | LOCK_UNLOCK | + | |
| CMD55 | APP_CMD | + | |
| CMD56 | GEN_CMD | - | This command is for vendor-specific |
| CMD58 | READ_OCR | + | |
| CMD59 | CRC_ON_OFF | + | |
| ACMD13 | SD_STATUS | + | |
| ACMD22 | SEND_NUM_WR_BLOCKS | + | |
| ACMD23 | SET_WR_BLK_ERASE_COUNT | + | |
| ACMD41 | SD_APP_OP_COND | + | |
| ACMD42 | SET_CLR_CARD_DETECT | + | |
| ACMD51 | SEND_SCR | + | |
| ACMD18 | SECURE_READ_MULTI_BLOC | - | |
| ACMD25 | SECURE_WRITE_MULTI_BLO | - | |
| ACMD26 | SECURE_WRITE_MKB | - | |
| ACMD38 | SECURE_ERASE | - | |
| ACMD43 | GET_MKB | - | |
| ACMD44 | GET_MID | - | |
| ACMD45 | SET_CER_RN1 | - | |
| ACMD46 | SET_CER_RN2 | - | |
| ACMD47 | SET_CER_RES2 | - | |
| ACMD48 | SET_CER_RES1 | - | |
| ACMD49 | CHANGE_SECURE_AREA | - | |

# 7. Electrical Characteristics

## 7.1 Absolute Maximum Ratings

| | |
|---|---|
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -55°C to +125°C |
| Voltage on I/O Pin with Respect to Ground(XTSDG0x Series) | -0.3V to VDD+0.3V (<= 3.9V) |
| Voltage on I/O Pin with Respect to Ground(XTSDQ0x Series) | -0.3V to VDD+0.3V (<= 2.25V) |
| $V_{DD}$(XTSDG0x Series) | -0.3V to 3.9V |
| $V_{DD}$(XTSDQ0x Series) | -0.3V to 2.25V |

**Notes:**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 7.2 Bus Signal Line Load

The total capacitance $C_L$ of each line of the SD NAND bus is the sum of the bus master capacitance $C_{HOST}$, the bus capacitance $C_{BUS}$ itself and the capacitance $C_{CARD}$ of each card connected to this line:

$$C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$$

Where N is the number of connected SD NAND/Cards.

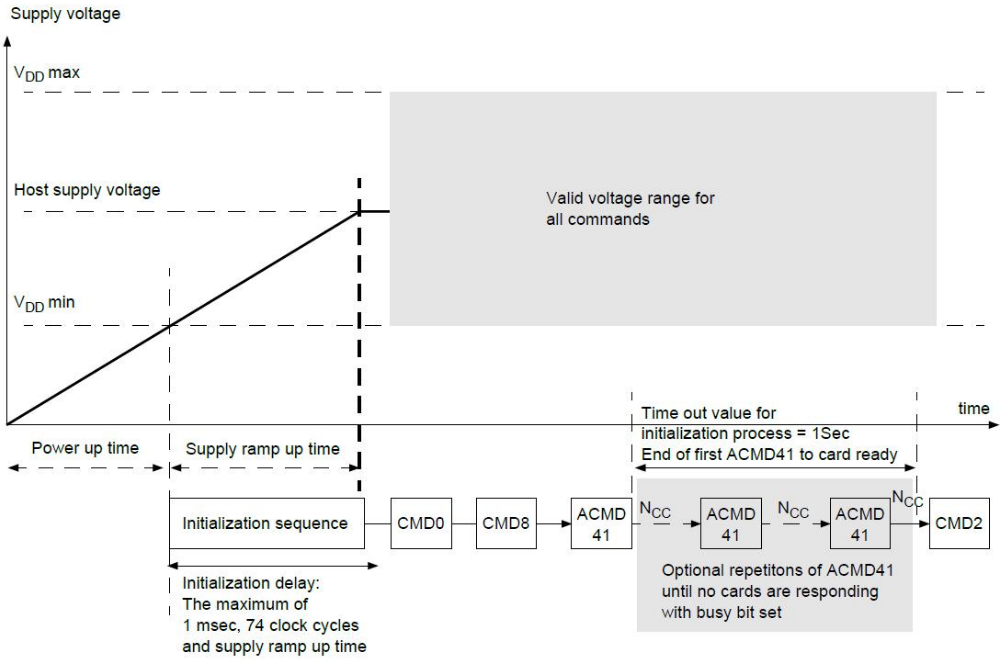
| Symbol | Parameter | Min. | Max. | Units | Remark |
|---|---|---|---|---|---|
| $C_L$ | Total bus capacitance for each signal line | | 40 | pF | $C_{HOST}+C_{BUS}$ <= 30pF |
| $C_{CARD}$ (1) | Single card capacitance | | 10 | pF | |
| $R_{CMD}$ | Pull-up resistance | 10 | 100 | K Ohm | Prevent bus floating |
| | Maximum signal line inductance | | 16 | nH | $f_{PP}$ <= 20MHz |
| $R_{DAT3}$ | Pull-up resistance inside card(pin1) | 10 | 90 | K Ohm | May be used for card detection |
| $C_C$(2) | Capacity connected to power line | | 5 | uF | To prevent inrush current |

**Notes:**

1. Characterized and is not 100% tested.
2. To limit inrush current caused by host insertion, card maximum capacitance between VDD - VSS is defined as 5uF. To support host hot insertion, the host should consider decoupling capacitor connected to power line. As SD NAND Cc is 5uF (Max.), 45uF (min.) is recommended for Decoupling capacitor.

## 7.3 Power-up

The power-up of the SD NAND bus is handled locally in each SD NAND and in the host.




Power up time is defined as voltage rising time from 0 volt to VDD(min.) and depends on application parameters such as the maximum number of SD NAND/Cards, the bus length and the characteristic of the power supply unit.

Supply ramp up time provides the time that the power is built up to the operating level (the host supply voltage) and the time to wait until the SD NAND can accept the first command.

The host shall supply power to the SD NAND so that the voltage is reached to VDD (min.) within 250ms and start to supply at least 74 SD clocks to the SD NAND with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.

After power up the SD NAND enters the idle state. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to send the card to SPI mode.

CMD8 is to support multiple voltage ranges and used to check whether the card supports supplied voltage. The host that does not support CMD8 shall supply high voltage range.

ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the SD NAND until they are out of their power-up sequence.

## 7.4 DC Electrical Characteristics

**DC Characteristics – 3.3V**

Applicable over recommended operating range from: TA =-40°C to 85°C, VDD = 2.7V to 3.6 V, (unless otherwise noted)

| SYMBOL | PARAMETER | CONDITIONS | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| VDD | Supply Voltage | | 2.7 | | 3.6 | V |
| ILI | Input Leakage Current | | -2 | | 2 | μA |
| ILO | Output Leakage Current | | -2 | | 2 | μA |
| ICC1 | Standby Current | VDD=3.6V | | 130 | 2500(2) | μA |
| ICC2 | Read Current | FCLK=50MHz | | 32 | 75 | mA |
| | Write Current | | | 32 | 75 | mA |
| VIL (1) | Input Low Voltage | | -0.3 | | 0.3VDD | V |
| VIH | Input High Voltage | | 0.7VDD | | VDD+0.3 | V |
| VOL | Output Low Voltage | IOL = 2mA $V_{DD}$ min | | | 0.4 | V |
| VOH | Output High Voltage | IOH = -2mA $V_{DD}$ min | VDD-0.3 | | | V |

**Notes:**

1. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.
2. **Standby Current at Ta=-40°C-70°C will not exceed 1300μA**.

**DC Characteristics – 1.8V**

Applicable over recommended operating range from: TA =-40°C to 85°C, VDD = 1.7V to 1.95 V, (unless otherwise noted)

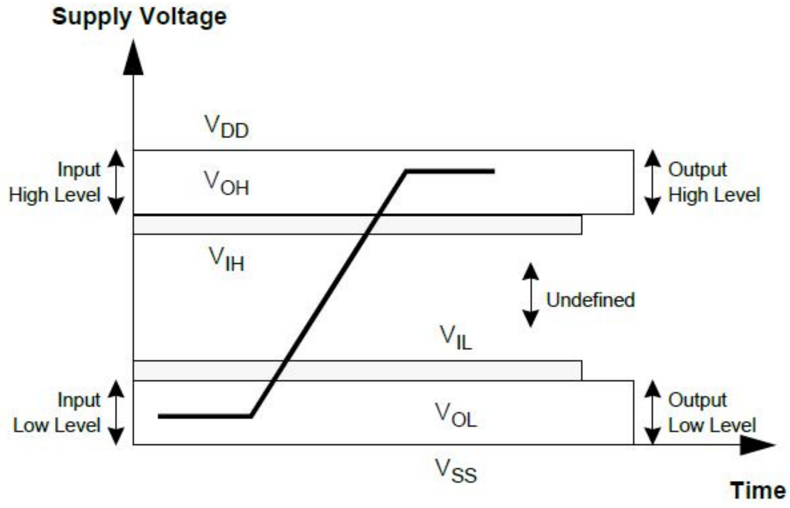
| SYMBOL | PARAMETER | CONDITIONS | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| VDD | Supply Voltage | | 1.7 | | 1.95 | V |
| ILI | Input Leakage Current | | -2 | | 2 | µA |
| ILO | Output Leakage Current | | -2 | | 2 | µA |
| ICC1 | Standby Current | VDD=1.95V | | 130 | 2500(2) | µA |
| ICC2 | Read Current | FCLK=50MHz | | 32 | 75 | mA |
| | Write Current | | | 32 | 75 | mA |
| VIL (1) | Input Low Voltage | | -0.3 | | 0.3VDD | V |
| VIH | Input High Voltage | | 0.7VDD | | VDD+0.3 | V |
| VOL | Output Low Voltage | IOL = 2mA | | | 0.4 | V |
| VOH | Output High Voltage | IOH = -2mA | VDD-0.3 | | | V |

**Notes:**

1. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.
2. **Standby Current at Ta=-40°C-70°C will not exceed 1300µA**.

## 7.5 Bus Signal Levels

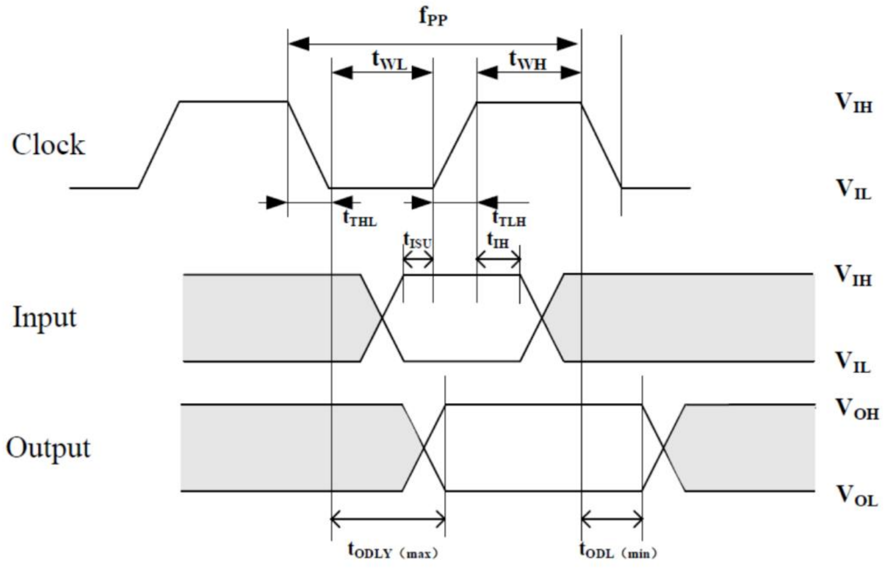
As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.




To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specified ranges for any VDD of the allowed voltage range.

## 7.6 AC Electrical Characteristics

Bus Timing (Default Mode)




Shared areas are not valid

**AC Characteristics – Default Mode – 3.3V**

Applicable over recommended operating range from: TA = -40°C to 85°C, VDD = 2.7V to 3.6V, CL = 30pF

| SYMBOL | PARAMETER | SPEC | | | UNIT |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| Clock CLK (All values are referred to min. (VIH) and max. (VIL ) | | | | | |
| $f_{PP}$ | Clock frequency Data Transfer Mode | | | 25 | MHz |
| $f_{OD}$ | Clock frequency Identification Mode | 0[1] / 100 | | 400 | KHz |
| $t_{WL}$ | Clock low time | 10 | | | ns |
| $t_{WH}$ | Clock high time | 10 | | | ns |
| $t_{TLH}$ | Clock rise time | | | 10 | ns |
| $t_{THL}$ | Clock fall time | | | 10 | ns |
| Inputs CMD, DAT (referenced to CLK) | | | | | |
| $t_{ISU}$ | Input setup time | 5 | | | ns |
| $t_{IH}$ | Input hold time | 5 | | | ns |
| Outputs CMD, DAT (referenced to CLK) | | | | | |
| $t_{ODLY}$ | Output delay time during Data Transfer Mode | 0 | | 14 | ns |
| $t_{ODLY}$ | Output delay time during Identification Mode | 0 | | 50 | ns |

**Notes:**

1.0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

### AC Characteristics – Default Mode – 1.8V

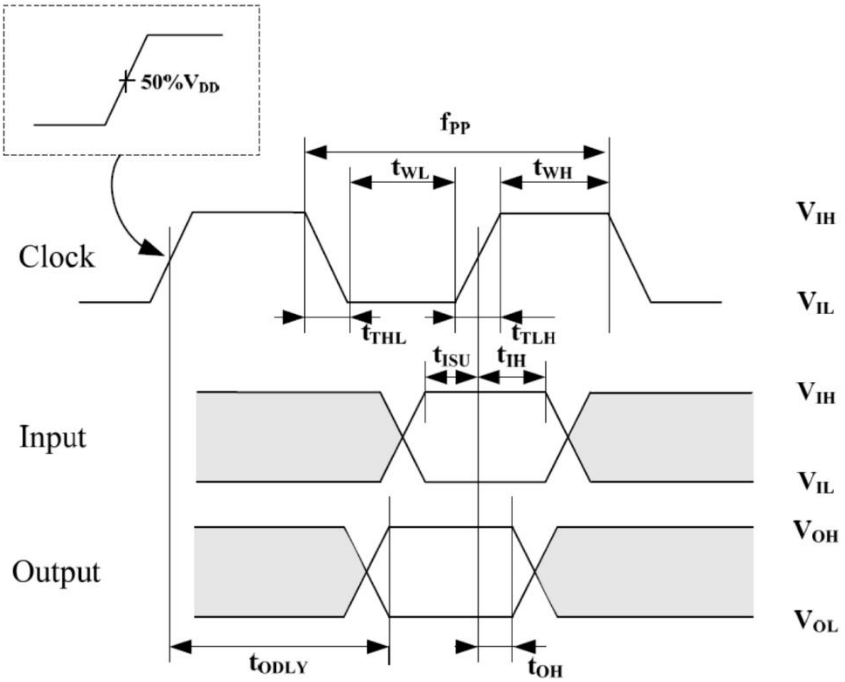
Applicable over recommended operating range from: TA = -40°C to 85°C, VDD = 1.7V to 1.95V, CL = 30pF

| SYMBOL | PARAMETER | SPEC | | | UNIT |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| Clock CLK (All values are referred to min. (VIH) and max. (VIL ) | | | | | |
| $f_{PP}$ | Clock frequency Data Transfer Mode | | | 25 | MHz |
| $f_{OD}$ | Clock frequency Identification Mode | 0[1] / 100 | | 400 | KHz |
| $t_{WL}$ | Clock low time | 10 | | | ns |
| $t_{WH}$ | Clock high time | 10 | | | ns |
| $t_{TLH}$ | Clock rise time | | | 10 | ns |
| $t_{THL}$ | Clock fall time | | | 10 | ns |
| Inputs CMD, DAT (referenced to CLK) | | | | | |
| $t_{ISU}$ | Input setup time | 5 | | | ns |
| $t_{IH}$ | Input hold time | 5 | | | ns |
| Outputs CMD, DAT (referenced to CLK) | | | | | |
| $t_{ODLY}$ | Output delay time during Data Transfer Mode | 0 | | 14 | ns |
| $t_{ODLY}$ | Output delay time during Identification Mode | 0 | | 50 | ns |

**Notes:**

1.0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

Bus Timing (High-speed Mode)




**AC Characteristics – High-Speed Mode – 3.3V**

Applicable over recommended operating range from: TA = -40°C to 85°C, VDD = 2.7V to 3.6V, CL = 30pF

| SYMBOL | PARAMETER | SPEC | | | UNIT |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| Clock CLK (All values are referred to min. (VIH) and max. (VIL ) | | | | | |
| $f_{PP}$ | Clock frequency Data Transfer Mode | | | 50 | MHz |
| $t_{WL}$ | Clock low time | 7 | | | ns |
| $t_{WH}$ | Clock high time | 7 | | | ns |
| $t_{TLH}$ | Clock rise time | | | 3 | ns |
| $t_{THL}$ | Clock fall time | | | 3 | ns |
| Inputs CMD, DAT (referenced to CLK) | | | | | |
| $t_{ISU}$ | Input setup time | 6 | | | ns |
| $t_{IH}$ | Input hold time | 2 | | | ns |
| Outputs CMD, DAT (referenced to CLK) | | | | | |
| $t_{ODLY}$ | Output delay time during Data Transfer Mode | 0 | | 14 | ns |
| $t_{OH}$ | Output Hold time | 2.5 | | | ns |
| $C_L$ | Total system capacitance for each line[1] | | | 40 | pF |

**Notes:**
1. In order to satisfy severe timing, host shall drive only one SD NAND.

**AC Characteristics – High-Speed Mode – 1.8V**

Applicable over recommended operating range from: TA = -40°C to 85°C, VDD = 1.7V to 1.95V, CL = 30pF

| SYMBOL | PARAMETER | SPEC | | | UNIT |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| Clock CLK (All values are referred to min. (VIH) and max. (VIL ) | | | | | |
| $f_{PP}$ | Clock frequency Data Transfer Mode | | | 50 | MHz |
| $t_{WL}$ | Clock low time | 7 | | | ns |
| $t_{WH}$ | Clock high time | 7 | | | ns |
| $t_{TLH}$ | Clock rise time | | | 3 | ns |
| $t_{THL}$ | Clock fall time | | | 3 | ns |
| Inputs CMD, DAT (referenced to CLK) | | | | | |
| $t_{ISU}$ | Input setup time | 6 | | | ns |
| $t_{IH}$ | Input hold time | 2 | | | ns |
| Outputs CMD, DAT (referenced to CLK) | | | | | |
| $t_{ODLY}$ | Output delay time during Data Transfer Mode | 0 | | 14 | ns |
| $t_{OH}$ | Output Hold time | 2.5 | | | ns |
| $C_L$ | Total system capacitance for each line[1] | | | 40 | pF |

**Notes:**

1. In order to satisfy severe timing, host shall drive only one SD NAND.

# 8. Part Numbering

The ordering part number is formed by a valid combination of the following

XT SDG 01G WS I G A

**Company Prefix**

XT = XTX

**Product Family**

**SDG** = 2.7~3.6V SD NAND Flash Memory
**SDQ** = 1.7~1.95V SD NAND Flash Memory

**Product Density**

**01/02G** = 1G bit/2G bit
**04/08G** = 4G bit/8G bit

**Product Package**

**WS** = WSON8 (8x6mm)
**LA** = LGA8 (6x5mm)

**Temperature & Moisture Sensitivity Level**

**I** = Industrial Level Temperature. (-40°C to +85°C), MSL3

**Green Code**

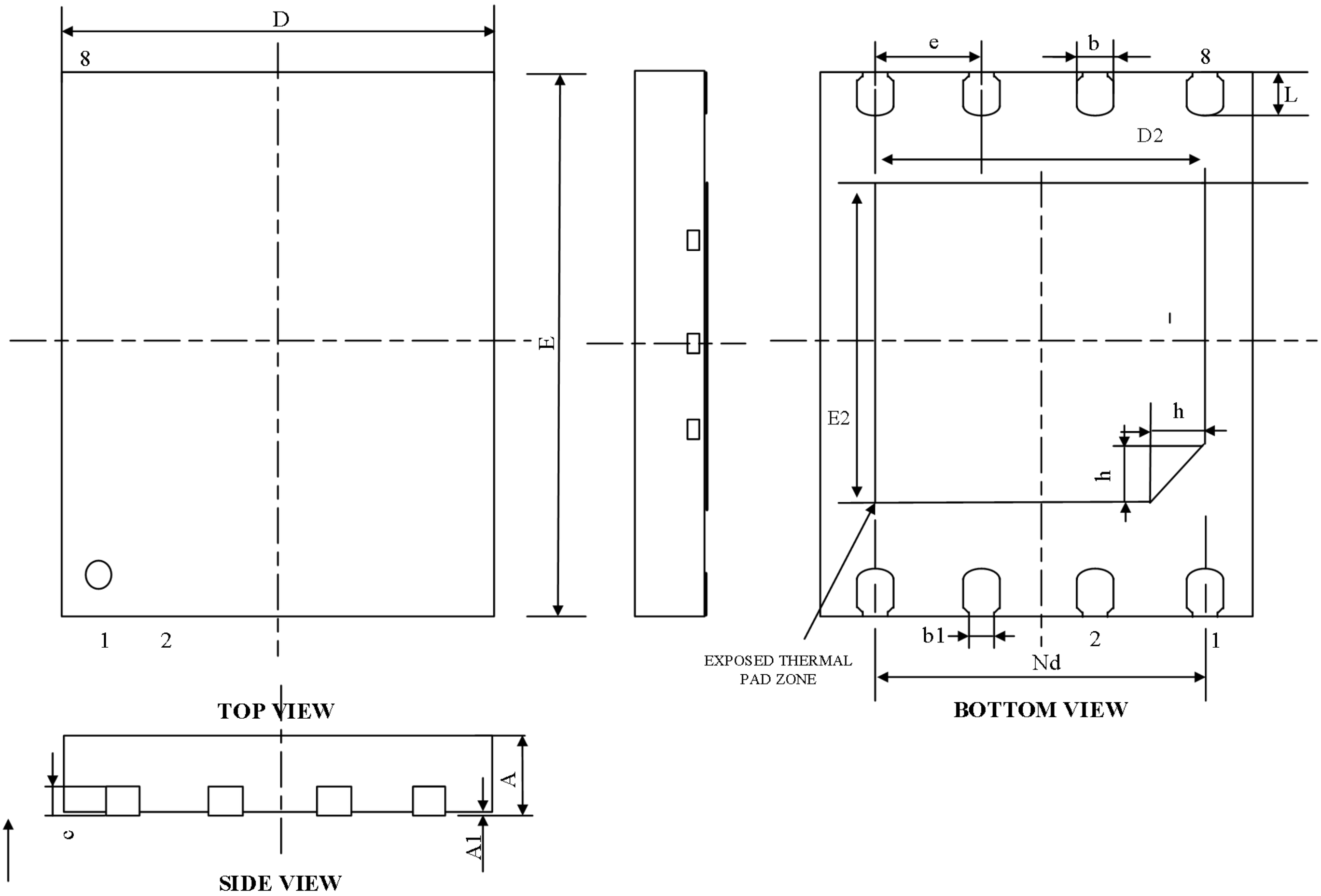
**G** = Green/Reach Package

**Product Carrier**

**U** = Tube; **T** = Tape & Reel; **A** = Tray

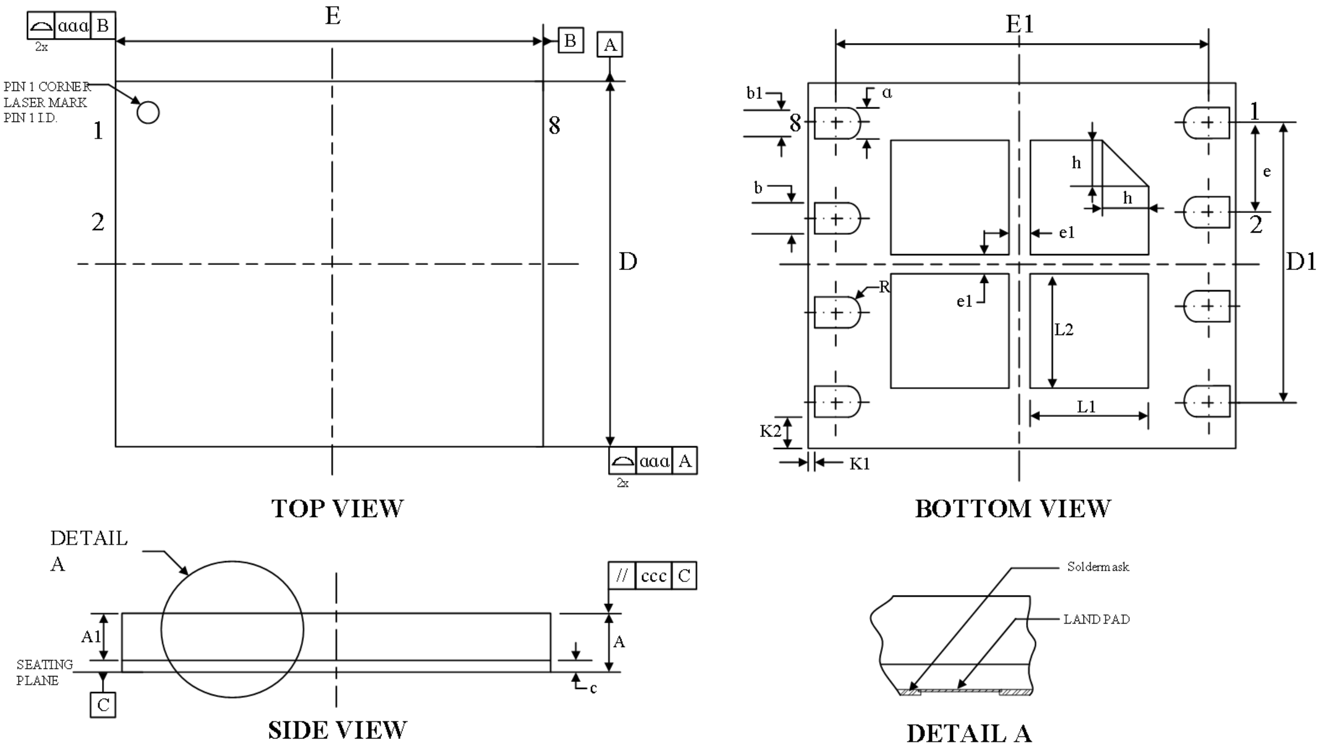
# 9. Package Information

## 9.1 Package WSON8 8x6mm




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| **A** | 0.70 | 0.75 | 0.80 |
| **A1** | 0.00 | 0.02 | 0.05 |
| **b** | 0.35 | 0.40 | 0.45 |
| **b1** | 0.25 REF | | |
| **c** | 0.18 | 0.20 | 0.25 |
| **D** | 5.90 | 6.00 | 6.10 |
| **Nd** | 3.81 BSC | | |
| **e** | 1.27 BSC | | |
| **E** | 7.90 | 8.00 | 8.10 |
| **D2** | 4.20 | 4.30 | 4.40 |
| **E2** | 3.30 | 3.40 | 3.50 |
| **L** | 0.45 | 0.50 | 0.55 |
| **h** | 0.30 | 0.35 | 0.40 |

## 9.2 Package LGA8 6x5mm




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.53 BASIC | | |
| c | 0.19 | 0.22 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| D1 | 3.81 BASIC | | |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.40 BASIC | | |
| e | 1.27 BASIC | | |
| e1 | 0.40 BASIC | | |
| a | 0.55 | 0.60 | 0.65 |
| b | 0.35 | 0.40 | 0.45 |
| b1 | 0.25 REF | | |
| L1 | 1.30 | 1.80 | 2.30 |
| L2 | 1.00 | 1.50 | 2.00 |
| h | 0.30 | 0.35 | 0.40 |
| K1 | 0.100 REF | | |
| K2 | 0.395 REF | | |
| aaa | 0.10 | | |
| ccc | 0.20 | | |

# 10. Revision History

| Revision | Description | Date |
|---|---|---|
| 0.1 | Initial version | Jul 12, 2021 |
| 0.2 | Update Standby Current Typ. value from 180uA to 130uA<br>Update Standby Current Max. value from 450uA to 710uA<br>Update Read/Write Current Typ. value from 25mA to 32mA<br>Update Read/Write Current Typ. value from 40mA to 75mA | Nov 18, 2022 |
| 0.3 | Update Standby Current Max. value from 710uA to 2500uA<br>Add 1Gb/2Gb 1.8V LGA8(6x5mm) | Jun 05, 2023 |
| 0.4 | Update XTSDG0xG VIL Max. value from 0.2VDD to 0.3VDD<br>Update XTSDG0xG VOL Max. value from 0.125VDD to 0.4<br>Update XTSDG0xG VOH Min. value from 0.75VDD to VDD-0.3 | Aug 28,2023 |
| 0.5 | Delete Interface Description<br>Modify Package WSON8 thermal pad size | Jan 25, 2024 |
| 0.6 | Modify description from “Support 4bit SD mode” to “Support 1bit/4bit SD mode”<br>Add P/E cycles and Data retention | Nov 18, 2024 |