UCS4002

USB Type-C Port Protector with Integrated VCONN FETs

Features

- Short to Battery Protection on D+, D-, and CC (24V DC)
- Integrated Switch FETs with Overvoltage, Undervoltage, Overcurrent, and Reverse Voltage Protection for Passing VCONN
- Battery Short-to-GND Protection for Charging Port
- FAULT# Assertion Configurability
- IEC 61000-4-2 ESD Protection on D+, D-, CC, and SG_SENS (±8 kV Contact; ±15 kV Air)
- Overtemperature Protection (Thermal Shutdown)
- Temperature Range: -40°C to +125°C
- AEC-Q100 Automotive Qualified, See Product Identification System

Applications

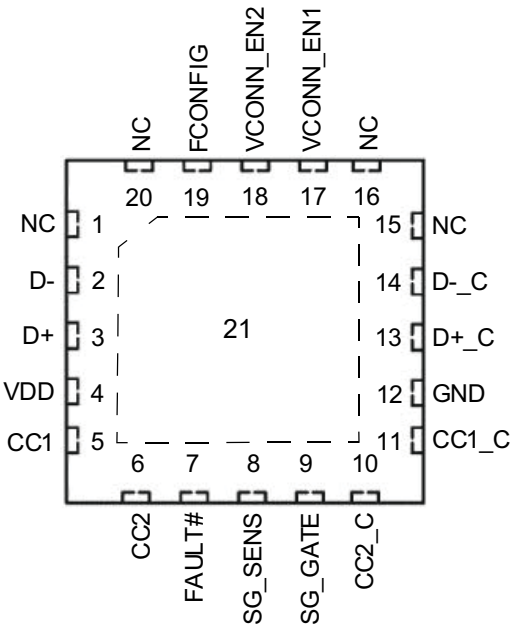
- USB Type-C
- Consumer, Industrial and Automotive Protection

Description

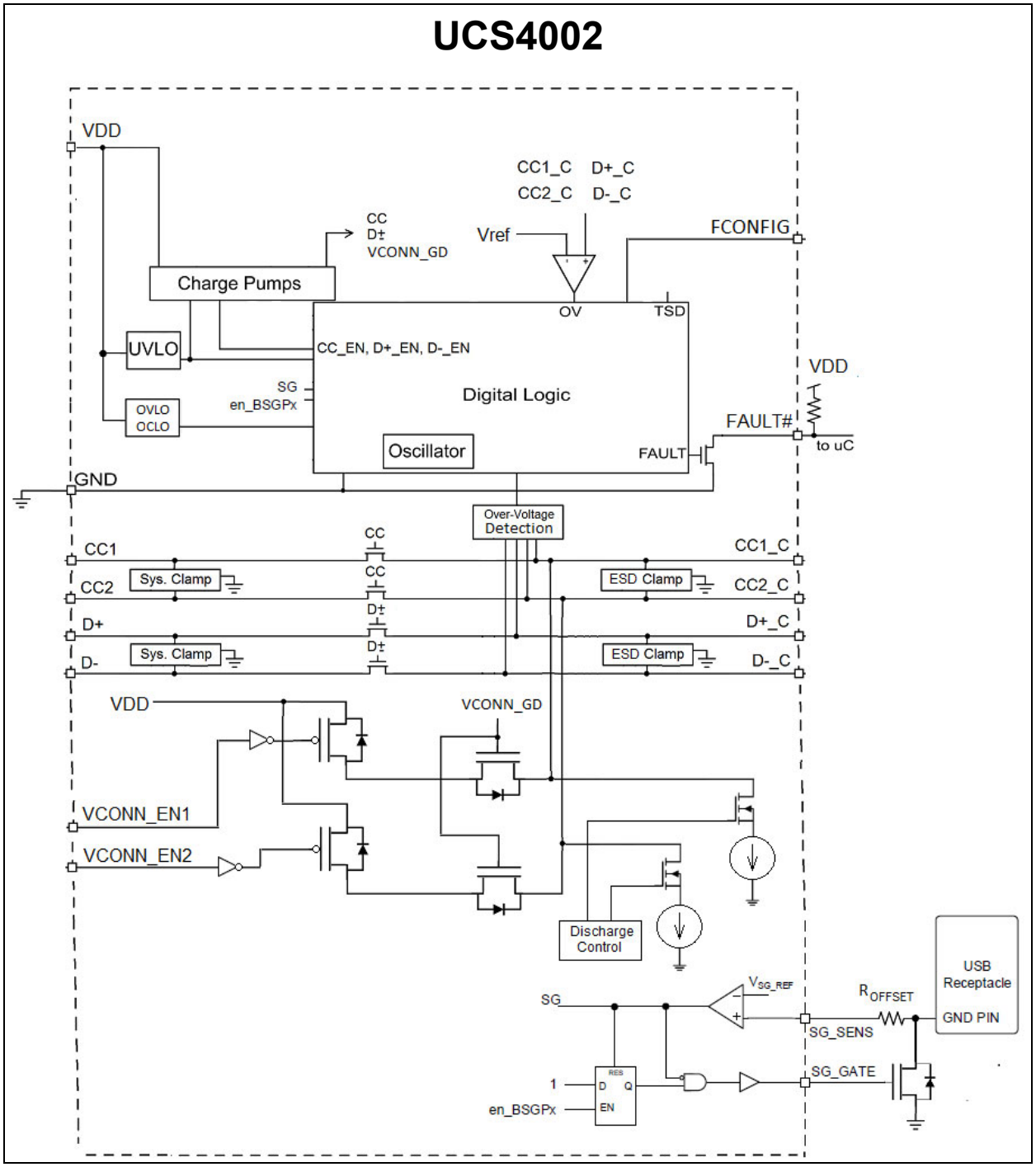
The UCS4002 is a USB Type-C port protector for Configuration Channel (CC), and D+, D- (data lines) with integrated VCONN FETs. The CC, D+, D-, and SG_SENS (short-to-GND) are ESD protected to meet IEC 61000-4-2. The UCS4002 provides short to battery protection on D+, D-, and CC. It also provides battery short-to-GND protection for the charging port. Additionally, it is configurable to assert FAULT# in case of any Fault, any Fault except VCONN back-voltage, or any Fault except D+/D- or CC overvoltage.

Package type

UCS4002
4x4 mm VQFN
(Top view)



Block Diagram



1.0 DEVICE OVERVIEW

The UCS4002 is a USB Type-C port protector for D+, D-, and CC with integrated VCONN FETs. The D+, D-, CC and SG_SENS (short-to-GND) are ESD protected to meet the IEC 61000-4-2 standard. The UCS4002 provides short to battery protection on D+, D-, and CC. The UCS4002 will also provide battery short-to-GND protection for a charging port. Additionally, the UCS4002 is configurable to assert FAULT# in case of any Fault, any Fault except VCONN back-voltage, or any Fault except D+/D- or CC overvoltage as defined in Section 1.6, FAULT Configuration (FCONFIG).

The UCS4002 protects the load on the application's VCONN from being supplied by voltages higher than intended (overvoltage lockout) and provides overcurrent protection (overcurrent lockout). Additionally, the UCS4002 implements VDD undervoltage lockout protection. It also has a thermal shutdown circuit, which will shut the port protection device off when the junction temperature exceeds the limit.

The UCS4002 is a pass-through device that will be transparent to the application and will not affect the signal integrity of the USB data lines or the intended USB application functions.

1.1 D+, D- (USB DATA LINES)

The D+_C and D-_C pins are protected against short to battery and VBUS of the USB application. As shown in Figure 1-1, when the voltage on D+_C/D-_C exceeds $V_{OVP\_D\pm}$, the pass FETs for D+, D-, CC1, CC2 and VCONN will turn OFF in $t_{OVP\_RT\_D\pm\_C}$, and the FAULT# pin will be asserted in t_{FAULT_ASSERT}. Once the voltage on D+_C/D-_C goes below $V_{OVP\_D\pm}$ minus $V_{OVP\_D\pm\_HYST}$ and $t_{OVP\_REC\_D\pm\_C}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

As shown in Figure 1-2, if the Overvoltage condition remains on D+_C/D-_C after $t_{OVP\_REC\_D\pm\_C}$ elapses, all the pass FETs will remain OFF and FAULT# will remain asserted. Once the voltage on D+_C/D-_C goes below $V_{OVP\_D\pm}$ minus $V_{OVP\_D\pm\_HYST}$ and $t_{REC\_D\pm\_C}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

Additionally, the UCS4002 implements voltage clamps after the pass FETs on the D+/D- side of the protection circuit. The purpose of these clamps is to limit the voltage on the D+/D- pins for the duration of $t_{OVP\_RT\_D\pm\_C}$ until the pass FETs are turned OFF.

1.2 CC (CONFIGURATION CHANNEL)

The CC1_C and CC2_C pins are protected against short to battery and VBUS for USB applications implementing higher than 5V on VBUS.

Figure 1-1 shows the overvoltage timing diagram for D+ and D- when the Overvoltage condition is shorter than the recovery time. This also applies to CC1_C and CC2_C by replacing D± with its corresponding CCx timing and voltage parameters. When the voltage on CC1_C/CC2_C exceeds V_{OVP_CCx}, the pass FETs for D+, D-, CC1, CC2 and VCONN will turn OFF in $t_{OVP\_RT\_CCx\_C}$, and the FAULT# pin will be asserted in t_{FAULT_ASSERT}. Once the voltage on CC1_C/CC2_C goes below V_{OVP_CCx} minus $V_{OVP\_CCx\_HYST}$ and $t_{OVP\_REC\_CCx\_C}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

Figure 1-2 shows the overvoltage timing diagram for D+ and D- when the Overvoltage condition is longer than the recovery time. This also applies to CC1_C and CC2_C by replacing D± with its corresponding CCx timing and voltage parameters. If the Overvoltage condition remains on CC1_C/CC2_C after $t_{OVP\_REC\_CCx\_C}$ has elapsed, all the pass FETs will remain OFF and FAULT# will remain asserted. Once the voltage on CC1_C/CC2_C goes below V_{OVP_CCx} minus $V_{OVP\_CCx\_HYST}$ and $t_{REC\_CCx\_C}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

Additionally, the UCS4002 implements voltage clamps after the pass FETs on the CC1/CC2 side of the protection circuit. The purpose of these clamps is to limit the voltage on the CC1/CC2 pins for the duration of $t_{OVP\_RT\_CCx\_C}$ until the pass FETs are turned OFF.

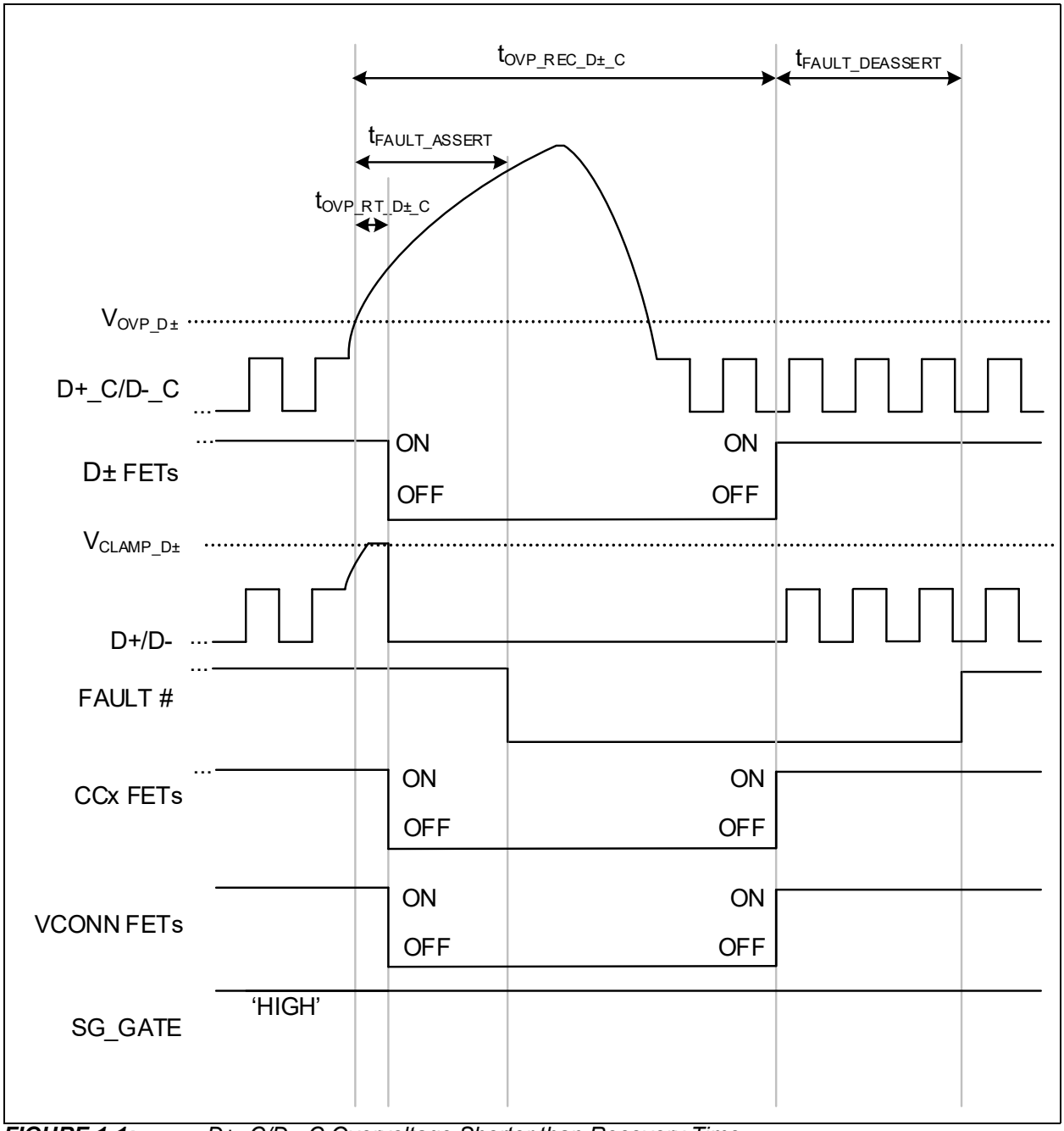


FIGURE 1-1: *D+_C/D-_C Overvoltage Shorter than Recovery Time.*

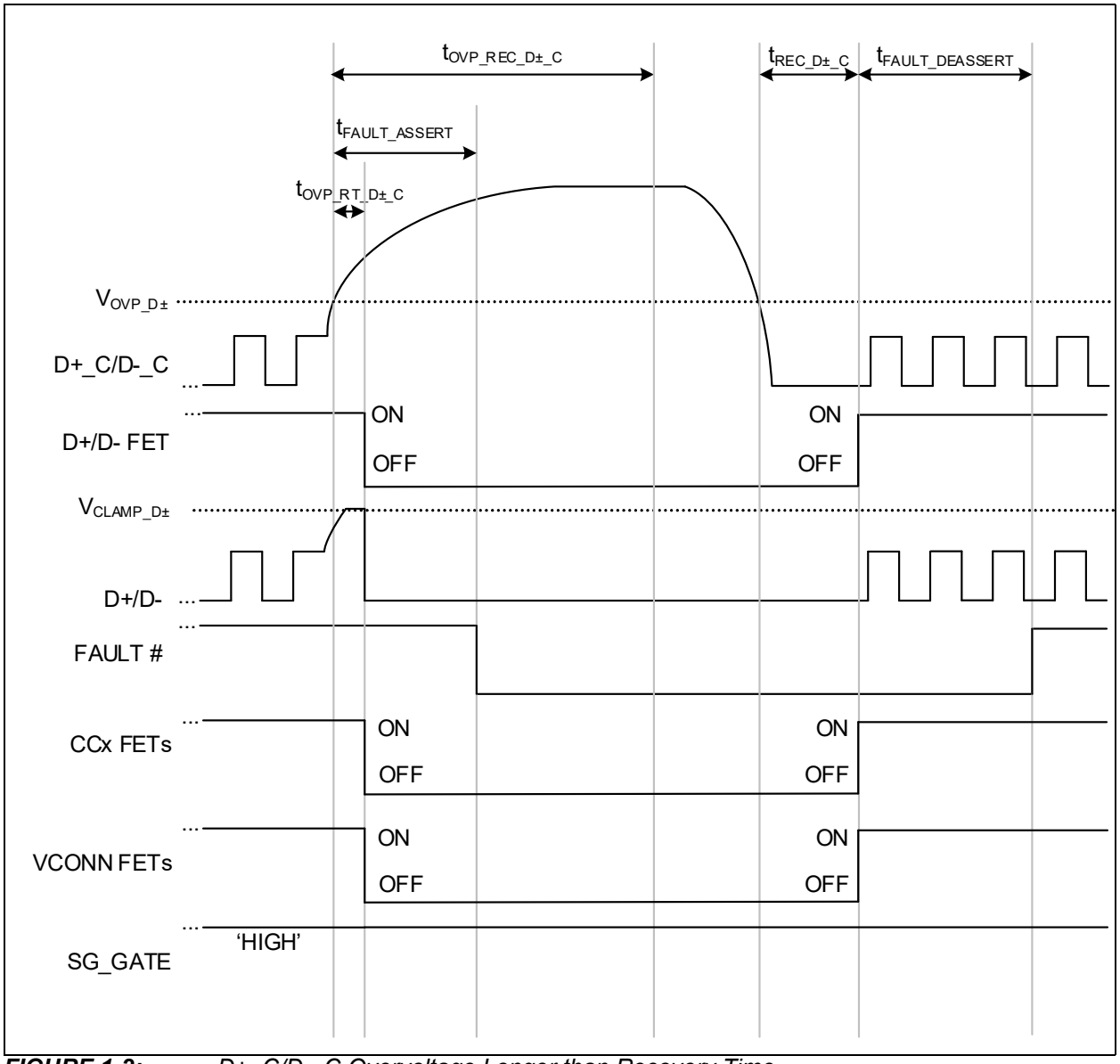


FIGURE 1-2: *D+_C/D-_C Overvoltage Longer than Recovery Time.*

1.3 SG_SENS, SG_GATE

The SG_SENS and SG_GATE are dedicated protection pins for Short-to-GND conditions on a charging port. If this protection feature is not implemented, SG_SENS must be connected to GND and SG_GATE must be left open.

An external FET and a 10 kΩ ±10% or better resistor (R_{OFFSET}) may optionally be implemented to protect against battery shorts to GND. The external FET must have an RdsON ranging from 5 mΩ to 30 mΩ (R_{FET}) and must be able to sustain I_{DS} for t_{STG_RT}. The amount of current the external FET must be able to sustain can be computed with the following formula:

$$I_{DS} = \frac{V_{DS}}{R_{FET}}$$

where the drain to source voltage (V_{DS}) on the external FET can be computed using the following formula:

$$V_{DS} = \frac{V_{BAT} \times R_{FET}}{R_{SHORT} + R_{CABLE} + R_{FET}}$$

The minimum voltage shorted to GND must be greater than 6V (V_{BAT}) in order to guarantee the short-to-GND detection. In addition to FET RdsON and minimum voltage shorted to GND, cable resistance (R_{CABLE})

must be taken into account, as well as the resistance of the short (R_{SHORT}). The following formula can then be used to compute the voltage on the SG_SENS pin:

$$V_{SG\_SENS} = R_{OFFSET} \times I_{OFFSET} + V_{DS}$$

Please refer to Figure 1-3 for the short-to-GND simplified application diagram.

As shown in Figure 1-4, when the SG_SENS pin voltage goes above V_{SG_IH}, the SG signal is asserted. The SG_GATE pin will drive low to turn OFF external FET and the pass FETs for D+, D-, CC1, CC2 and VCONN will turn OFF in t_{STG_RT}, and the FAULT# pin will be asserted in t_{FAULT_ASSERT}. Once the voltage on SG_SENS pin goes below V_{SG_IL} and t_{SG_REC} has elapsed, the UCS4002 will automatically turn all internal pass FETs back ON and drive the SG_GATE pin high to turn the external FET back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

As shown in Figure 1-5, if the Short-to-GND condition is still present after t_{SG_REC} elapses, the SG_GATE pin will remain driven low, all pass FETs will remain OFF and FAULT# will remain asserted. Once the voltage on SG_SENS goes below V_{SG_IL} and $t_{SG\_REC\_LONG}$ has elapsed, the UCS4002 will automatically turn all internal pass FETs back ON and drive the SG_GATE pin high to turn the external FET back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

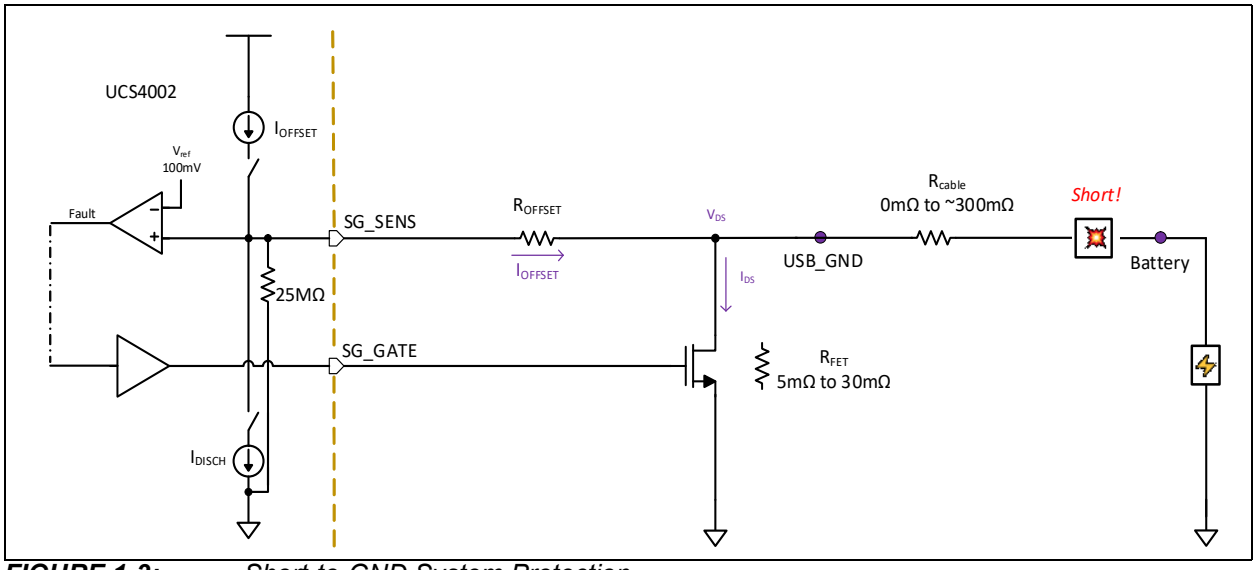


FIGURE 1-3: *Short-to-GND System Protection.*

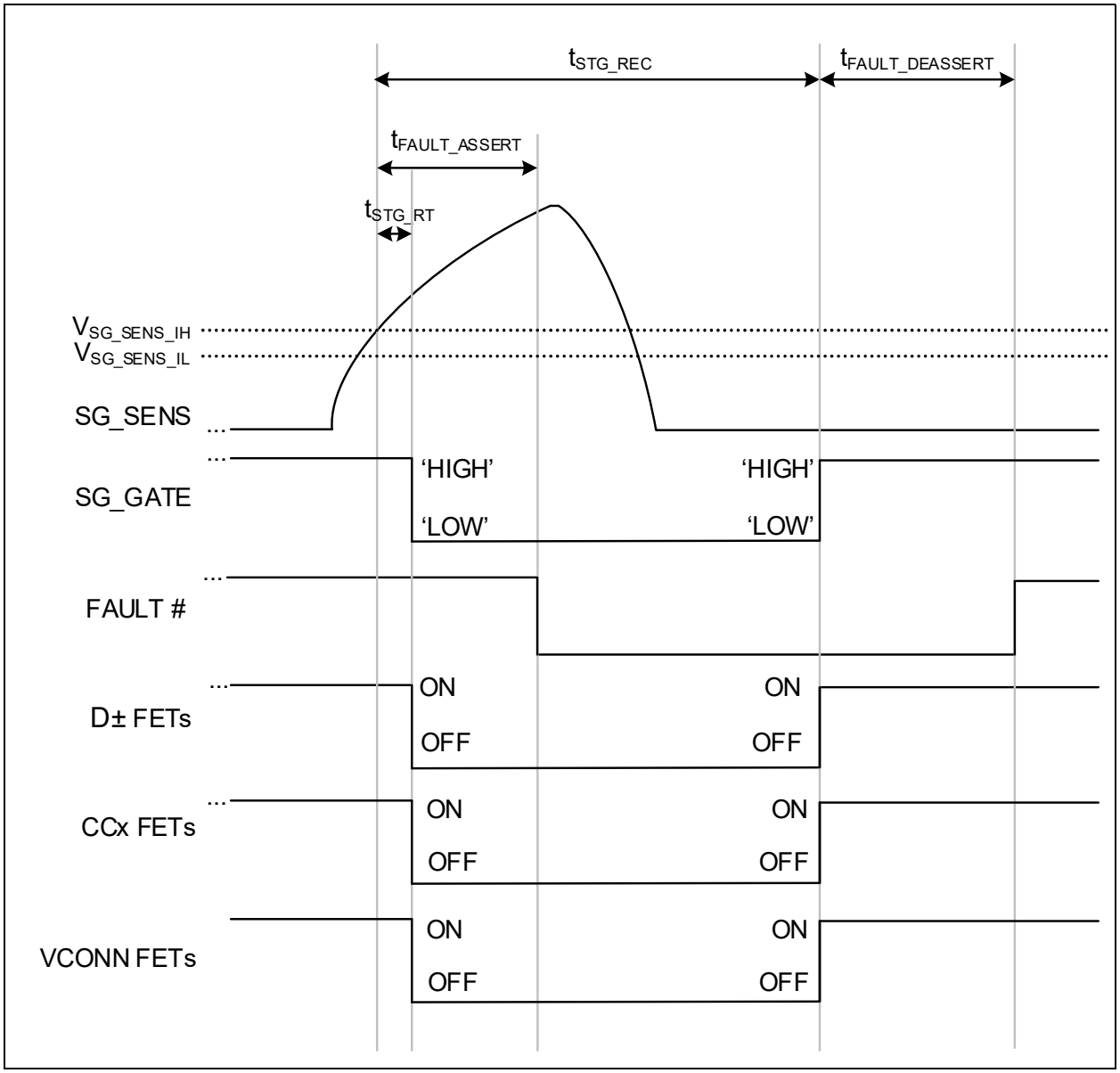


FIGURE 1-4: *Short-to-GND Shorter than Recovery Time.*

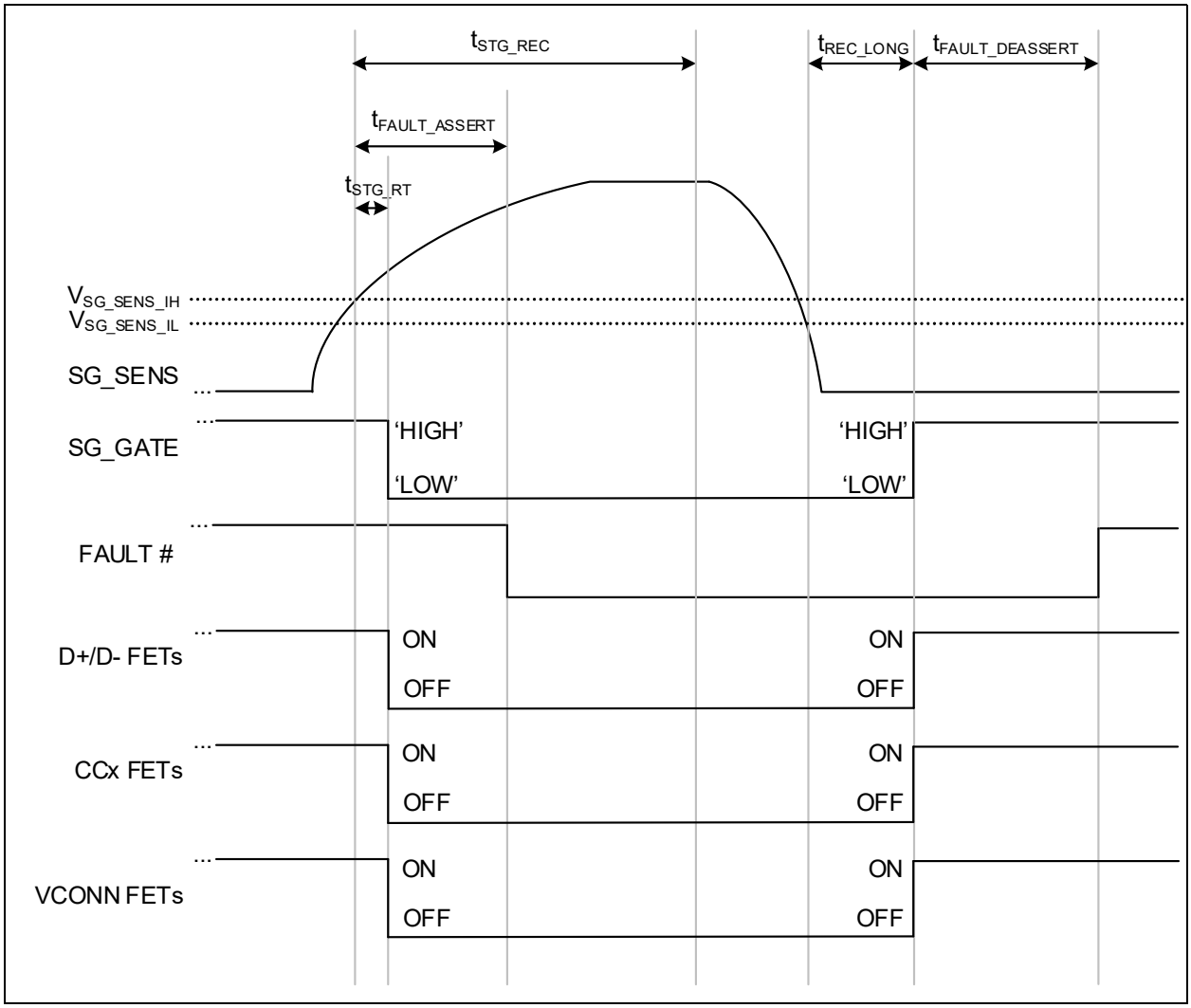


FIGURE 1-5: *Short-to-GND Longer than Recovery Time.*

1.4 VCONN (VDD)

The pass FETs from VDD to the CC1_C/CC2_C pins are controlled by the VCONN_EN1/VCONN_EN2 pins, respectively. The FETs will turn ON in t_{ON_VCONN} after the voltage on VCONN_EN1/VCONN_EN2 goes above V_{IH}. When the pass switch is turned ON, it automatically slews at a typical rate of 20V/ms to reduce inrush current. When the voltage on VCONN_EN1/VCONN_EN2 goes below V_{IL}, the pass FETs will turn OFF in t_{OFF_VCONN}.

The VCONN pass switch is protected against Overvoltage conditions on VDD. Figure 1-1 shows the overvoltage timing diagram for D+ and D- when the Overvoltage condition is shorter than the recovery time. This also applies to the VDD (VCONN) pass switch by replacing D± with its corresponding VDD (VCONN) timing and voltage parameters. When the voltage on VDD exceeds V_{DD_OVLO}, the pass FETs for D+, D-, CC1, CC2 and VCONN will turn OFF in $t_{OFF\_VCONN\_ERR}$ and the FAULT# pin will be asserted after t_{FAULT_ASSERT}. Once the voltage on VDD goes below V_{DD_OVLO} minus V_{DD_OVHYS} and $t_{ERR\_REC\_VCONN}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

Figure 1-2 shows the overvoltage timing diagram for D+ and D- when the Overvoltage condition is longer than the recovery time. This also applies to the VDD (VCONN) pass switch by replacing D± with its corresponding VDD (VCONN) timing and voltage parameters. If the Overvoltage condition remains on VDD after $t_{ERR\_REC\_VCONN}$ elapses, all the pass FETs will remain OFF and FAULT# will remain asserted. Once the voltage on VDD goes below V_{DD_OVLO} minus V_{DD_OVHYS} and t_{REC_VCONN} has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

The VCONN pass switch is also protected against Undervoltage conditions. The pass FETs for D+, D-, CC1, CC2 and VCONN will turn OFF in $t_{OFF\_VCONN\_ERR}$ after the voltage on VDD goes below V_{DD_UVLO}. Once the voltage on VDD goes above V_{DD_UVLO}, the UCS4002 will automatically turn all the pass FETs back ON when t_{ON} elapses.

There is also back-voltage protection on the VCONN pass switch. Because the reverse blocking function is required, the VCONN switch consists of one P-channel and one N-channel MOSFET back-to-back. Figure 1-1 shows the overvoltage timing diagram for D+ and D- when the Overvoltage condition is shorter than the recovery time. This also applies to the VDD (VCONN) pass switch by replacing D± with its corresponding VDD (VCONN) timing and voltage parameters. When the switch is ON and the voltage on CC1_C/CC2_C exceeds the voltage on VDD by $V_{BV\_FAULT\_ON}$, the pass FETs for D+, D-, CC1, CC2 and VCONN open in $t_{OFF\_VCONN\_ERR,}$ and the FAULT# pin is asserted in t_{FAULT_ASSERT}. Once the voltage delta between CC1_C/CC2_C and VDD is more than $V_{BV\_FAULT\_OFF}$ and $t_{ERR\_REC\_VCONN}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

Figure 1-2 shows the overvoltage timing diagram for D+ and D- when the Overvoltage condition is longer than the recovery time. This also applies to the VDD (VCONN) pass switch by replacing D± with its corresponding VDD (VCONN) timing and voltage parameters. If the Back-Voltage condition is still present after $t_{ERR\_REC\_VCONN}$ elapses, all the pass FETs will remain OFF and FAULT# will remain asserted. Once the voltage delta between CC1_C/CC2_C and VDD is less than $V_{BV\_FAULT\_OFF}$ and $t_{ERR\_REC\_VCONN}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

The VCONN pass switch is also protected against Overcurrent conditions on the VCONN pass FETs. As shown in Figure 1-6, when the current going through the VCONN FET exceeds I_{DD_OCLO}, the pass FETs for D+, D-, CC1, CC2 and VCONN will turn OFF in $t_{OFF\_VCONN\_ERR}$ and the FAULT# pin will be asserted after t_{FAULT_ASSERT}. Once $t_{ERR\_REC\_VCONN}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

After $t_{ERR\_REC\_VCONN}$ elapses and all the pass FETs are turned back ON, if the Overcurrent condition is still present (VCONN FET current exceeds I_{DD_OCLO}) all the pass FETs will turn back OFF in $t_{OFF\_VCONN\_ERR}$ and FAULT# will remain asserted.

Once $t_{ERR\_REC\_VCONN}$ has elapsed, the UCS4002 will automatically turn all the pass FETs back ON. The FAULT# pin will then be deasserted after $t_{FAULT\_DEASSERT}$ elapses.

1.5 VCONN-CCX AUTOMATIC DISCHARGE

The output discharge circuit is implemented through a current source, placed between CC1_C/CC2_C pins and ground. This current source is controlled by the corresponding VCONN_EN1/VCONN_EN2 pin, a maximum discharge timer ($t_{DISCHARGE}$), and additional digital logic to keep it OFF when the corresponding VCONN switch is closed.

1.6 FAULT CONFIGURATION (FCONFIG)

The UCS4002 allows the user to configure the FAULT# behavior via the FCONFIG pin as follows:

- **FCONFIG = GND**
  Assert FAULT# in case of any Fault
- **FCONFIG = 'OPEN'**
  Assert FAULT# in case of any Fault except VCONN back-voltage
- **FCONFIG = 'HIGH'**
  Assert FAULT# in case of any Fault except D+/D- or CC overvoltage

Although the FAULT# may not be asserted based upon the specific FCONFIG setting, the pass FETs for D+, D-, CC1, CC2 and VCONN will still turn OFF and back ON based upon the Fault condition.

1.7 Thermal Shutdown

The thermal shutdown circuit sends the TSD signal to the digital logic when the die temperature exceeds T_{TSD}. It has a hysteresis of T_{TSD_HYST}.

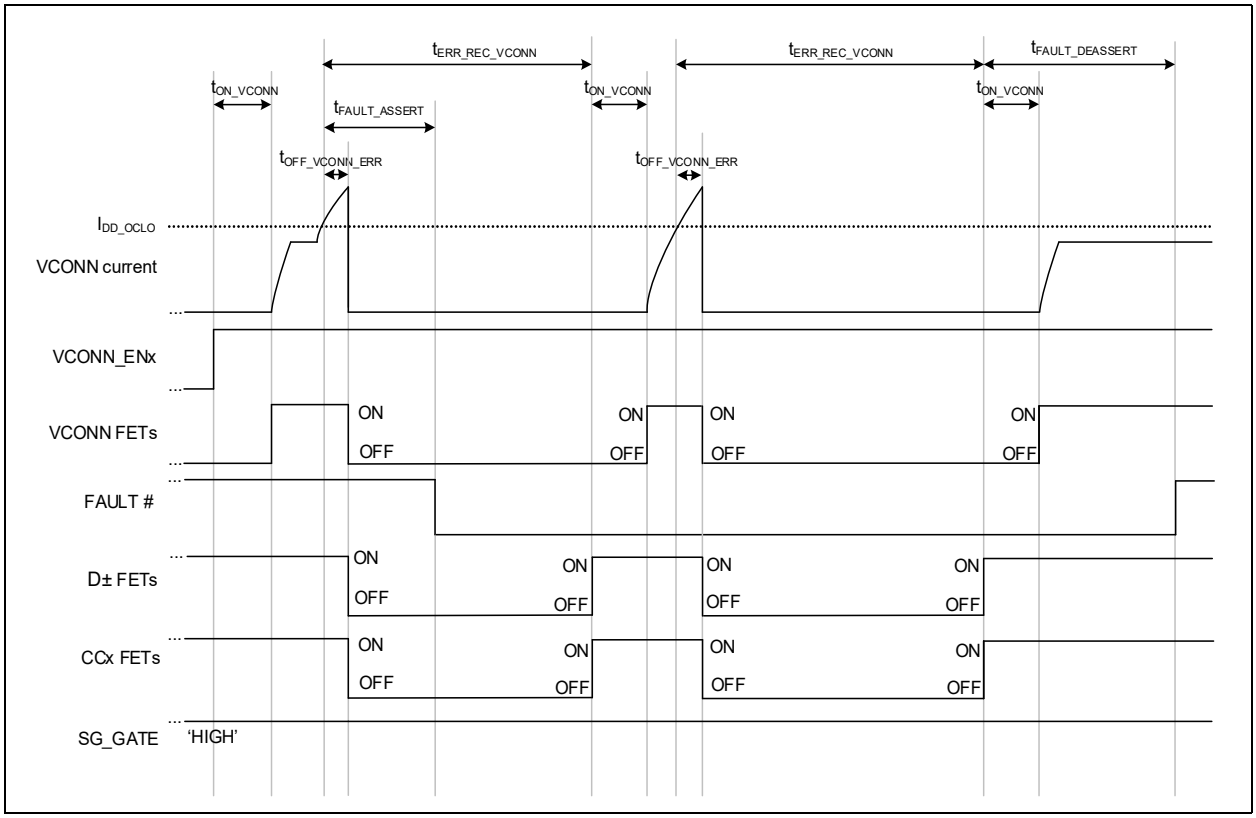


FIGURE 1-6: *VCONN FET Overcurrent.*

1.8 OPERATING MODE

When VDD is below the V_{DD_UVLO} threshold, the UCS4002 functionality is fully disabled except for the short-to-GND gate driver.

When VDD is higher than the V_{DD_UVLO} threshold, the VCONN_GD, D+, D-, and CC MOSFETs, the short-to-GND gate driver, and the Fault detection blocks are fully enabled. The UCS4002 will remain in the same power state when a Fault condition has occurred.

1.8.1 VCONN (VDD) AUTOMATIC DISCHARGE

To perform automatic discharge, the digital logic sends the DISCHG signal to connect the internal current source between the CC1_C/CC2_C pin and ground when the voltage on VCONN_EN1/VCONN_EN2 goes below V_{IL}. Once the voltage on CC1_C/CC2_C goes below V_{DISCHG} and $t_{DISCHARGE}$ has elapsed, the internal current source between the CC1_C/CC2_C pin and ground is disconnected.

The automatic discharge circuitry is also activated when the voltage on VDD goes below V_{DD_UVLO} while VCONN_EN1/VCONN_EN2 is above V_{IH}.

1.8.2 FAULT HANDLING

A Fault state means that at least one of the following conditions has occurred:

- Overvoltage (see Figure 1-7 for D+, D- example)
- Undervoltage
- Overcurrent
- VCONN Back-Voltage
- Short-to-GND
- Thermal Shutdown

The digital logic continuously monitors the comparator's outputs. Any Fault will cause the rest of the protection circuit blocks in the UCS4002 to be enabled. Example: If there is an overvoltage on D+, all the UCS4002 pass FETs will be disabled. The only protection circuit that will remain active, if implemented, is the external FET for battery short-to-GND (keeping GND connected).

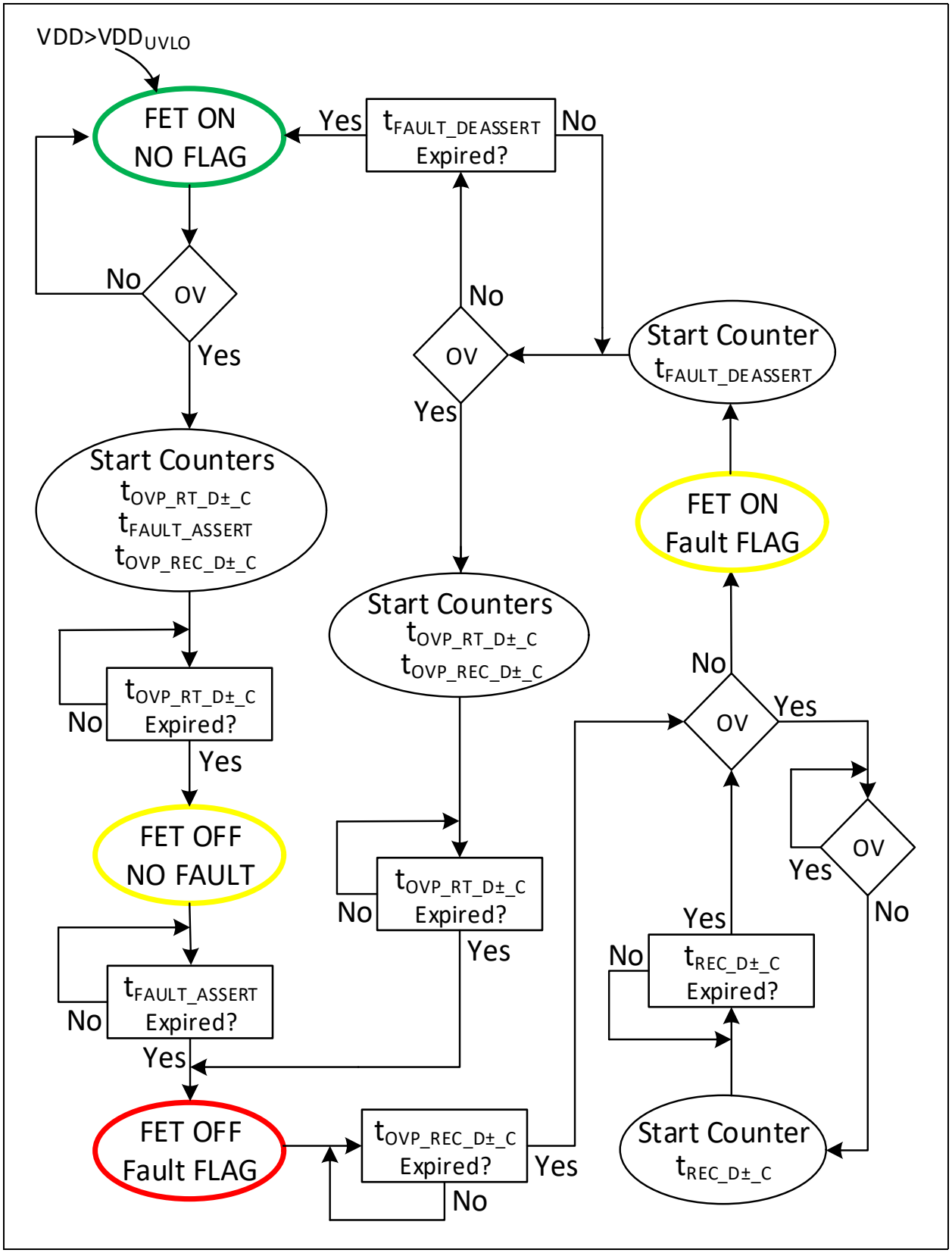


FIGURE 1-7: *D+, D- Fault Flow Chart.*

1.9 FUNCTIONAL PIN DESCRIPTIONS

The table below describes the function of each pin.

TABLE 1-1: PIN DESCRIPTION TABLE

Pin	Sym	Pin Type	Description
2	D-	I/O	Module side of the High Speed USB data line (-). This pin connects to the D- of the USB transceiver.
3	D+	I/O	Module side of the High Speed USB data line (+). This pin connects to the D+ of the USB transceiver.
4	VDD	Power	Power supply
5	CC1	I/O	Module side of the CC1 overvoltage protection FET. This pin is connected to either of the CC pins of the CC/PD Controller.
6	CC2	I/O	Module side of the CC2 overvoltage protection FET. This pin is connected to either of the CC pins of the CC/PD Controller.
7	FAULT#	Open Drain Output	A logic low state indicates a Fault condition. This pin requires an external pull-up resistor.
8	SG_SENS	I	Short-to-GND protection sense input. This pin must be grounded when protection feature not implemented.
9	SG_GATE	O	Short-to-GND protection gate drive. This pin must be left open when protection feature not implemented.
10	CC2_C	I/O	Connector side of the CC2 overvoltage protection FET. This pin is connected to either of the CC pins of the USB connector.
11	CC1_C	I/O	Connector side of the CC1 overvoltage protection FET. This pin is connected to either of the CC pins of the USB connector.
12	GND	Ground	Ground for the power supply
13	D+_C	I/O	Connector side of the High Speed USB data line (+). This pin connects to the D+ of the USB connector.
14	D-_C	I/O	Connector side of the High Speed USB data line (-). This pin connects to the D- of the USB connector.
17	VCONN_EN1	I	The CC1_C is enabled passing VCONN (VDD) when this pin is pulled high.
18	VCONN_EN2	I	The CC2_C is enabled passing VCONN (VDD) when this pin is pulled high.
19	FCONFIG	I	FAULT# assertion configuration pin. ‘low’ = FAULT# asserted in case of any fault ‘open’ = FAULT# asserted in case of any Fault except Back-Voltage condition when passing VCONN ‘high’ = FAULT# asserted in case of any Fault except D+/D- or CC overvoltage
1, 15, 16, 20	NC	Not Connected	Connect to ground
21	EP	Exposed Pad	Exposed pad is NOT electrically connected. It is recommended to connect exposed pad to ground.

1.10 Typical Applications

Figure 1-8 illustrates an example of a typical application of the UCS4002.

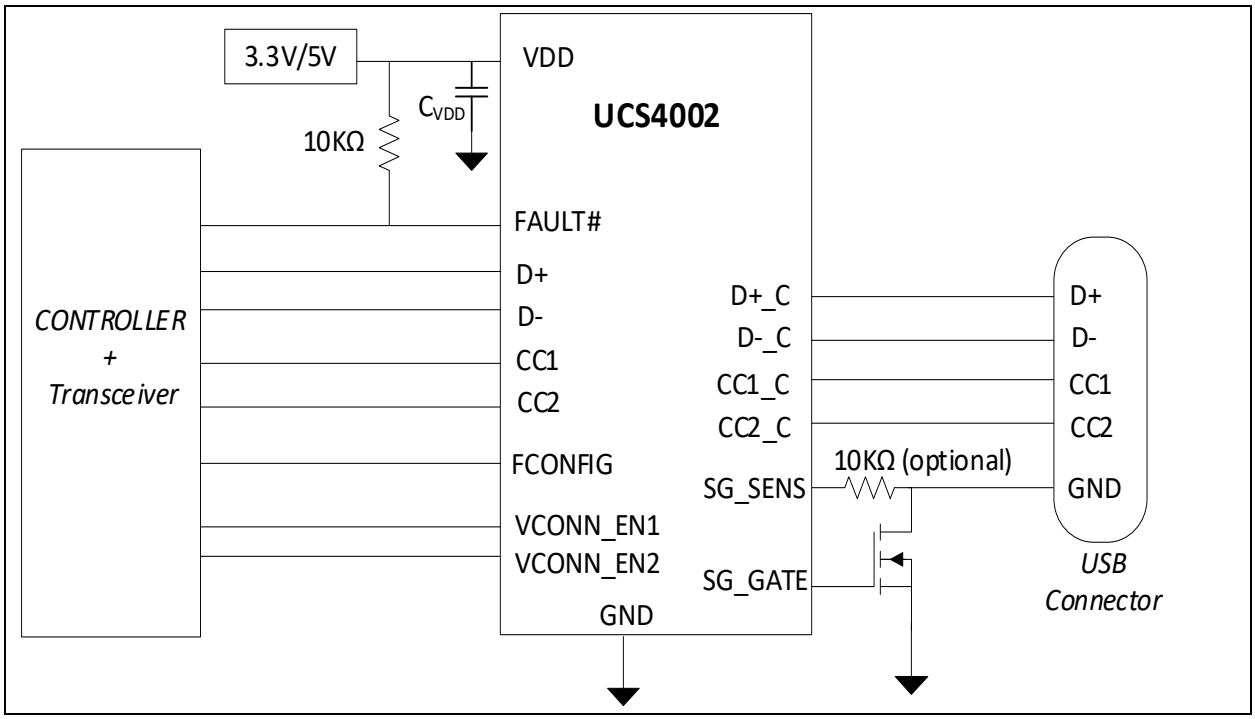


FIGURE 1-8: *Typical Application.*

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Voltage on D+_C, D-_C, CC1_C, CC2_C, SG_SENS ..... -0.3V to 25V
Voltage on any other pin to ground ..... -0.3V to 6V
VCONN switch current (internally limited) DC 0.8A
Current on the FAULT# pin ..... 10 mA
Operating junction temperature ..... -40°C to +125°C
Storage temperature range ..... -55°C to +150°C
Junction-to-Ambient Thermal resistance ..... 43°C/W
ESD protection on D+_C, D-_C, CC1_C, CC2_C, SG_SENS, GND pins
(IEC 61000-4-2) ..... ±15 kV
ESD protection on D+_C, D-_C, CC1_C, CC2_C, SG_SENS, GND pins
(JEDEC JESD22-A114; Human Body Model) ..... ±6 kV
ESD protection on all other pins (JEDEC JESD22-A114; Human Body Model) ..... ±2 kV
ESD protection on all pins (JEDEC JESD22-C101; Charge Device Model) ..... ±500V

† **NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: RECOMMENDED OPERATING CONDITIONS

Parameters	Pin/s	Min	Typ	Max	Units
Supply Voltage	VDD	2.7	—	5.5	V
Supply Voltage Capacitance		2.2	—	10	µF
USB data lines on module side voltage range	D+, D-	0	—	3.6	V
USB data lines on connector side voltage range	D+_C, D-_C	0	—	3.6	V
CC lines on module and connector side voltage range	CC1, CC2, CC1_C, CC2_C	0	—	5.5	V
VCONN enable voltage range	VCONN_EN1, VCONN_EN2	0	—	5.5	V
VCONN current capability; CCx_C	VDD	—	—	50	mA
FAULT# pull-up resistor power rail	FAULT#	2.7	—	5.5	V

TABLE 2-2: ELECTRICAL SPECIFICATIONS

T_J = -40 °C to 125 °C all typical values T_J = 25 °C, VDD = 2.7V to 5.5V unless otherwise noted.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Power						
Supply Voltage Capacitance	C_{VDD}	2.2	—	—	µF	Minimum capacitance required VDD
Operating Current	I_{DD}	—	1	2.5	mA	VDD = 5.5V VCONN_EN1 = '1' VCONN_EN2 = GND All other pins = OPEN Measure current into VDD
Under Voltage Lockout Threshold	V_{DD_UVLO}	2.1	2.3	2.5	V	Ramp up voltage on VDD until switches turn ON
Under Voltage Lockout Hysteresis	V_{UVLO_HYS}	100	150	200	mV	Ramp down voltage on VDD until switches turn OFF. Calculate delta between rise and fall voltages.
Turn-ON Time	t_{ON}	—	—	3.5	ms	Time from V_{DD_UVLO} until VCONN_GD FET, D+, D- and CC overvoltage protection FETs are ON. Note 1
Turn-OFF Slew Rate	t_{OFF_SR}	—	—	0.5	V/µs	Highest slew rate allowed to guarantee D+, D- and CC FETs turn OFF during power OFF Note 1
D+, D-, D+_C, D-_C						
On Resistance	$R_{DS\_ON\_D\pm}$	—	4	6.5	Ω	0 to 0.4V signal on D± 10 mA test current
Equivalent ON Capacitance	$C_{ON\_D\pm}$	—	5	—	pF	Capacitance across D±_C with 0V to 0.4V bias voltage when FET is ON
D±_C Overvoltage Protection	$V_{OVP\_D\pm}$	3.6	4	4.5	V	Ramp up voltage on D±_C from 3.3V to 4.5V until FAULT# is asserted
D±_C Overvoltage Protection Hysteresis	$V_{OVP\_D\pm\_HYST}$	—	50	—	mV	Ramp down voltage on D±_C until FAULT# is deasserted. Calculate delta between rise and fall voltages
ON Bandwidth (-3dB)	BW_{ON}	—	1000	—	MHz	Measure S_{21} bandwidth from D+ to D+_C or D- to D-_C with voltage swing = 400 mVpp. V_{CM}=0.2V
ON Bandwidth (-3dB) Differential	BW_{ON_DIFF}	—	1050	—	MHz	Measure S_{DD21} bandwidth from D± to D±_C with voltage swing = 800 mVpp. V_{CM} = 0.2V
Crosstalk	X_{TALK}	—	-40	—	dB	Measure S_{21} bandwidth from D+ to D-_C or D- to D+_C with voltage swing = 400 mVpp. Be sure to terminate open sides to 50 ohms. f = 480 MHz
D± Leakage Current (Powered or Unpowered)	$I_{LEAK\_D\pm}$	—	—	3	µA	VDD = 5V, D±_C = 3.5V, D± pins floating, measure leakage into D±_C pins and vice-versa
D± Leakage Current (Overvoltage)	$I_{LEAK\_D\pm\_OV}$	—	—	±1	µA	VDD = GND or 5V, D±_C = 24V, D± pins = GND. Measure leakage out of D± pins
D±_C Leakage Current (Overvoltage) Powered or Unpowered	$I_{LEAK\_D\pm\_C\_OV}$	—	—	80	µA	VDD = GND or 5V, D±_C = 24V, D± pins = GND. Measure leakage into D±_C pins

Note 1: This parameter is characterized, not 100% tested.

2: This parameter is guaranteed by design.

TABLE 2-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

T_J = -40 °C to 125 °C all typical values T_J = 25 °C, VDD = 2.7V to 5.5V unless otherwise noted.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Overvoltage Response Time	$t_{OVP\_RT\_D\pm\_C}$	—	200	—	ns	Time from overvoltage detected until OVP FETs turn OFF
Overvoltage Recovery Time	$t_{OVP\_REC\_D\pm\_C}$	10	20	30	ms	Minimum time duration after Overvoltage condition is removed until FETs turn back ON
Overvoltage Recovery Time - Long	$t_{REC\_D\pm\_C}$	—	500	—	µs	Time from removal of Overvoltage condition until OVP FETs turn ON when OVP condition is longer than $t_{OVP\_REC\_D\pm\_C}$
D± Overvoltage Clamp	$V_{CLAMP\_D\pm}$	—	8	—	V	Hot-plug 24V to D±_C with a 30Ω load on D± VDD > V_{DD_UVLO}
CC1, CC2, CC1_C, CC2_C						
On Resistance	$R_{DS\_ON\_CC}$	—	4	6.5	Ω	CCx = 3.6V 10 mA test current
CCx Leakage Current (Powered)	I_{LEAK_CC}	—	—	15	µA	VDD = 5V, CCx_C = 5.65V, CCx pins floating, measure leakage into CCx_C pins and vice-versa.
CCx Leakage Current (Overvoltage)	$I_{LEAK\_CC\_OV}$	—	—	±1	µA	VDD = GND or 5V, CCx_C = 24V, CCx pins = GND. Measure leakage out of CCx pins
CCx_C Leakage Current (Overvoltage)	$I_{LEAK\_CC\_C\_OV}$	—	—	30	µA	VDD = GND or 5V, CCx_C = 24V, CCx pins = GND. Measure leakage into CCx_C pins
CCx_C Overvoltage Protection	$V_{OVP\_CCx\_C}$	5.75	6	6.2	V	Ramp up voltage on CCx_C from 5.5 to 6.2V until FAULT# is asserted
CCx_C Overvoltage Protection Hysteresis	$V_{OVP\_CCx\_HYST}$	—	60	—	mV	Ramp down voltage on CCx_C until FAULT# is deasserted. Calculate delta between rise and fall voltages
ON Bandwidth (-3dB)	BW_{ON_CCx}	—	300	—	MHz	Measure -3dB bandwidth from CCx_C to CCx. Single ended measurement, 50Ω system. V_{cm} = 0.1V to 1.2V
Overvoltage Response Time	$t_{OVP\_RT\_CCx\_C}$	—	100	—	ns	Time from overvoltage detected until OVP FETs turn OFF.
Overvoltage Recovery Time	$t_{OVP\_REC\_CCx\_C}$	10	20	30	ms	Minimum time duration after Overvoltage condition is removed until FETs turn back ON
Overvoltage Recovery Time - Long	$t_{REC\_CCx\_C}$	—	500	—	µs	Time from removal of Overvoltage condition until OVP FETs turn ON when OVP condition is longer than $t_{OVP\_REC\_CCx\_C}$
CCx Overvoltage Clamp	V_{CLAMP_CCx}	—	8	—	V	Hot-plug 24V to CCx_C with a 30Ω load on CCx. VDD > V_{DD_UVLO}
FAULT						
FAULT# Low Level Output Voltage	V_{OL}	—	—	0.4	V	I_{SINK_IO} = 8 mA
FAULT# Assertion Time	t_{FAULT_ASSERT}	—	20	—	µs	Time from overvoltage detected to FAULT# assertion

Note 1: This parameter is characterized, not 100% tested.

2: This parameter is guaranteed by design.

TABLE 2-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

T_J = -40 °C to 125 °C all typical values T_J = 25 °C, VDD = 2.7V to 5.5V unless otherwise noted.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
FAULT# Deassertion Time	$t_{FAULT\_DEASSERT}$	—	5	—	ms	Time from FET turn ON after an OVP event to FAULT# deassertion.
VDD (VCONN Switch)						
On Resistance	$R_{DS\_ON\_VCONN}$	—	3	6	Ω	5.5V on VDD 10 mA test current Measured from VDD pin to CCx_C
Overvoltage Lockout Threshold	V_{DD_OVLO}	5.6	5.7	5.8	V	Ramp up voltage on VDD until VCONN FET OFF
Overvoltage Lockout Hysteresis	V_{DD_OVHYS}	45	75	125	mV	Ramp down voltage on VDD until VCONN FET ON. Calculate delta between rise and fall voltages
Overcurrent Lockout Threshold	I_{DD_OCLO}	40	—	70	mA	Ramp up current on VDD with VCONN_ENx 'HIGH' until VCONN FET OFF
Back-Voltage Fault Protection Threshold	$V_{BV\_FAULT\_ON}$	10	60	100	mV	VDD > V_{DD_UVLO} Switch turned OFF when $V_{BV\_FAULT\_ON}$ = = (CC1_C/CC2_C – VDD)
Back-Voltage Re-Enable Threshold	$V_{BV\_FAULT\_OFF}$	—	20	45	mV	VDD > V_{DD_UVLO} Switch turned ON when $V_{BV\_FAULT\_OFF}$ = = (CC1_C/CC2_C – VDD)
Discharge Current	I_{DISCHG}	—	5	—	mA	
Discharge Voltage Level	V_{DISCHG}	—	0.6	—	V	
Turn Off Time	$t_{OFF\_VCONN\_ERR}$	—	6	—	µs	Time from TSD to VCONN switch OFF
		—	1	—	µs	Time from OC to VCONN switch OFF
		—	100	—	ns	Time from OV or BV to VCONN switch OFF
Maximum Discharge Time	$t_{DISCHARGE}$	—	20	35	ms	Amount of time discharge internal current source applied (I_{DISCHG}) VCONN_EN1/VCONN_EN2 < V_{IL}
Turn ON Delay	t_{EN_VCONN}	—	0.5	—	ms	Time from the transition of VCONN_EN1/VCONN_EN2 from low to high until VCONN switch is ON (CC1_C/CC2_C > 600 mV)
Turn ON Time	t_{ON_VCONN}	—	—	1	ms	Time from the transition of VCONN_EN1/VCONN_EN2 from low to high until VCONN switch is fully ON (CC1_C/CC2_C > 90% of VDD)
VCONN Error Recovery Time	$t_{ERR\_REC\_VCONN}$	10	20	30	ms	Time from TSD, OV, BV, OC event to VCONN switch ON
VCONN Error Recovery Time - Long	t_{REC_VCONN}	—	500	—	µs	Time from removal of Overvoltage condition until pass FETs turn ON when error condition is longer than $t_{ERR\_REC\_VCONN}$

Note 1: This parameter is characterized, not 100% tested.

2: This parameter is guaranteed by design.

TABLE 2-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

T_J = -40 °C to 125 °C all typical values T_J = 25 °C, VDD = 2.7V to 5.5V unless otherwise noted.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Turn OFF Delay	t_{OFF_VCONN}	—	—	230	µs	Time from the transition of VCONN_EN1/VCONN_EN2 from high to low until VCONN switch OFF (CC1_C/CC2_C < VDD – 600 mV) VDD = 5V, NO C_{OUT}
VCONN_EN1, VCONN_EN2						
Input High Voltage	V_{IH}	2	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.7	V	
Input High, Low Voltage Hysteresis	$V_{IH\_IL\_HYS}$	—	200	—	mV	
Leakage Current	I_{LEAK}	—	—	±7	µA	VCONN_ENx = 0V VCONN_ENx = 5.5V
FCONFIG						
Input High Voltage	V_{IH}	VDD – 1	—	—	V	Note 2
Input Low Voltage	V_{IL}	—	—	1	V	Note 2
Leakage Current	$I_{FCONFIG\_LEAK}$	—	—	±20	µA	FCONFIG = 0V FCONFIG = 5.5V
SG_SENS, SG_GATE						
Short-to-GND Sense	$V_{SG\_SENS\_IH}$	90	—	—	mV	Ramp up SG_SENS from 10 mV to 150 mV until SG_GATE < $V_{SG\_GATE\_OL}$
Short-to-GND Release	$V_{SG\_SENS\_IL}$	—	—	80	mV	Ramp down SG_SENS from 120 mV to 0 mV until SG_GATE > $V_{SG\_GATE\_OL}$
SG_SENS Bias Current	I_{OFFSET}	—	5		µA	Current coming out of SG_SENS
SG_SENS Discharge Current	I_{DISCH}	0.4	6	15	µA	Current coming into SG_SENS
SG_GATE Output Low Voltage	$V_{SG\_GATE\_OL}$	—	—	0.4	V	I_{OL} = 8 mA SG_GATE
Short-to-GND Response Time	t_{STG_RT}	—	500	—	ns	Time from short-to-GND detected until SG_GATE < $V_{SG\_GATE\_OL}$
Short-to-GND Recovery Time	t_{SG_REC}	10	20	30	ms	Minimum time duration after Short-to-GND condition is removed until SG_GATE > $V_{SG\_GATE\_OL}$
Short-to-GND Recovery Time - Long	t_{REC_LONG}	—	500	—	µs	Time from removal of Short-To-GND condition until SG_GATE driven ‘high’ when Short-to-GND condition is longer than t_{SG_REC}
Thermal						
Thermal Shutdown Threshold	T_{TSD}	—	145	—	°C	Die Temperature at which ALL of the UCS4002 switches will turn OFF Note 1
Thermal Shutdown Hysteresis	T_{TSD_HYST}	—	40	—	°C	After shutdown due to T_{TSD} being reached, die temperature drop required before the UCS4002 can be turned ON again Note 1

Note 1: This parameter is characterized, not 100% tested.

2: This parameter is guaranteed by design.

3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables shown following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

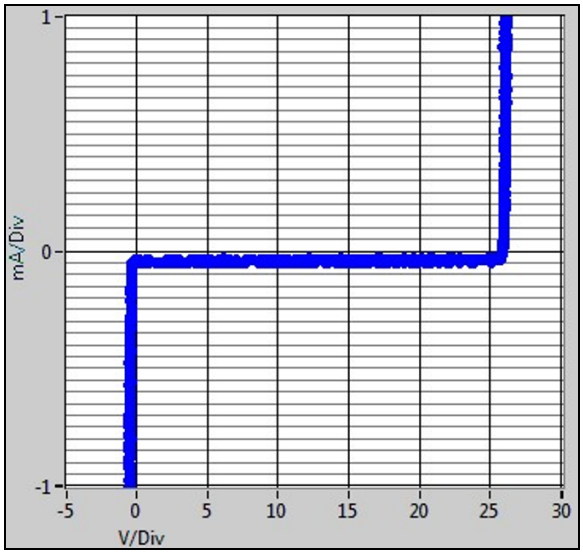


FIGURE 3-1: *D±_C I-V Curve.*

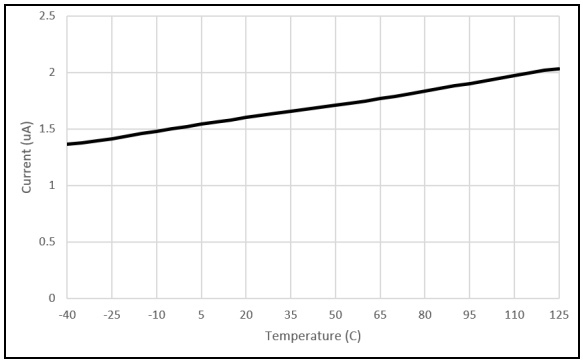


FIGURE 3-2: *D±_C Short-to-5V across Temperature (Powered).*

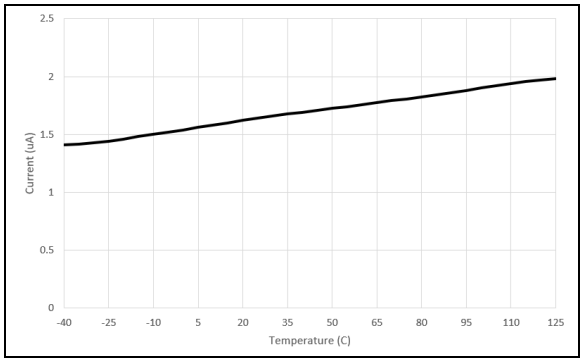


FIGURE 3-3: *D±_C Short-to-5V across Temperature (Unpowered).*

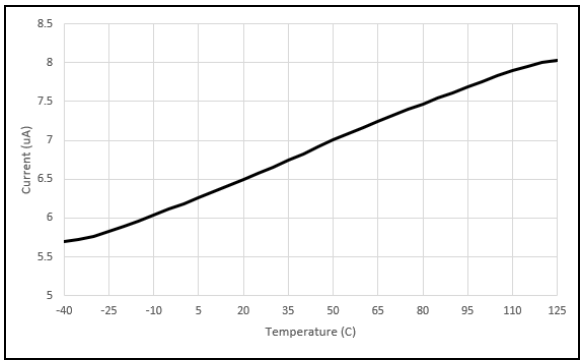


FIGURE 3-4: *D±_C Short-to-20V across Temperature (Powered).*

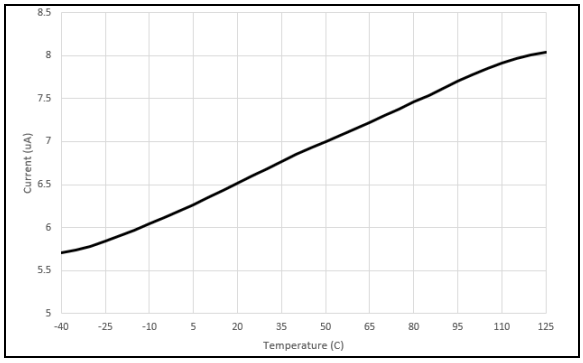


FIGURE 3-5: *D±_C Short-to-20V across Temperature (Unpowered).*

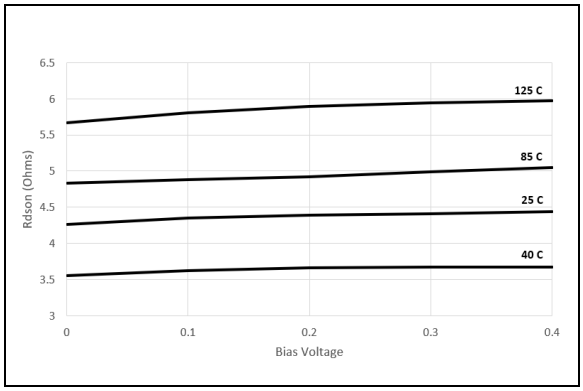


FIGURE 3-6: *D± R_ON vs Bias Voltage.*

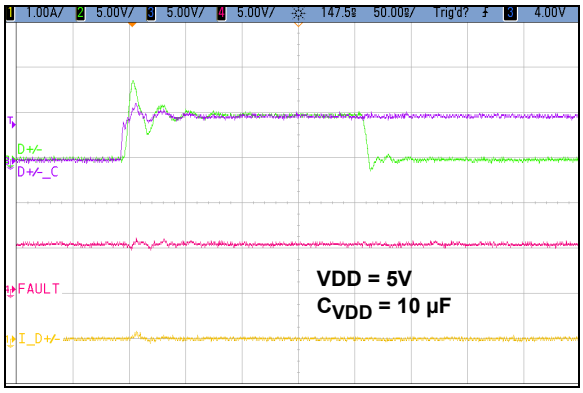


FIGURE 3-7: *D± Short-to-5V Response Waveform.*

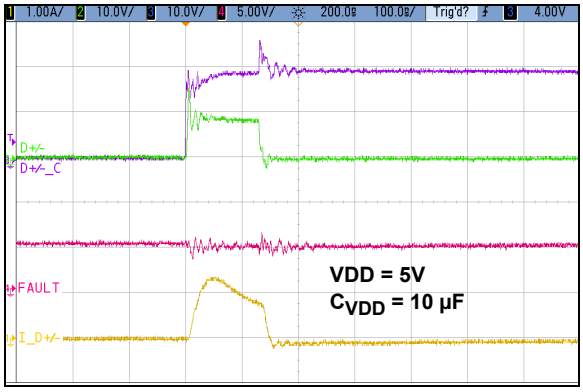


FIGURE 3-8: *D± Short-to-20V Response Waveform.*

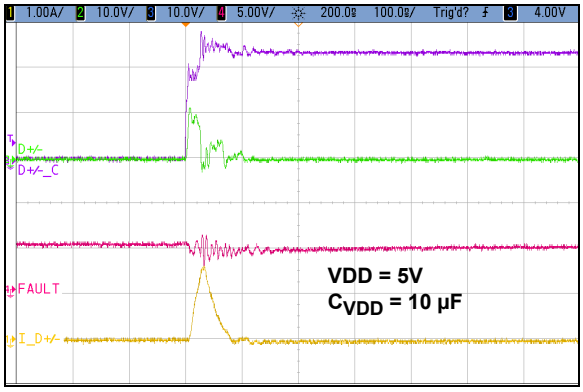


FIGURE 3-9: *D± Short-to-24V Response Waveform.*

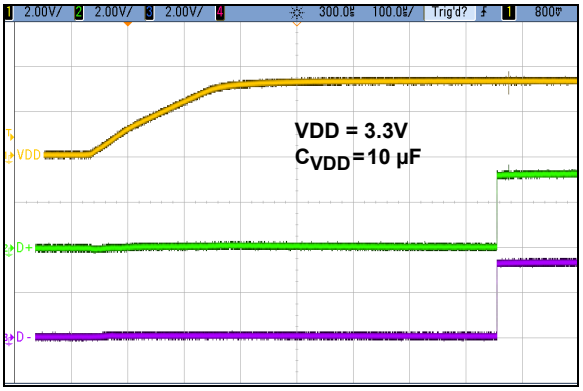


FIGURE 3-10: *Soft Start Turn ON: D+/-.*

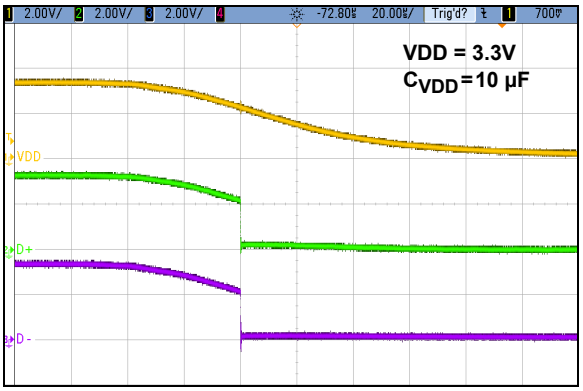


FIGURE 3-11: *Soft Start Turn OFF: D+/-.*

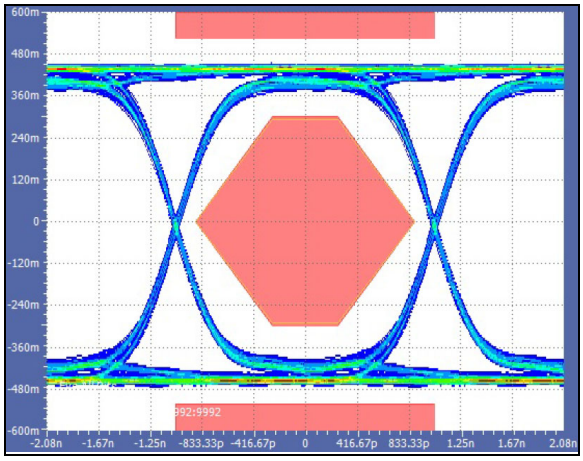


FIGURE 3-12: *USB 2.0 High-Speed Eye Diagram without UCS4002.*

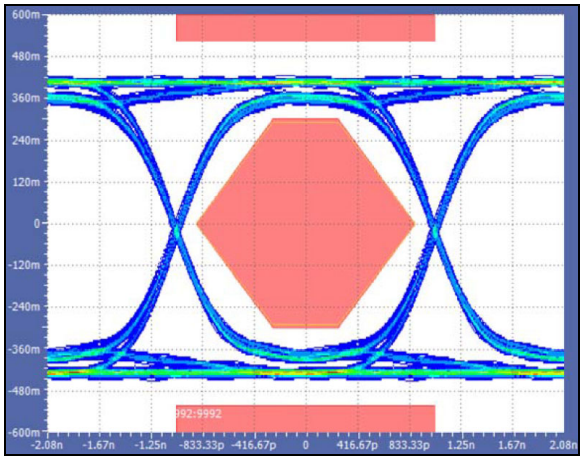


FIGURE 3-15: *USB 2.0 High-Speed Eye Diagram with UCS4002.*

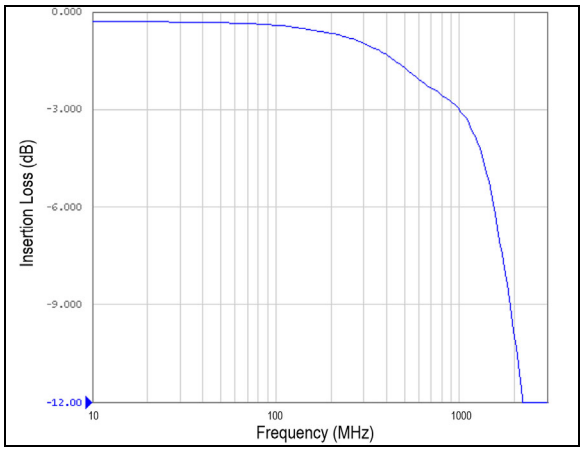


FIGURE 3-13: *D+/- Single-Ended Bandwidth.*

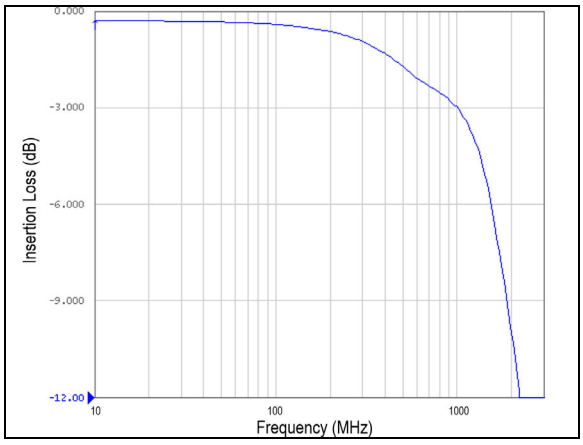


FIGURE 3-16: *D+/- Differential Bandwidth.*

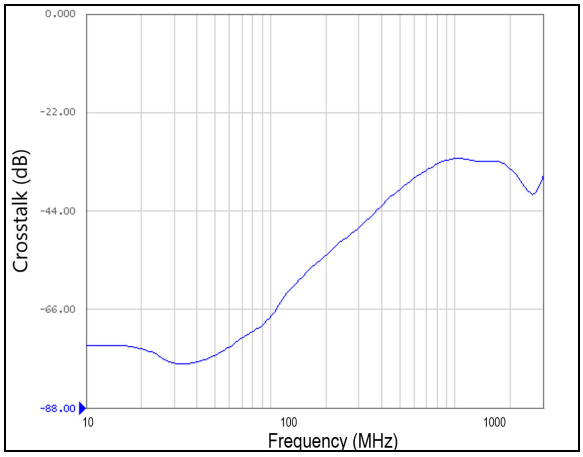


FIGURE 3-14: *D+/- Crosstalk.*

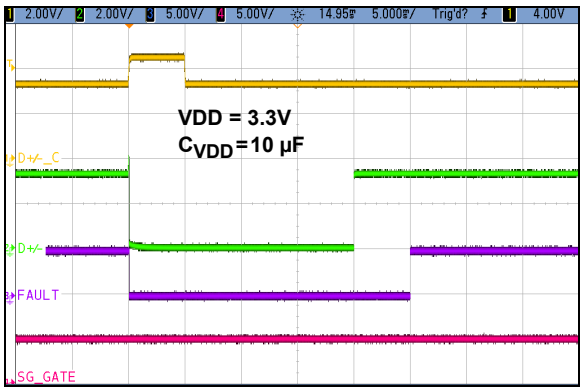


FIGURE 3-17: *D+/-_C Overvoltage.*

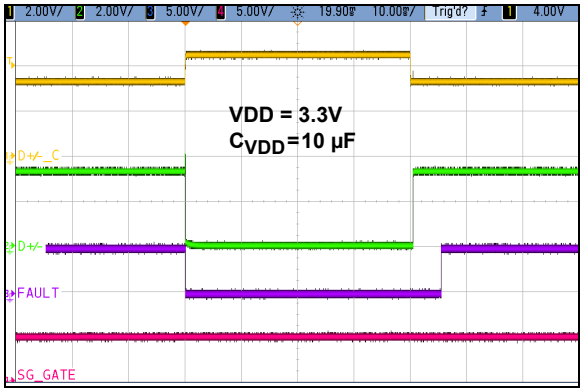


FIGURE 3-18: *D+/-_C Overvoltage Long.*

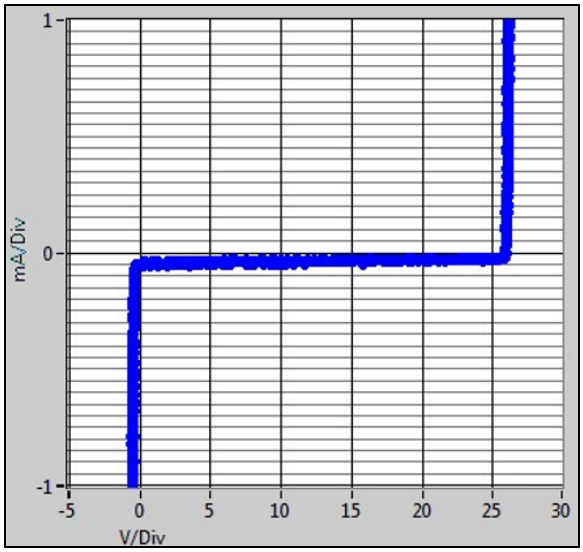


FIGURE 3-19: *CC1/CC2 I-V Curve.*

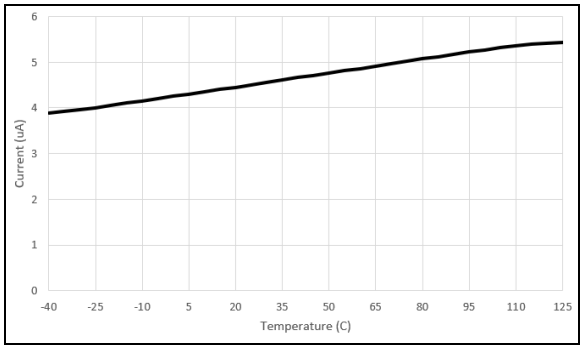


FIGURE 3-20: *CC1_C/CC2_C Short-to-5.5V Across Temperature (Powered).*

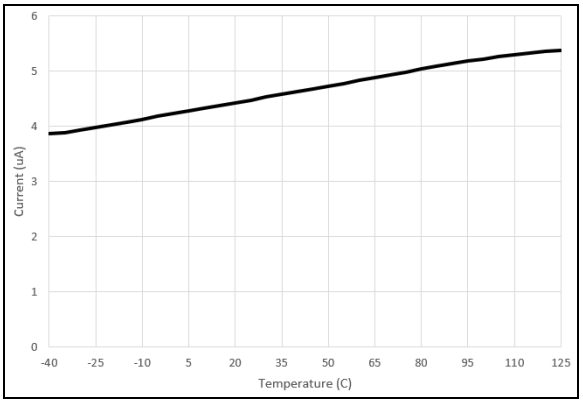


FIGURE 3-21: *CC1_C/CC2_C Short-to-5.5V Across Temperature (Unpowered).*

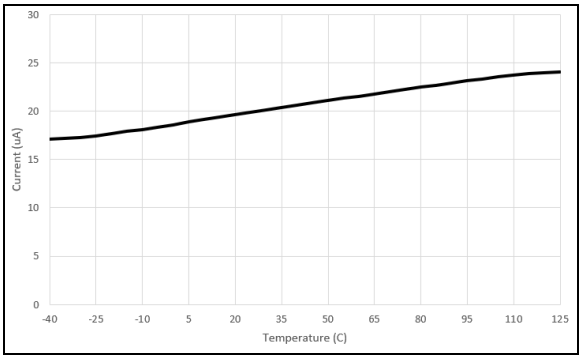


FIGURE 3-22: *CC1_C/CC2_C Short-to-24V Across Temperature (Powered).*

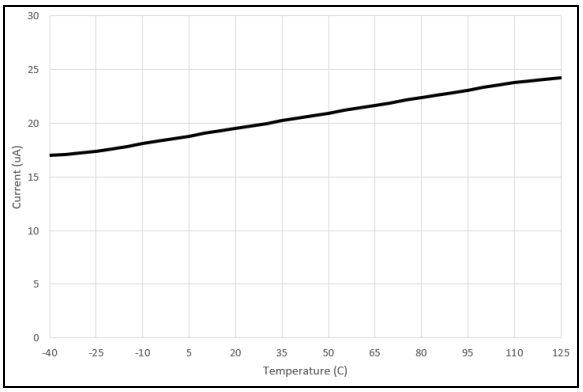


FIGURE 3-23: *CC1_C/CC2_C Short-to-24V Across Temperature (Unpowered).*

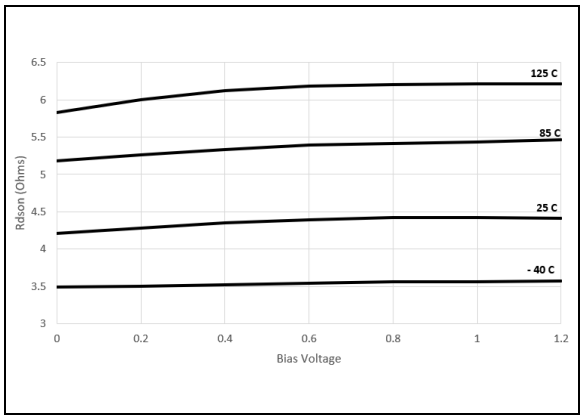


FIGURE 3-24: *CC1, CC2 R_ON vs Bias Voltage.*

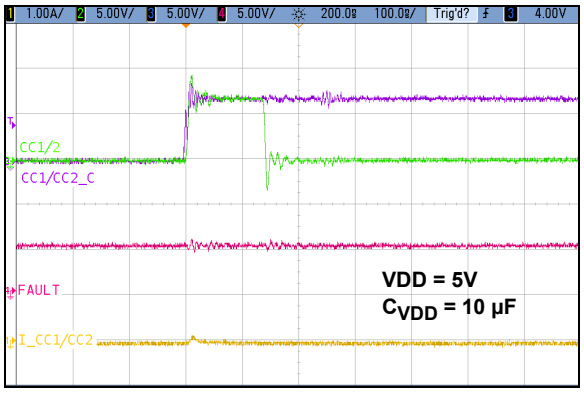


FIGURE 3-25: *CC1, CC2 Short-to-7V Response Waveform.*

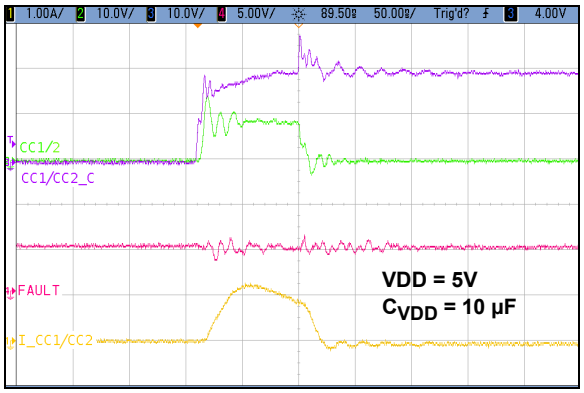


FIGURE 3-26: *CC1, CC2 Short-to-20V Response Waveform.*

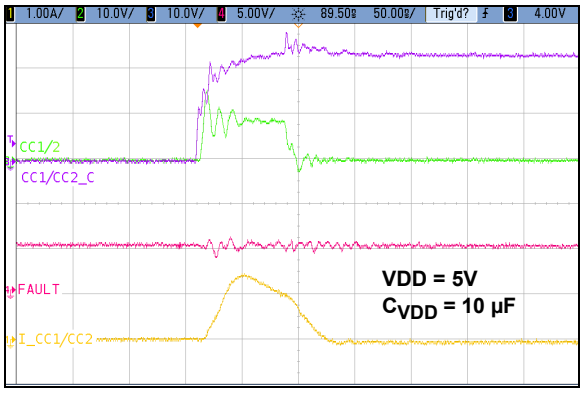


FIGURE 3-27: *CC1, CC2 Short-to-24V Response Waveform.*

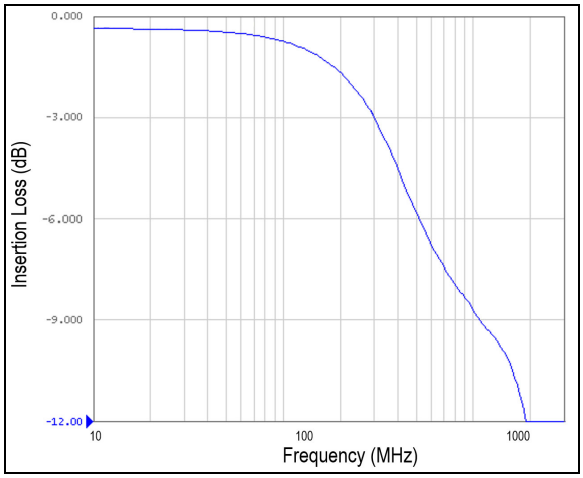


FIGURE 3-28: *CC1, CC2 Bandwidth.*

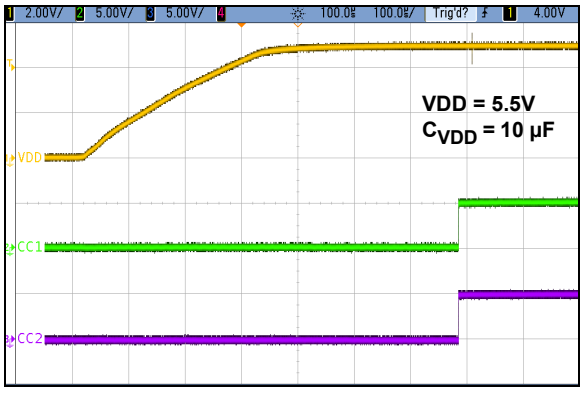


FIGURE 3-29: *Soft Start Turn ON: CC1, CC2.*

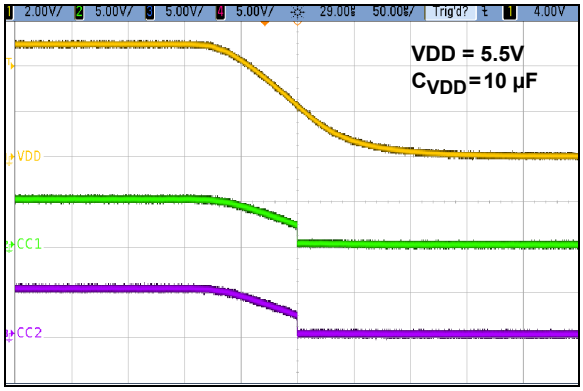


FIGURE 3-30: *Soft Start Turn OFF: CC1, CC2.*

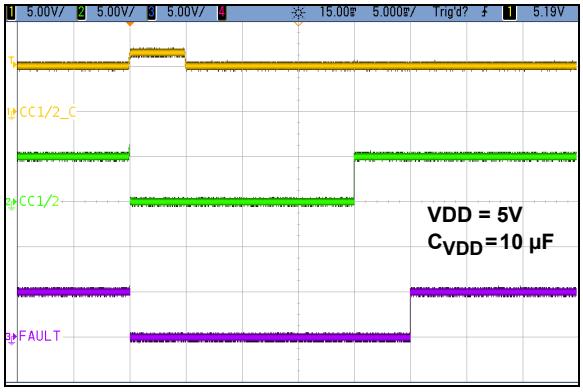


FIGURE 3-31: *CC1_C, CC2_C Overvoltage.*

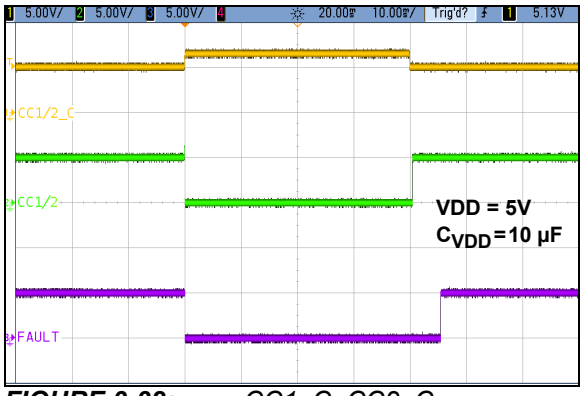


FIGURE 3-32: *CC1_C, CC2_C Overvoltage Long.*

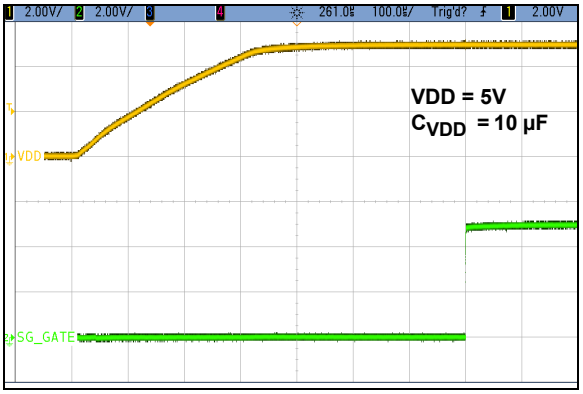


FIGURE 3-33: *Soft Start Turn ON: SG_GATE.*

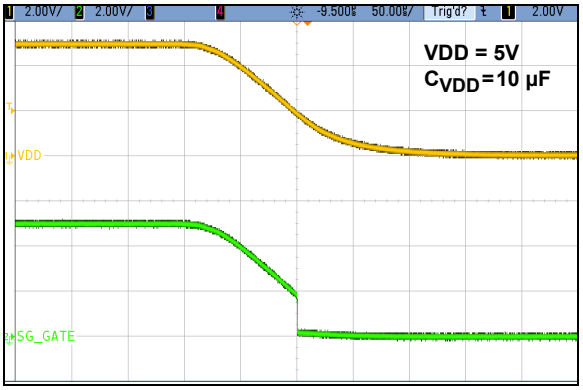


FIGURE 3-34: *Soft Start Turn OFF: SG_GATE.*

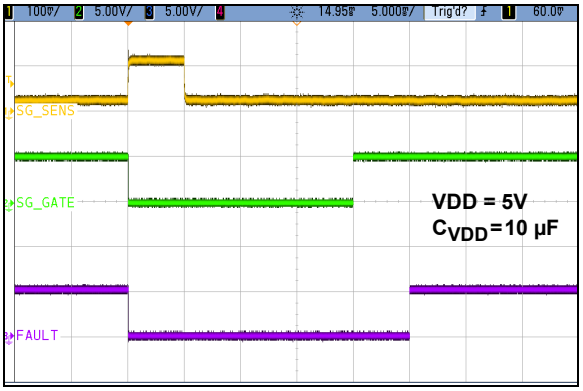


FIGURE 3-35: *Battery Short-to-GND.*

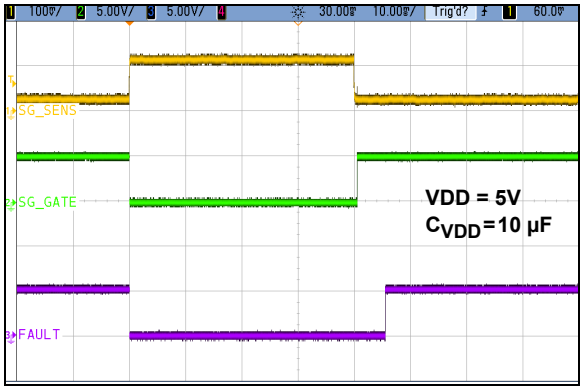


FIGURE 3-36: *Battery Short-to-GND Long.*

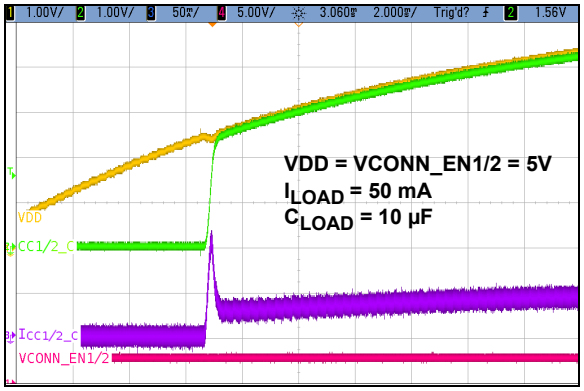


FIGURE 3-37: *Soft Start Turn ON: VCONN.*

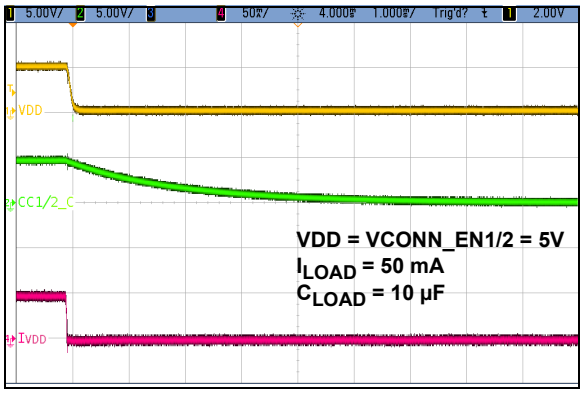


FIGURE 3-38: *Soft Start Turn OFF: VCONN.*

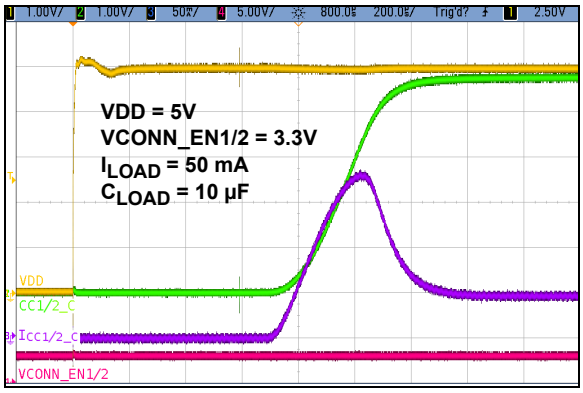


FIGURE 3-39: *Hot Plug: VCONN.*

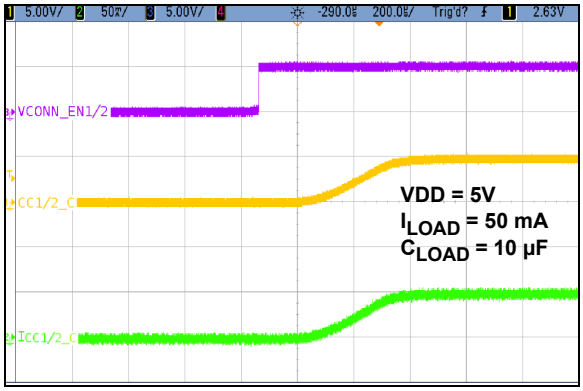


FIGURE 3-40: *Turn ON with VCONN_EN1/2: VCONN.*

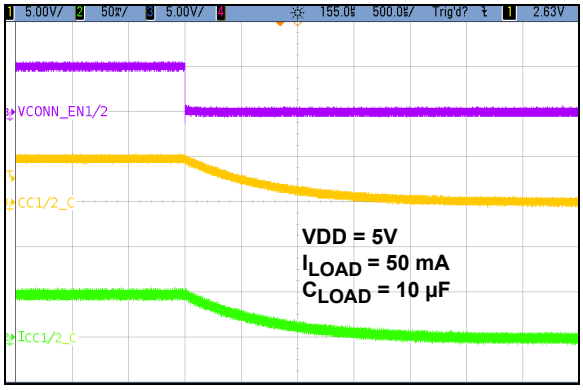


FIGURE 3-41: *Turn OFF with VCONN_EN1/2: VCONN.*

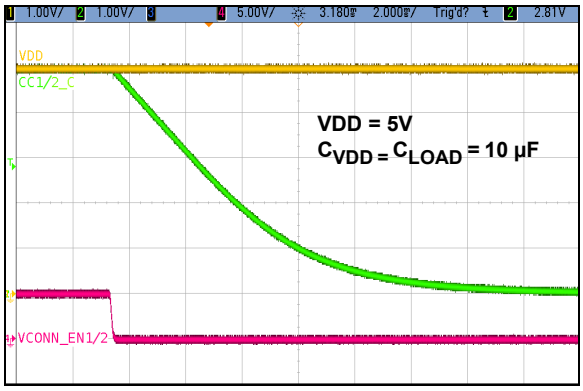


FIGURE 3-42: *VCONN_EN1/2 to CC1_C, CC2_C Pull-Down Level: VCONN.*

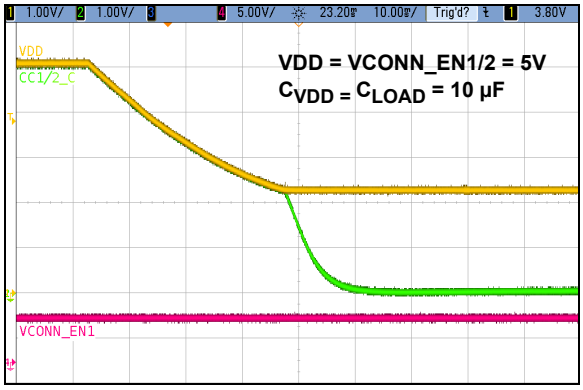


FIGURE 3-43: *Undervoltage Lockout to CC1_C, CC2_C Pull-Down Level: VCONN.*

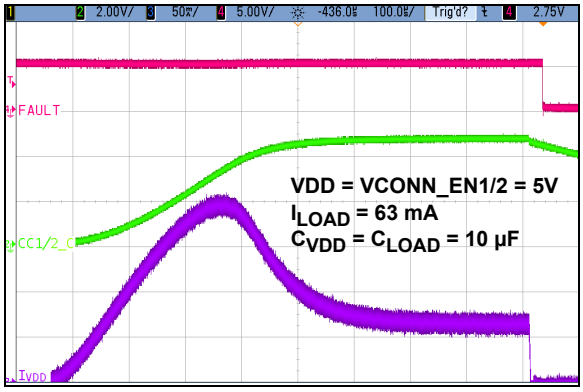


FIGURE 3-44: *Turn ON into 25% Overload – 63 mA: VCONN.*

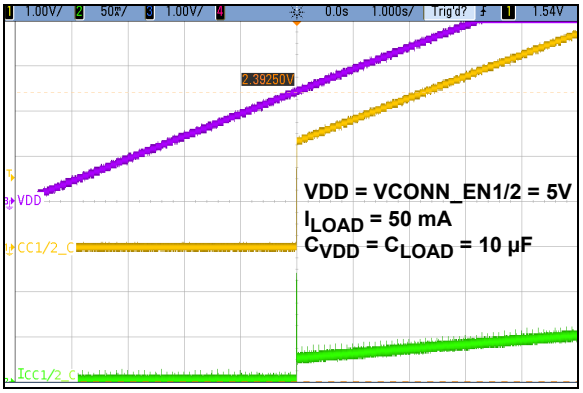


FIGURE 3-45: *VDD UVLO Threshold.*

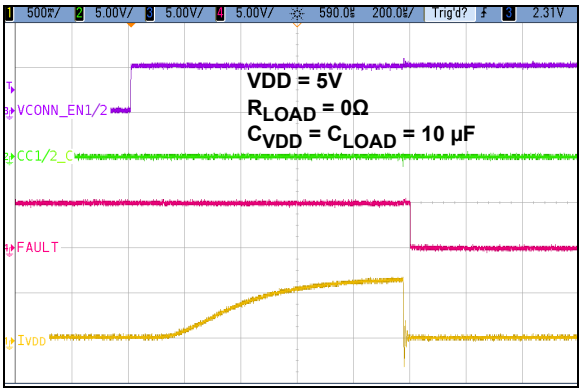


FIGURE 3-46: *Turn ON with CC1_C, CC2_C Shorted to GND: VCONN.*

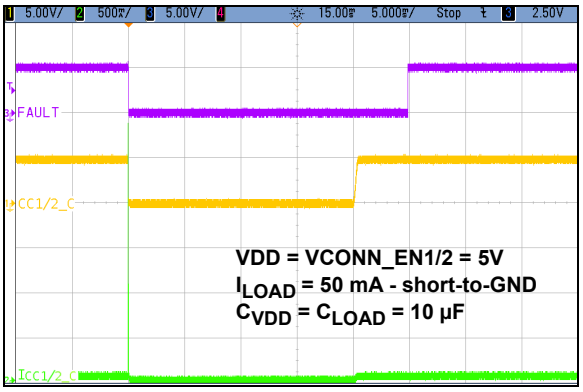


FIGURE 3-47: *Output Recovery from Short Circuit: VCONN.*

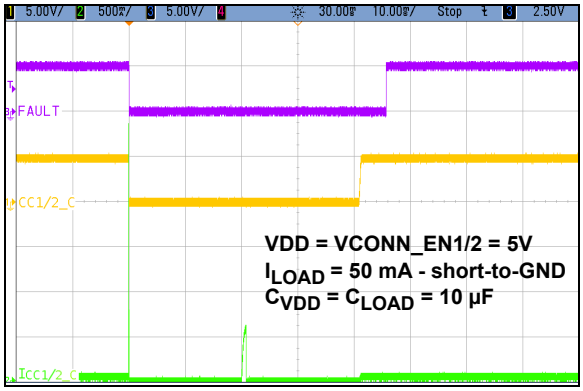


FIGURE 3-48: *Output Recovery from Short Circuit – Long: VCONN.*

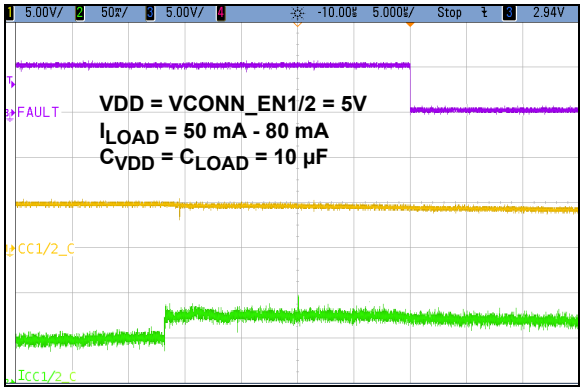


FIGURE 3-51: *80 mA Overload Response: VCONN.*

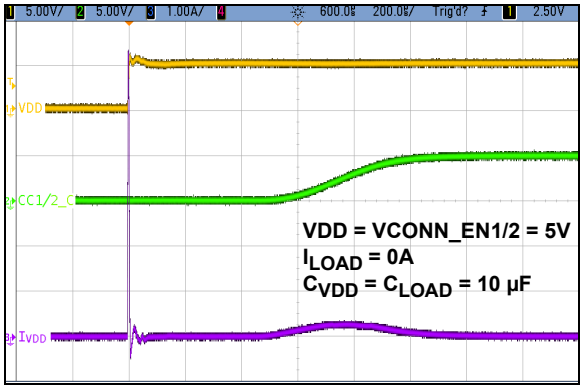


FIGURE 3-49: *Inrush Current.*

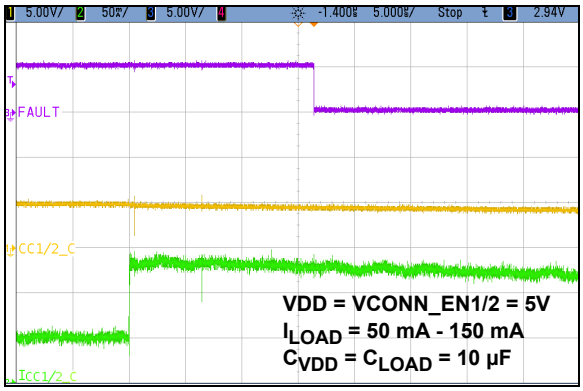


FIGURE 3-52: *150 mA Overload Response: VCONN.*

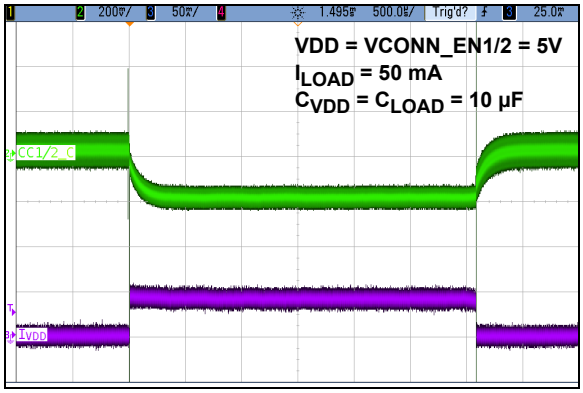
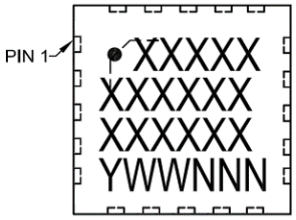


FIGURE 3-50: *Fast Load Transient Response: VCONN.*

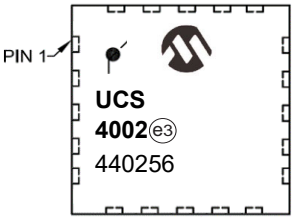
4.0 PACKAGING INFORMATION

4.1 Package Drawing

20-Lead VQFN, 4x4x1.0 mm



Example:

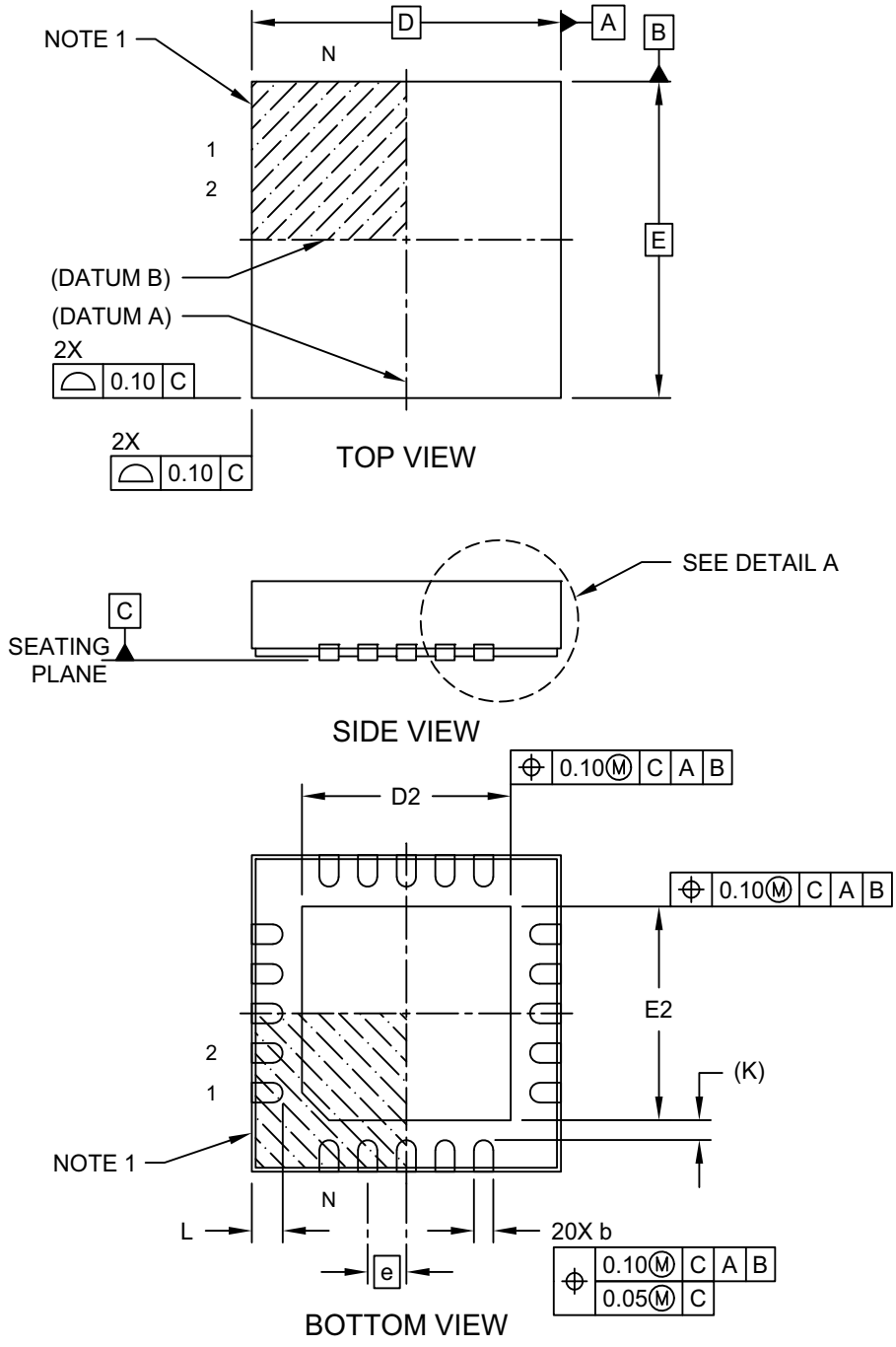


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

20-Lead Plastic Quad Flat, No Lead Package (6N,6NX) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

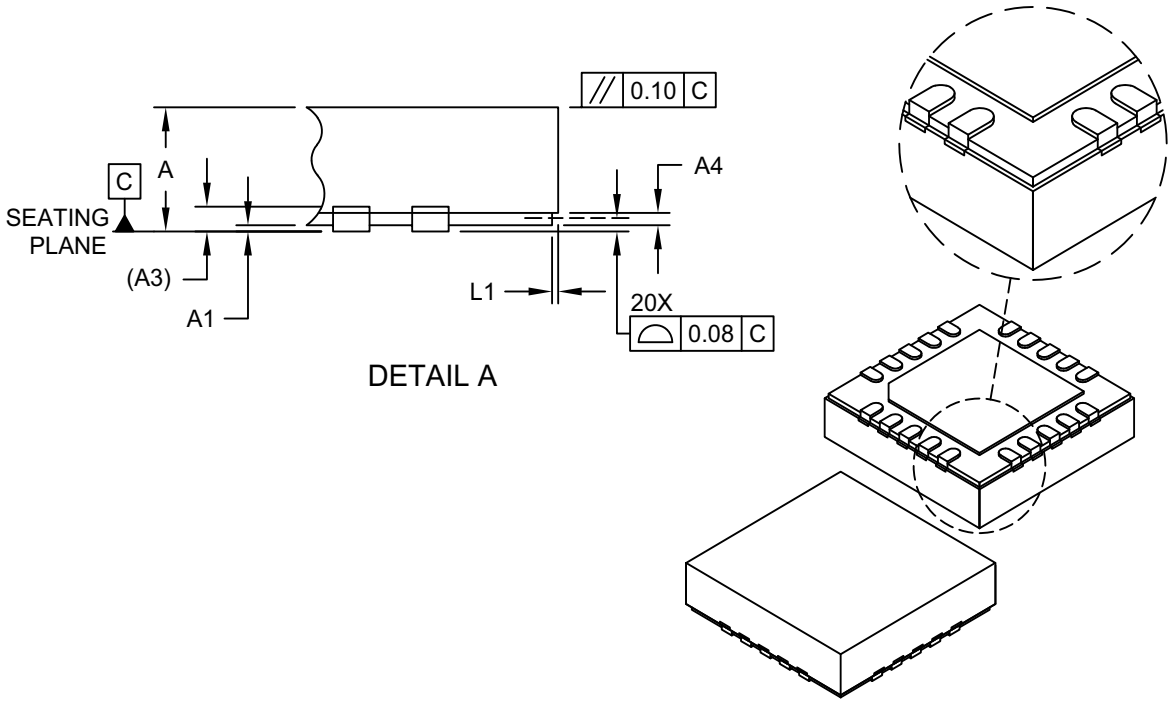
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-402E Sheet 1 of 2

20-Lead Plastic Quad Flat, No Lead Package (6N,6NX) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Step Height	A4	0.10	–	0.19
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Step Length	L1	0.035	0.060	0.085
Terminal-to-Exposed Pad	K		0.25 REF	

Notes:

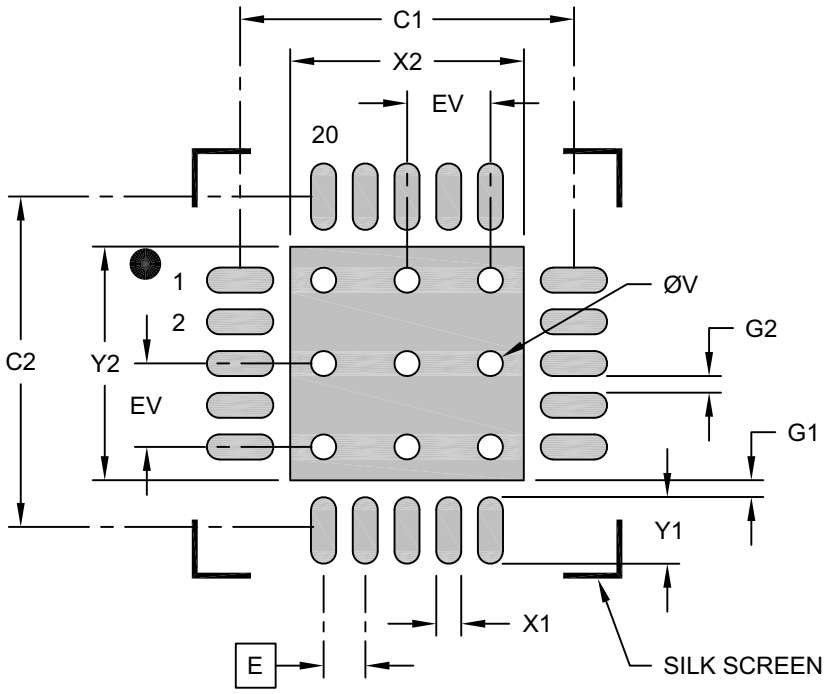
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-402E Sheet 2 of 2

20-Lead Plastic Quad Flat, No Lead Package (6N,6NX) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X20)	G1	0.25		
Contact Pad to Contact Pad (X16)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2402E

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2024)

- Original release of this document.

Revision B (April 2024)

- Updated Electrical Specifications.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[T]	-X	/XX	XXX
Device	Tape and Reel	Temperature Range	Package	Qualification

Device:	UCS4002: Type-C port protector for D+, D- and CC with integrated VCONN FETs	
Tape and Reel Option(1):	(Blank)	= Standard packaging (tube: 91/tube)
	T	= Tape and Reel[1] (3300/reel)
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	6NX	= Very Thin Plastic Quad Flatpack No-Leads Package, with Wettable Flanks - 4x4 mm Body with 0.40 mm Contact Length, VQFN, 20-lead
Qualification*:	(Blank)	= Standard Part
	VAO	= AEC-Q100 Automotive Qualified

Examples:

a) UCS4002-E/6N: USB Type-C port protector for D+, D- and CC with integrated VCONN FETs, Standard Packaging (tube)

b) UCS4002T-E/6N: USB Type-C port protector for D+, D- and CC with integrated VCONN FETs, Tape and Reel

c) UCS4002-E/6NVAO: USB Type-C port protector for D+, D- and CC with integrated VCONN FETs, Standard Packaging (tube), AEC-Q100 Automotive Qualified

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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