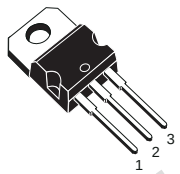
STP50NE10

N-channel 100V - 0.021Ω - 50A TO-220
STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STP50NE10	100V	<0.027Ω	50A

- Exceptional high dv/dt capability
- 100% avalanche tested
- Low gate charge at 100 °C
- Application oriented characterization

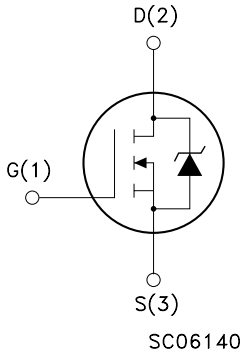


TO-220

Description

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibil ty.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STP50NE10	P50NE10	TO-220	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	50	A
I_D	Drain current (continuous) at T_C=100°C	35	A
I_{DM}(1)	Drain current (pulsed)	200	A
P_{TOT}	Total dissipation at T_C = 25°C	180	W
	Derating factor	1	W/°C
dv/dt(2)	Peak diode recovery voltage slope	6	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	175 -65 to 175	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤50A, di/dt ≤300A/µs, V_{DD} ≤$V_{(BR)DSS}$, T_j ≤T_{JMAX}

Table 2. Thermal data

$R_{thj\text{-}case}$	Thermal resistance junction-case Max	1	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	62.5	°C/W
Rthc-sink	Thermal resistance case-sink typ	0.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	50	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	300	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 25A		0.021	0.027	Ω

Table 5. Dynamic

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > ID(on) x RDS(on)max, I_D = 25A	20	35		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		4350 5000 175	6000 675 238	pF pF pF
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 50V, I_D = 25A, R_G = 4.7Ω, V_{GS} = 10V (see Figure 12)		25 100	34 135	ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=80V, I_D = 50A V_{GS} =10V		123 24 47	166	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Source drain diode

Symbol	Parameter	Test condictions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				6	A
I_{SDM}(1)	Source-drain current (pulsed)				24	A
V_{SD}(2)	Forward on voltage	I_{SD}=50A, V_{GS}=0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=50A, di/dt = 100A/µs, V_{DD}=30V, Tj=150°C (see Figure 14)		155 700 9		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

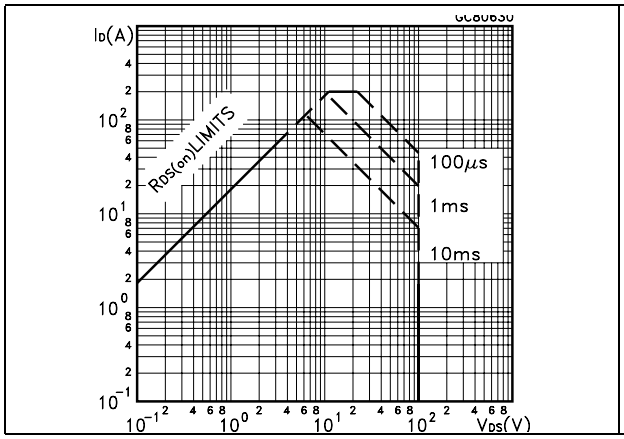


Figure 2. Thermal impedance

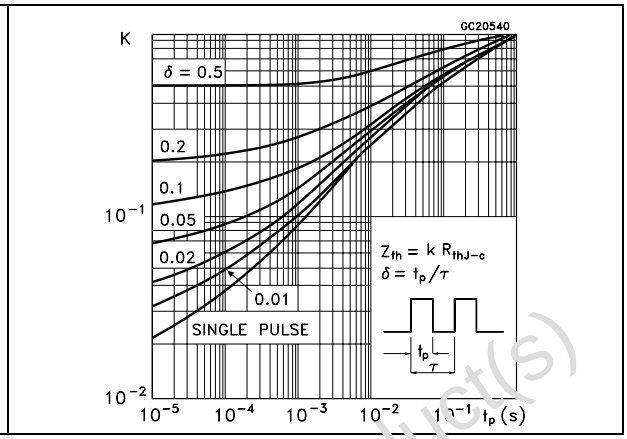


Figure 3. Output characterisics

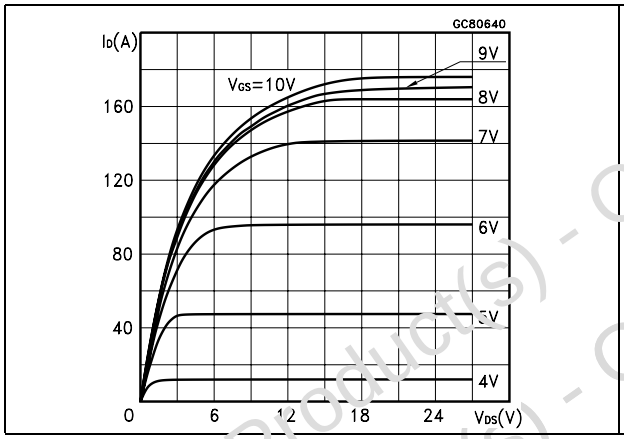


Figure 4. Transfer characteristics

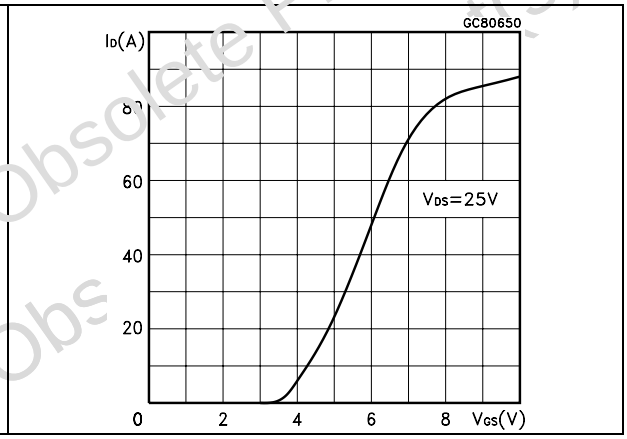


Figure 5. Transconductance

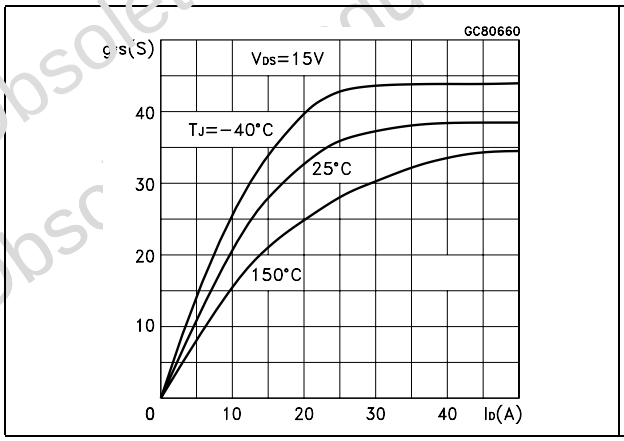


Figure 6. Static drain-source on resistance

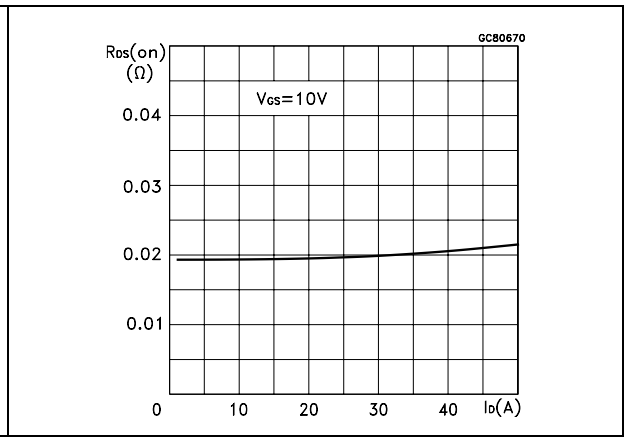


Figure 7. Gate charge vs gate-source voltage

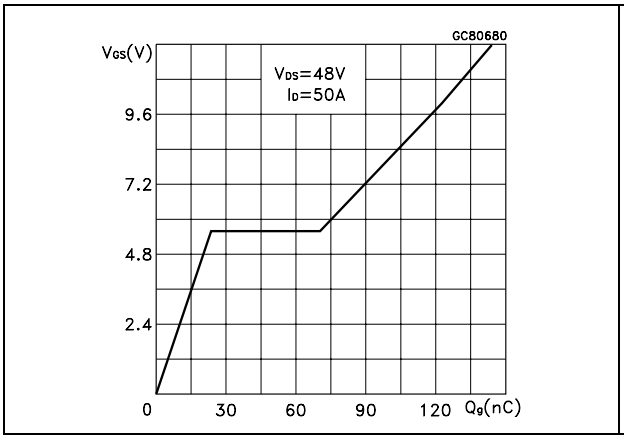


Figure 8. Capacitance variations

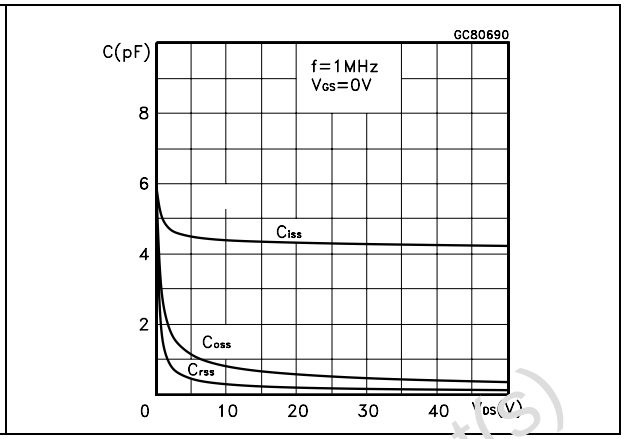


Figure 9. Normalized gate threshold voltage vs temperature

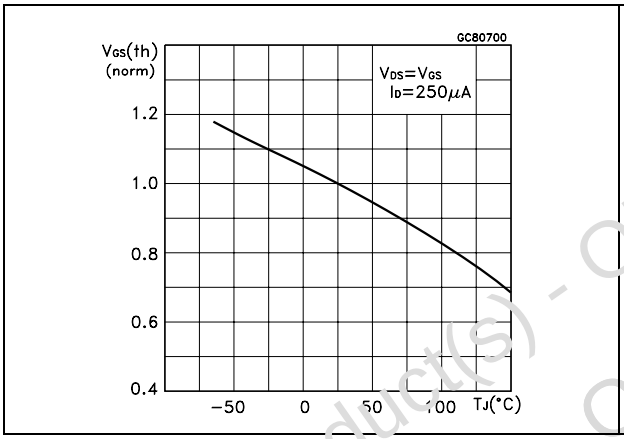


Figure 10. Normalized on resistance vs temperature

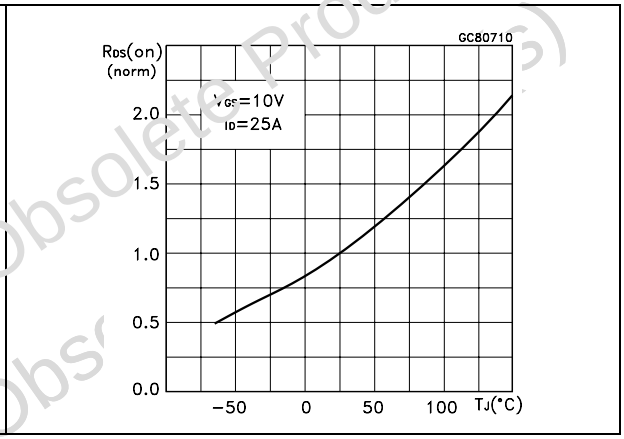
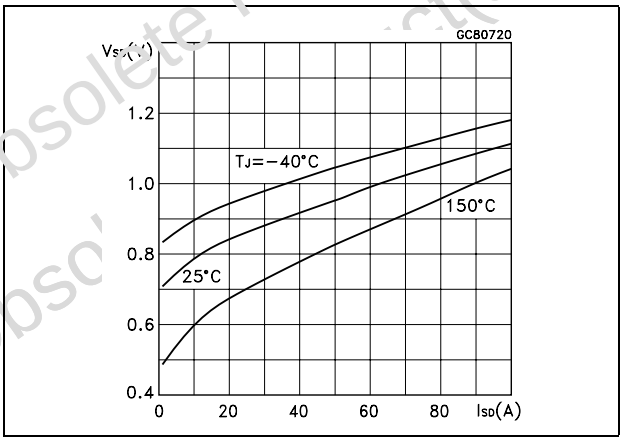


Figure 11. Source drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

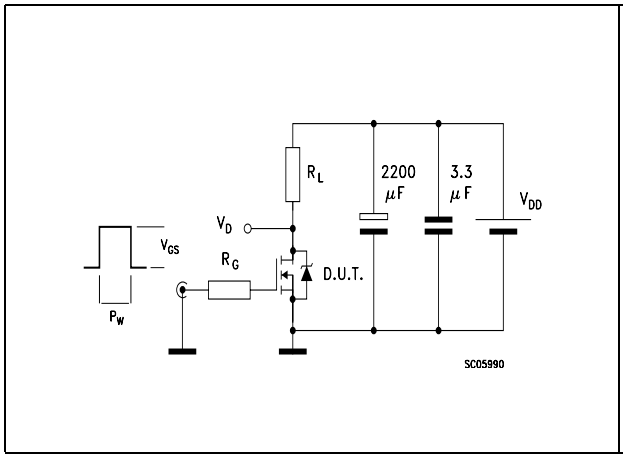


Figure 13. Gate charge test circuit

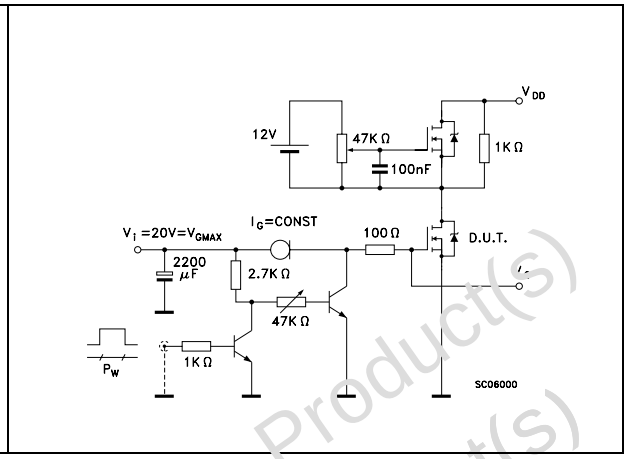


Figure 14. Test circuit for inductive load switching and diode recovery times

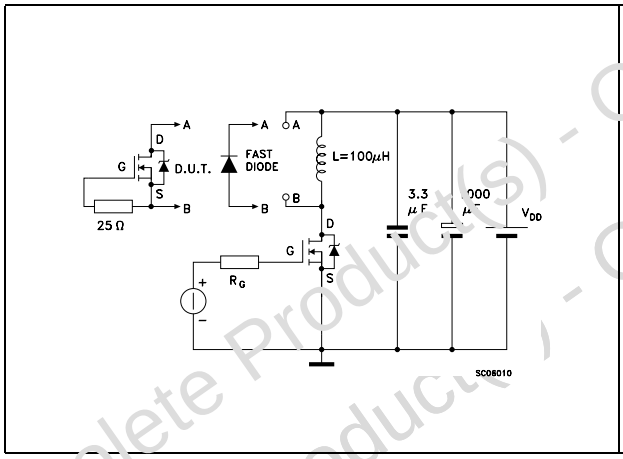


Figure 15. Unclamped Inductive load test circuit

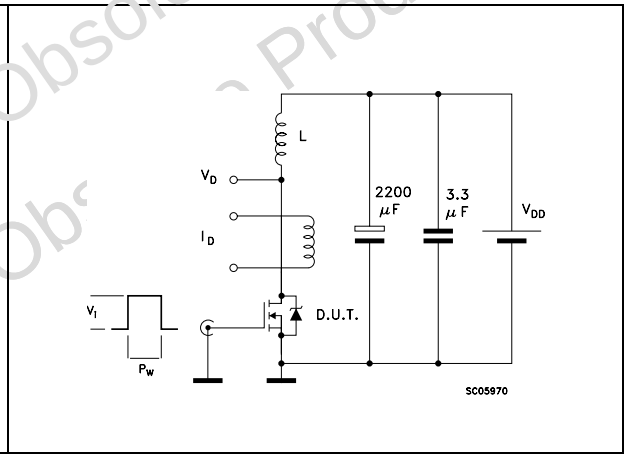


Figure 16. Unclamped inductive waveform

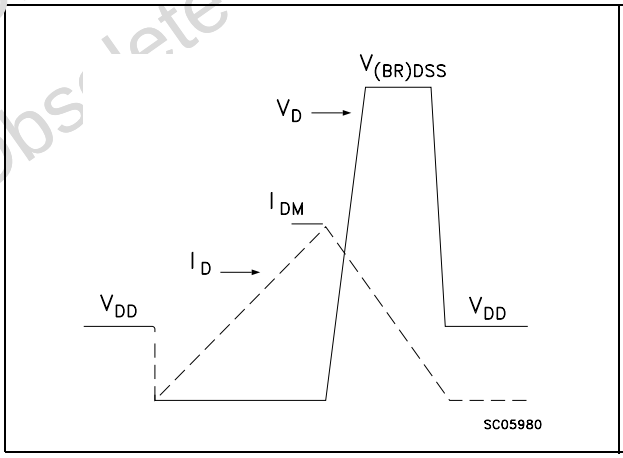
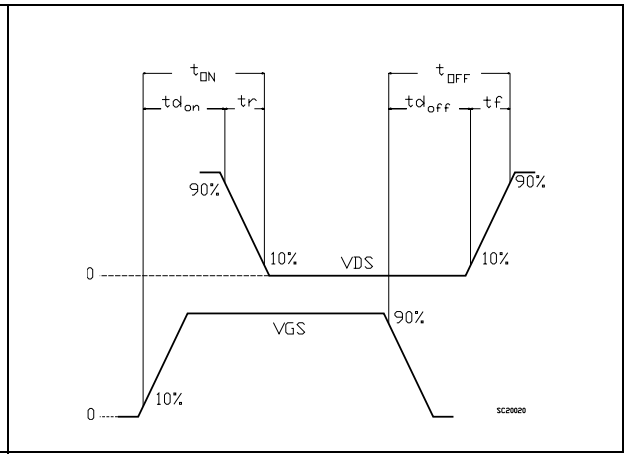


Figure 17. Switching time waveform

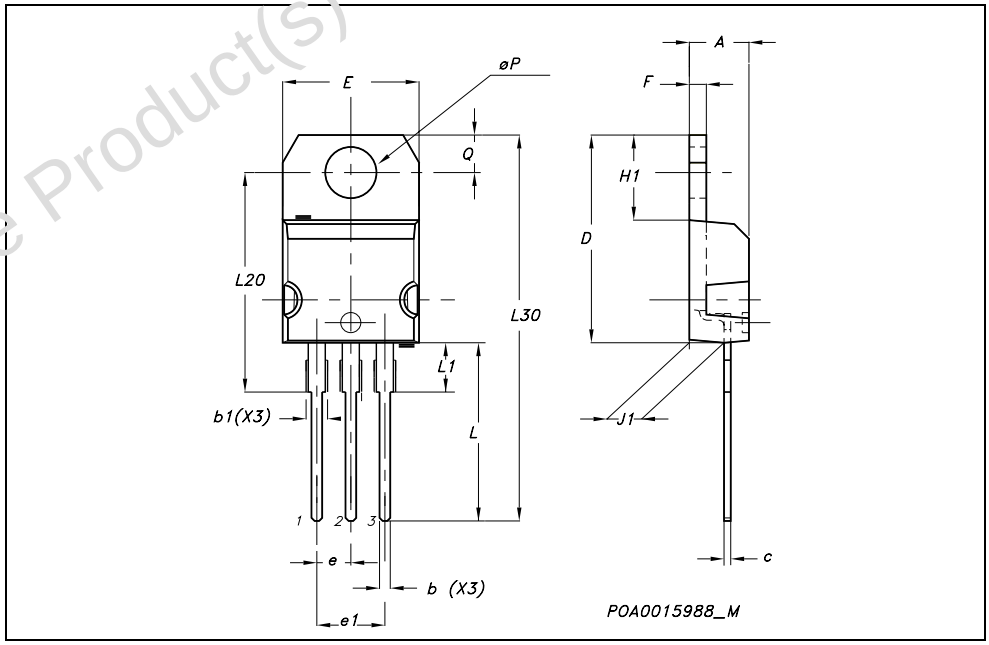


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Sep-2004	7	Complete version
10-Aug-2006	8	New template, no content change

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