

Dual Operational Transconductance Amplifier

NE5517

The NE5517 contains two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to 0.5% THD. The NE5517 is suited for a wide variety of industrial and consumer applications.

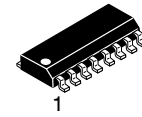
Constant impedance of the buffers on the chip allow general use of the NE5517. These buffers are made of Darlington transistors and a biasing network that virtually eliminate the change of offset voltage due to a burst in the bias current I_{ABC} , hence eliminating the audible noise that could otherwise be heard in high quality audio applications.

Features

- Constant Impedance Buffers
- ΔV_{BE} of Buffer is Constant with Amplifier I_{BIAS} Change
- Excellent Matching Between Amplifiers
- Linearizing Diodes
- High Output Signal-to-Noise Ratio
- This is a Pb-Free Device

Applications

- Multiplexers
- Timers
- Electronic Music Synthesizers
- Dolby® HX Systems
- Current-Controlled Amplifiers, Filters
- Current-Controlled Oscillators, Impedances



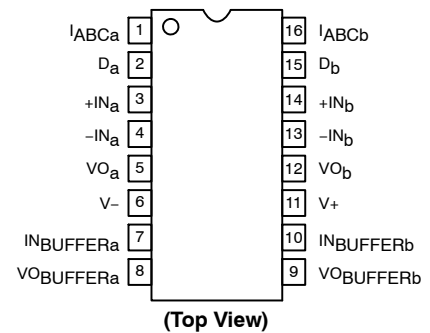
SOIC-16
D SUFFIX
CASE 751B

MARKING DIAGRAM



- xx = NE
- A = Assembly Location
- WL = Wafer Lot
- YY, Y = Year
- WW = Work Week
- G = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

NE5517

PIN DESCRIPTION

Pin No.	Symbol	Description
1	I_{ABCa}	Amplifier Bias Input A
2	D_a	Diode Bias A
3	$+IN_a$	Non-inverted Input A
4	$-IN_a$	Inverted Input A
5	VO_a	Output A
6	V_-	Negative Supply
7	$IN_{BUFFERa}$	Buffer Input A
8	$VO_{BUFFERa}$	Buffer Output A
9	$VO_{BUFFERb}$	Buffer Output B
10	$IN_{BUFFERb}$	Buffer Input B
11	V_+	Positive Supply
12	VO_b	Output B
13	$-IN_b$	Inverted Input B
14	$+IN_b$	Non-inverted Input B
15	D_b	Diode Bias B
16	I_{ABCb}	Amplifier Bias Input B

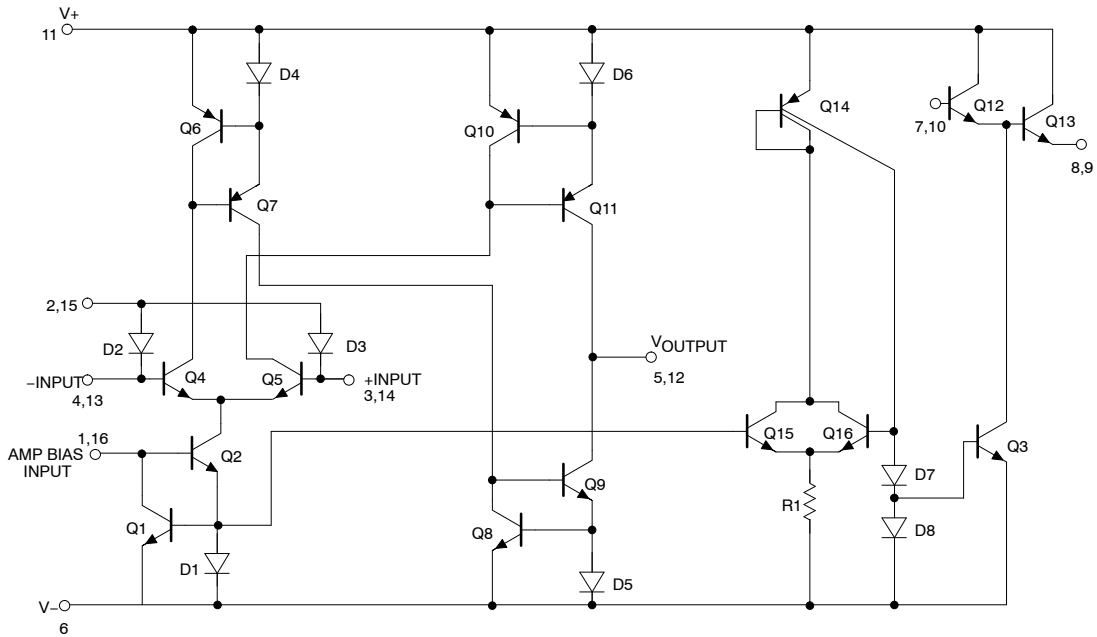
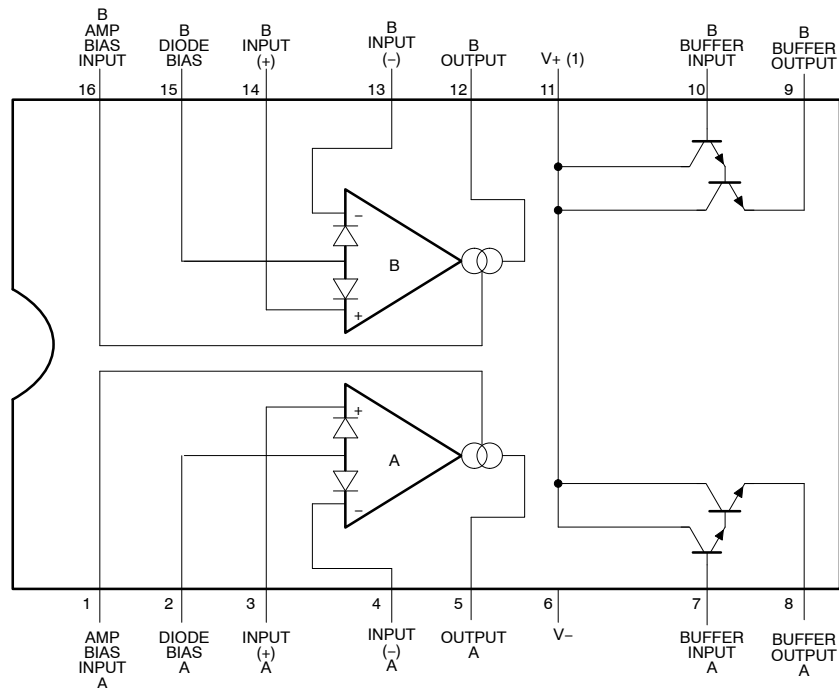


Figure 1. Circuit Schematic

NE5517



NOTE: V_+ of output buffers and amplifiers are internally connected.

Figure 2. Connection Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	V_S	44 V_{DC} or ± 22	V
Power Dissipation, $T_{amb} = 25^\circ\text{C}$ (Still Air) (Note 2)	P_D	1125	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	140	$^\circ\text{C}/\text{W}$
Differential Input Voltage	V_{IN}	± 5.0	V
Diode Bias Current	I_D	2.0	mA
Amplifier Bias Current	I_{ABC}	2.0	mA
Output Short-Circuit Duration	I_{SC}	Indefinite	
Buffer Output Current (Note 3)	I_{OUT}	20	mA
Operating Temperature Range	T_{amb}	0°C to $+70^\circ\text{C}$	$^\circ\text{C}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
DC Input Voltage	V_{DC}	$+V_S$ to $-V_S$	
Storage Temperature Range	T_{stg}	-65°C to $+150^\circ\text{C}$	$^\circ\text{C}$
Lead Soldering Temperature (10 sec max)	T_{slid}	230	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- For selections to a supply voltage above ± 22 V, contact factory.
- The following derating factors should be applied above 25°C
D package at $7.1\text{ mW}/^\circ\text{C}$.
- Buffer output current should be limited so as to not exceed package dissipation.

NE5517

ELECTRICAL CHARACTERISTICS (Note 4)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	Overtemperature Range $I_{ABC} = 5.0 \mu A$	V_{OS}		0.4 0.3	5.0 5.0	mV
$\Delta V_{OS}/\Delta T$	Avg. TC of Input Offset Voltage			7.0		$\mu V/^{\circ}C$
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA			0.5	5	mV
Input Offset Change	$5.0 \mu A \leq I_{ABC} \leq 500 \mu A$	V_{OS}		0.1		mV
Input Offset Current		I_{OS}		0.1	0.6	μA
$\Delta I_{OS}/\Delta T$	Avg. TC of Input Offset Current			0.001		$\mu A/^{\circ}C$
Input Bias Current	Overtemperature Range	I_{BIAS}		0.4 1.0	5.0 8.0	μA
$\Delta I_B/\Delta T$	Avg. TC of Input Current			0.01		$\mu A/^{\circ}C$
Forward Transconductance	Overtemperature Range	g_M	6700 5400	9600	13000	μmho
g_M Tracking				0.3		dB
Peak Output Current	$R_L = 0, I_{ABC} = 5.0 \mu A$ $R_L = 0, I_{ABC} = 500 \mu A$ $R_L = 0, \text{Overtemperature Range}$	I_{OUT}	350 300	5.0 500	650	μA
Peak Output Voltage Positive Negative	$R_L = \infty, 5.0 \mu A \leq I_{ABC} \leq 500 \mu A$ $R_L = \infty, 5.0 \mu A \leq I_{ABC} \leq 500 \mu A$	V_{OUT}	+12 -12	+14.2 -14.4		V
Supply Current	$I_{ABC} = 500 \mu A$, both channels	I_{CC}		2.6	4.0	mA
V_{OS} Sensitivity Positive Negative	$\Delta V_{OS}/\Delta V_+$ $\Delta V_{OS}/\Delta V_-$			20 20	150 150	$\mu V/V$
Common-mode Rejection Ratio		CMRR	80	110		dB
Common-mode Range			± 12	± 13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz			100		dB
Differential Input Current	$I_{ABC} = 0$, Input = ± 4.0 V	I_{IN}		0.02	100	nA
Leakage Current	$I_{ABC} = 0$ (Refer to Test Circuit)			0.2	100	nA
Input Resistance		R_{IN}	10	26		k Ω
Open-loop Bandwidth		B_W		2.0		MHz
Slew Rate	Unity Gain Compensated	SR		50		V/ μs
Buffer Input Current	5	$I_{N_{BUFFER}}$		0.4	5.0	μA
Peak Buffer Output Voltage	5	$V_{O_{BUFFER}}$	10			V
ΔV_{BE} of Buffer	Refer to Buffer V_{BE} Test Circuit (Note 6)			0.5	5.0	mV

4. These specifications apply for $V_S = \pm 15$ V, $T_{amb} = 25^{\circ}C$, amplifier bias current (I_{ABC}) = 500 μA , Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

5. These specifications apply for $V_S = \pm 15$ V, $I_{ABC} = 500 \mu A$, $R_{OUT} = 5.0$ k Ω connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

6. $V_S = \pm 15$, $R_{OUT} = 5.0$ k Ω connected from Buffer output to $-V_S$ and $5.0 \mu A \leq I_{ABC} \leq 500 \mu A$.

TYPICAL PERFORMANCE CHARACTERISTICS

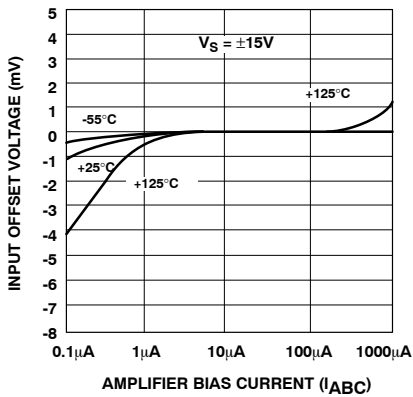


Figure 3. Input Offset Voltage

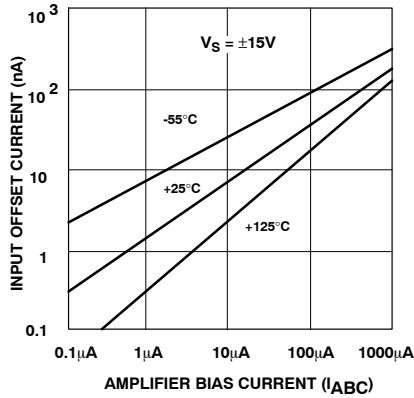


Figure 4. Input Bias Current

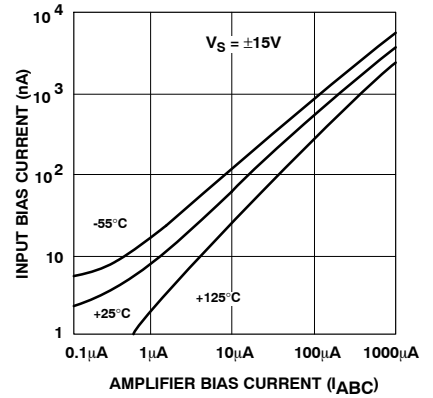


Figure 5. Input Bias Current

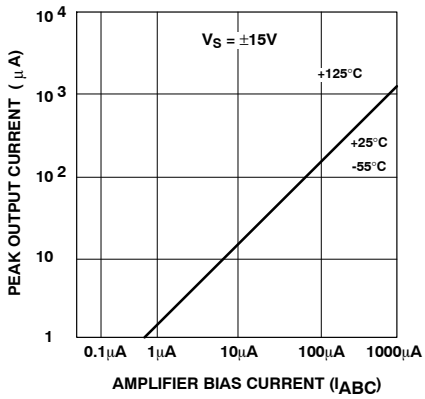


Figure 6. Peak Output Current

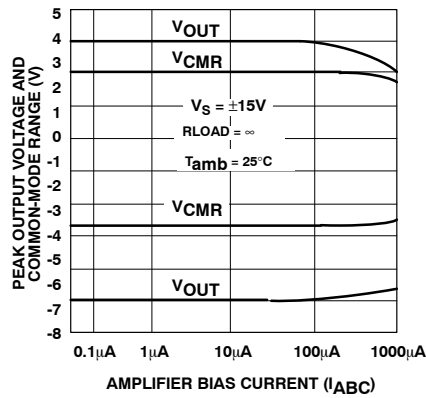


Figure 7. Peak Output Voltage and Common-Mode Range

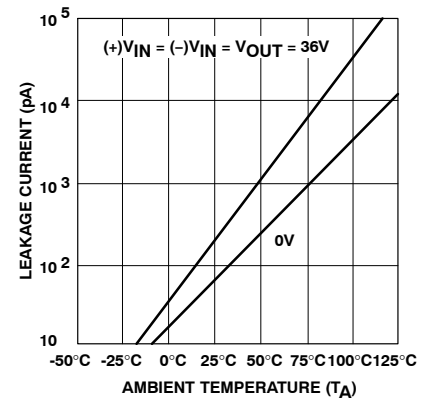


Figure 8. Leakage Current

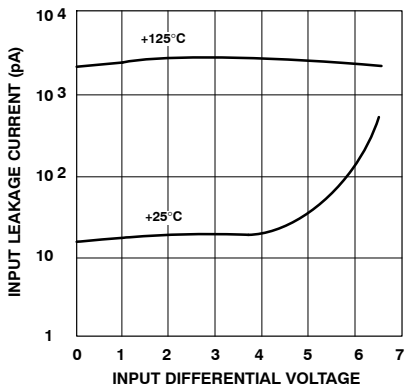


Figure 9. Input Leakage

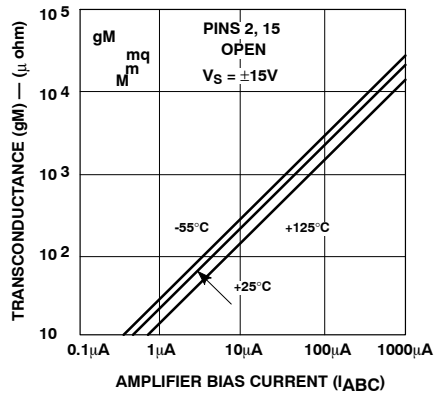


Figure 10. Transconductance

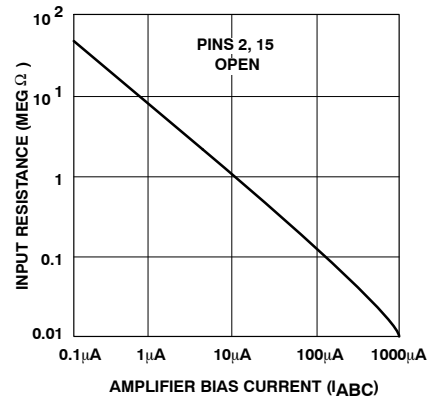


Figure 11. Input Resistance

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

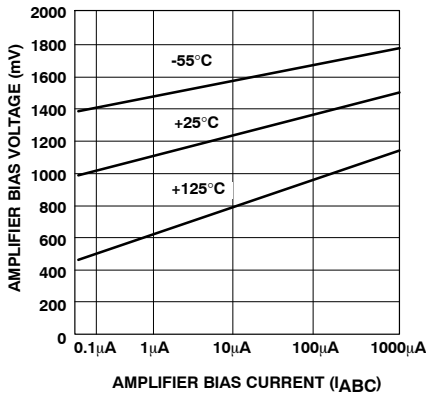


Figure 12. Amplifier Bias Voltage vs. Amplifier Bias Current

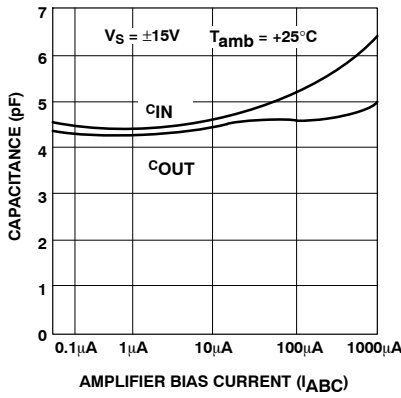


Figure 13. Input and Output Capacitance

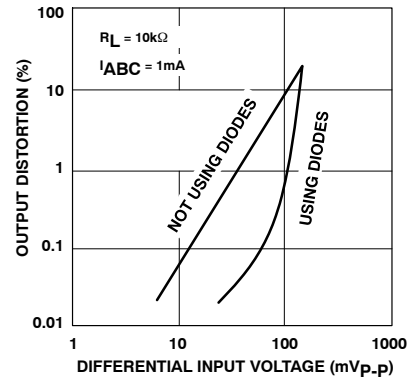


Figure 14. Distortion vs. Differential Input Voltage

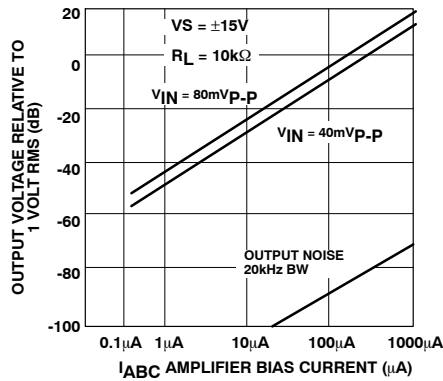


Figure 15. Voltage vs. Amplifier Bias Current

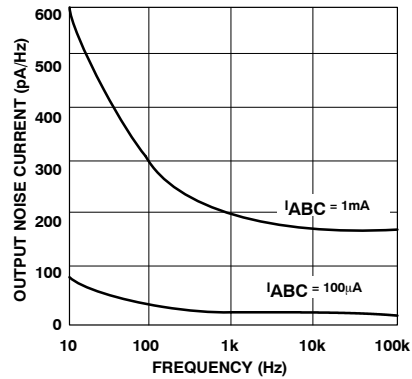


Figure 16. Noise vs. Frequency

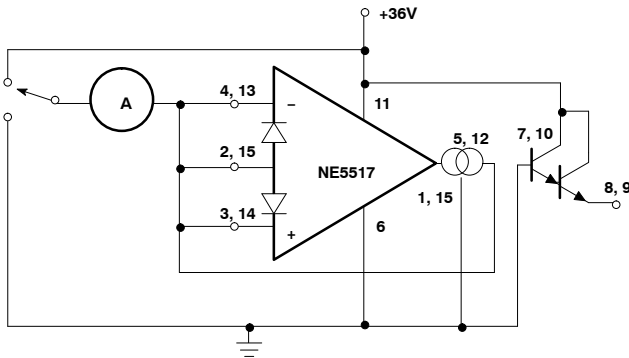


Figure 17. Leakage Current Test Circuit

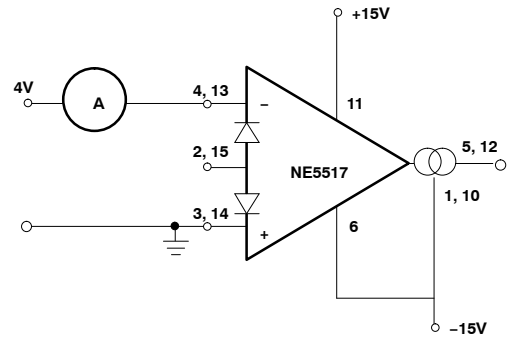


Figure 18. Differential Input Current Test Circuit

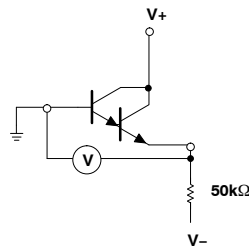


Figure 19. Buffer V_{BE} Test Circuit

APPLICATIONS

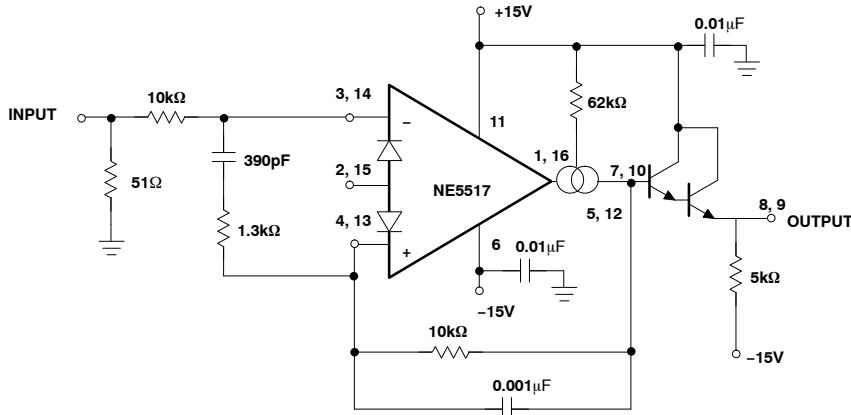


Figure 20. Unity Gain Follower

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 21.

Transconductance Amplifier

The transistor pair, Q₄ and Q₅, forms a transconductance stage. The ratio of their collector currents (I₄ and I₅, respectively) is defined by the differential input voltage, V_{IN}, which is shown in Equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (\text{eq. 1})$$

Where V_{IN} is the difference of the two input voltages
 KT ≅ 26 mV at room temperature (300°k).

Transistors Q₁, Q₂ and diode D₁ form a current mirror which focuses the sum of current I₄ and I₅ to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \quad (\text{eq. 2})$$

If V_{IN} is small, the ratio of I₅ and I₄ will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (\text{eq. 3})$$

$$\text{and } I_4 \cong I_5 \cong I_B$$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2 I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN} \quad (\text{eq. 4})$$

$$I_5 - I_4 = V_{IN} \frac{(I_B)^q}{2KT}$$

The remaining transistors (Q₆ to Q₁₁) and diodes (D₄ to D₆) form three current mirrors that produce an output current equal to I₅ minus I₄. Thus:

$$V_{IN} \left(\frac{I_B^q}{2KT} \right) = I_O \quad (\text{eq. 5})$$

The term $\frac{(I_B)^q}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

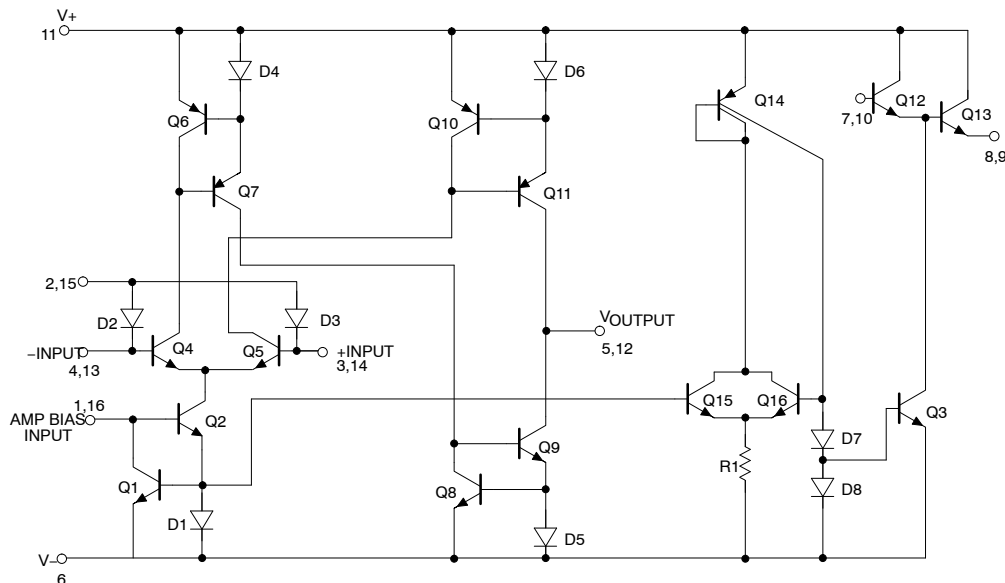


Figure 21. Circuit Diagram of NE5517

Linearizing Diodes

For V_{IN} greater than a few millivolts, Equation 3 becomes invalid and the transconductance increases non-linearly. Figure 22 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S . Since $I_4 + I_5 = I_B$ and $I_5 - I_4 = I_O$, that is: $I_4 = (I_B - I_O)$, $I_5 = (I_B + I_O)$

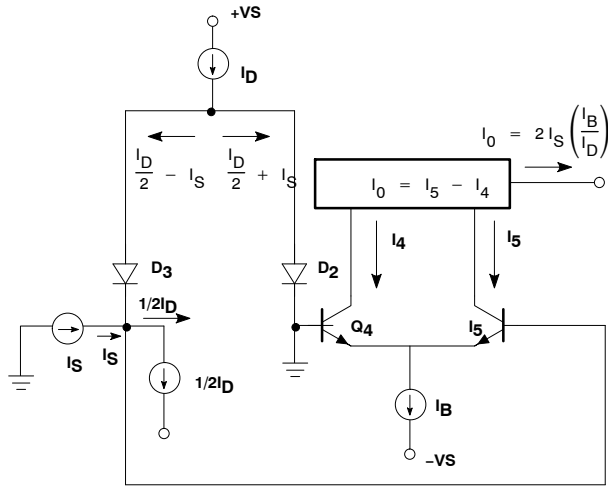


Figure 22. Linearizing Diode

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{I_D/2 + I_S}{I_D/2 - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_O)}{1/2(I_B - I_O)} \quad (\text{eq. 6})$$

$$I_O = I_S \frac{2I_B}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed I_D .

Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2.0 mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B , a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q_{14} , Q_{15} , Q_{16} , D_7 , D_8 , and R_1) suits the need.

APPLICATIONS

Voltage-Controlled Amplifier

In Figure 23, the voltage divider R_2 , R_3 divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot g_M;$$

$$V_{OUT} = I_{OUT} \cdot R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L$$

$$(3) g_M = 19.2 I_{ABC}$$

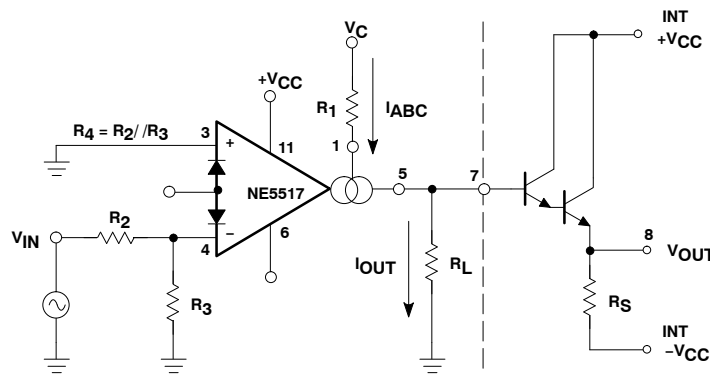
(g_M in μmhos for I_{ABC} in mA)

Since g_M is directly proportional to I_{ABC} , the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the NE5517.



TYPICAL VALUES: $R_1 = 47k\Omega$
 $R_2 = 10k\Omega$
 $R_3 = 200\Omega$
 $R_4 = 200\Omega$
 $R_L = 100k\Omega$
 $R_S = 47k\Omega$

Figure 23.

NE5517

Stereo Amplifier With Gain Control

Figure 24 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer, R_P , the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510 Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to I_{ABC} , the amplification of a signal can be controlled easily. The output current is the product from transconductance \times input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.

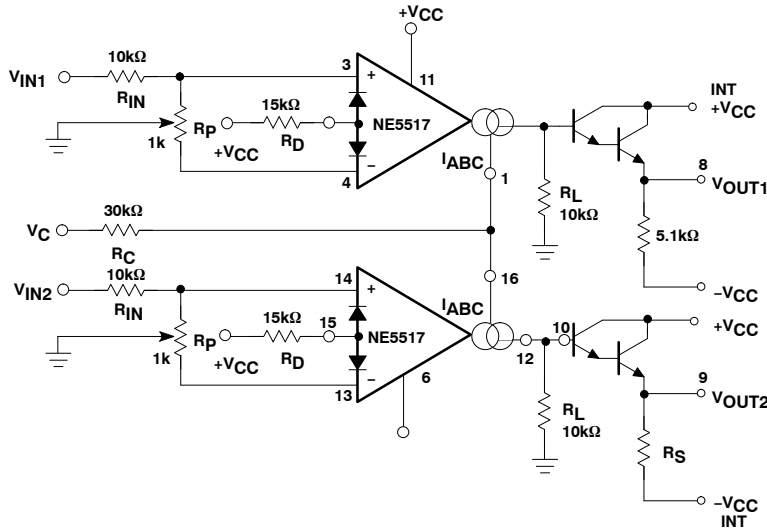


Figure 24. Gain-Controlled Stereo Amplifier

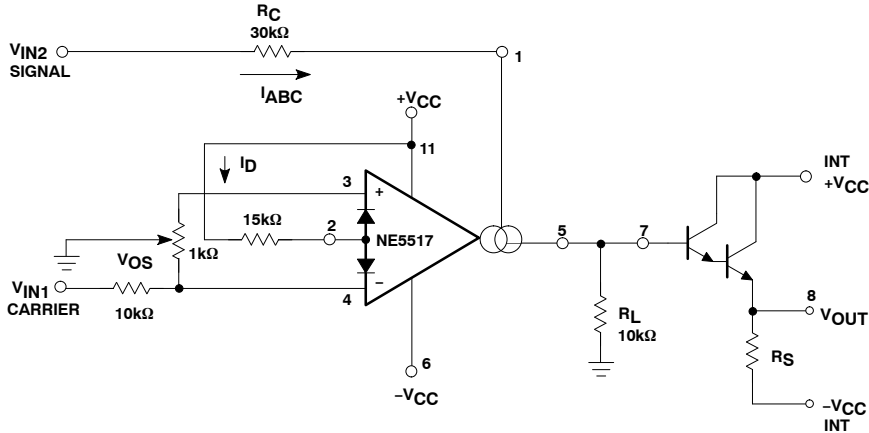


Figure 25. Amplitude Modulator

Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 26 shows how this is done. A voltage presented at the R_X terminals forces a voltage at the input. This voltage is multiplied by g_M and thereby forces a current through the R_X terminals:

$$R_x = \frac{R + R_A}{g_M + R_A}$$

where g_M is approximately 19.21 μ MHOs at room temperature. Figure 27 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

Voltage-Controlled Filters

Figure 28 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until X_C/g_M is equal to R/R_A . Then, the frequency response rolls off at a 6dB per octave with the -3 dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 29. Higher order filters can be made using additional amplifiers as shown in Figures 30 and 31.

Voltage-Controlled Oscillators

Figure 32 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2.0 Hz to 200 kHz is possible by varying I_{ABC} from 1.0 mA to 10 μ A.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5.0 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 33.

APPLICATION HINTS

To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1.0 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to -2.0 mA. In this application, however, the current range is set through R_{REF} (10 k Ω) to 0 to -1.0 mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{5V}{10k\Omega} = 1mA$$

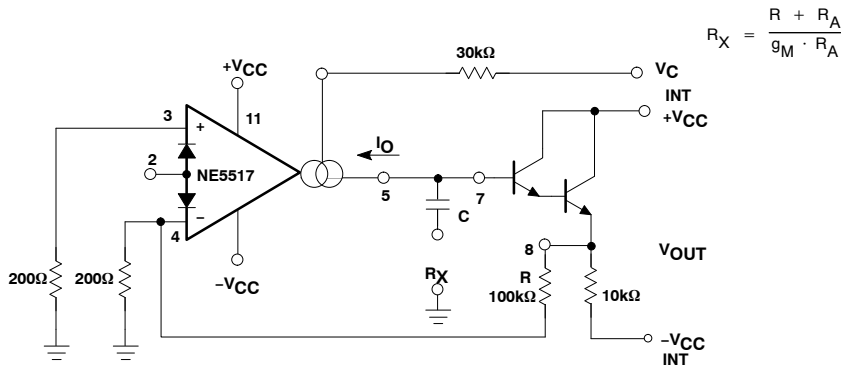


Figure 26. VCR

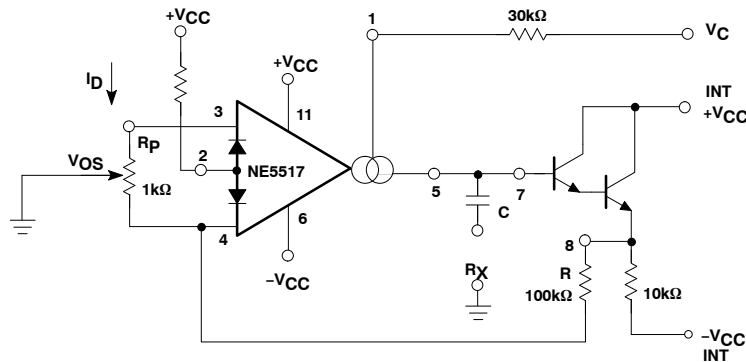
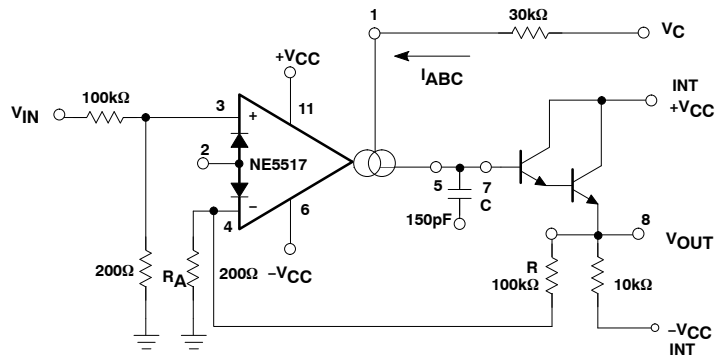


Figure 27. VCR with Linearizing Diodes

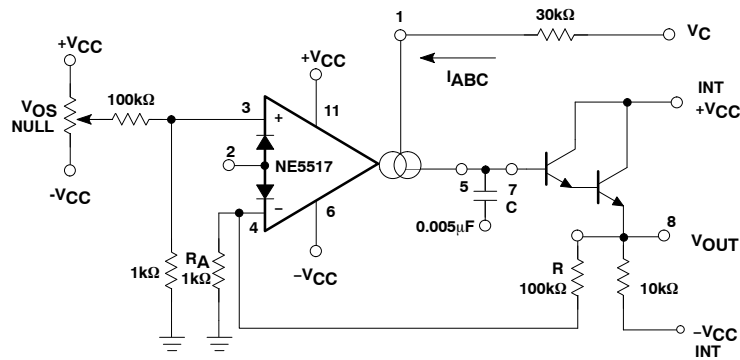
NE5517



NOTE:

$$f_O = \frac{R_A g_M}{g(R + R_A) 2\pi C}$$

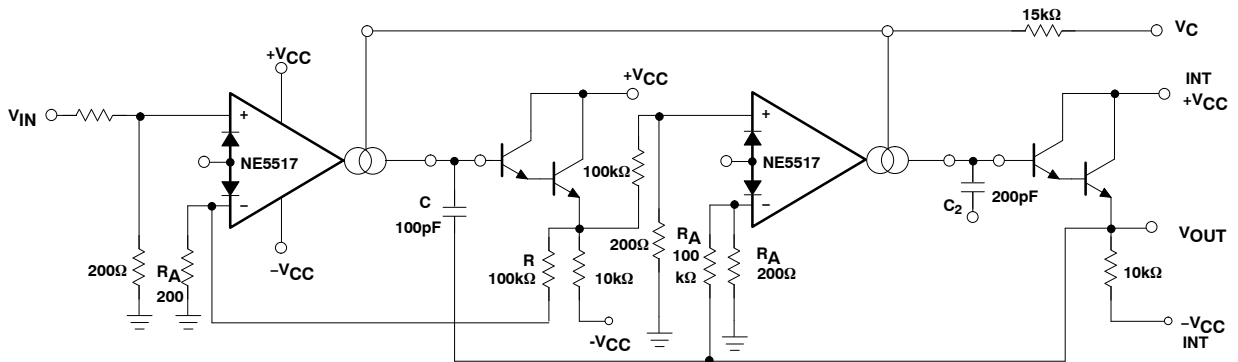
Figure 28. Voltage-Controlled Low-Pass Filter



NOTE:

$$f_O = \frac{R_A g_M}{g(R + R_A) 2\pi C}$$

Figure 29. Voltage-Controlled High-Pass Filter



NOTE:

$$f_O = \frac{R_A g_M}{(R + R_A) 2\pi C}$$

Figure 30. Butterworth Filter - 2nd Order

NE5517

ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
NE5517DR2G	0 to +70 °C	SOIC-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

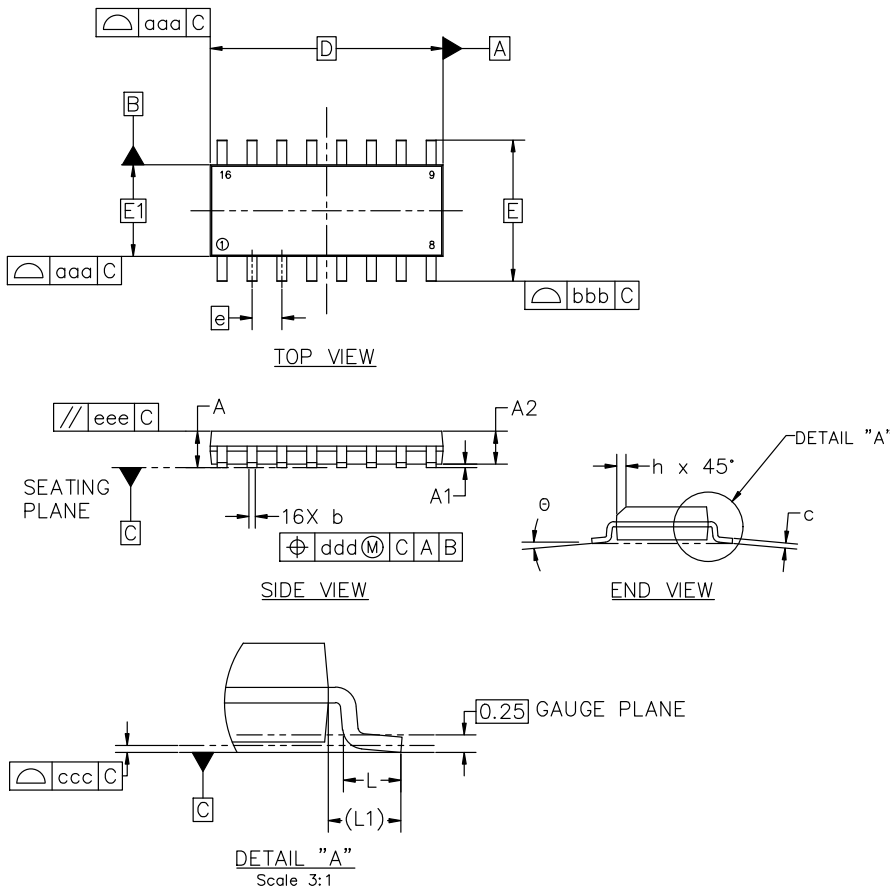


SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

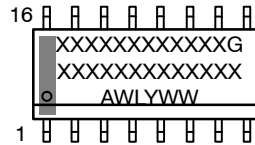
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH</p>	

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16 9.90X3.90X1.50 1.27P	PAGE 2 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales