

## FQA30N40-VB Datasheet

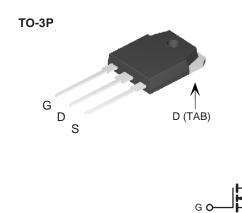
# N-Channel 600V(D-S) Super Junction Power MOSFET

PRODUCT SUMMARY				
$V_{DS}$ (V) at $T_J$ max.	600			
R <sub>DS(on)</sub> at 25 °C (Ω)	V <sub>GS</sub> = 10 V	0.06		
Q <sub>g</sub> max. (nC)	273			
Q <sub>gs</sub> (nC)	46			
Q <sub>gd</sub> (nC)	79			
Configuration	Single			

#### **FEATURES**

- Low figure-of-merit (FOM) Ron x Qq
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Ultra low gate charge (Q<sub>a</sub>)
- Avalanche energy rated (UIS)





N-Channel MOSFET

#### **APPLICATIONS**

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			$V_{DS}$	600	.,	
Gate-Source Voltage			$V_{GS}$	± 30	V	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	- I <sub>D</sub>	47		
		T <sub>C</sub> = 100 °C		30	А	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	142		
Linear Derating Factor				3.3	W/°C	
Single Pulse Avalanche Energy b			E <sub>AS</sub>	1410	mJ	
Maximum Power Dissipation			$P_{D}$	415	W	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Drain-Source Voltage Slope	T <sub>J</sub> = 125 °C		37		Mar	
Reverse Diode dV/dt <sup>d</sup>			dV/dt	9	- V/ns	
Soldering Recommendations (Peak Temperature) c	for 10 s			300	°C	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b.  $V_{DD}$  = 50 V, starting  $T_J$  = 25 °C, L = 28.2 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 10 A.
- c. 1.6 mm from case.
- d.  $I_{SD} \le I_D$ ,  $dI/dt = 100 \text{ A/}\mu\text{s}$ , starting  $T_J = 25 \,^{\circ}\text{C}$ .



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	40	°C/W	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.3	C/ VV	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		-					
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$		2	-	4	V
0.1. 0	I <sub>GSS</sub>	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Gate-Source Leakage			$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μA
Zone Ooto Voltana Dusia Ormant	,	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 520 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 \text{ °C}$		-	-	1	μА
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			-	-	25	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 24 A	-	0.06	=.	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 24 A		-	16.7	-	S
Dynamic		-					•
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	5682	-	pF
Output Capacitance	C <sub>oss</sub>			-	251	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	1	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-	192	-	
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>			-	665	-	
Total Gate Charge	$Q_g$			-	182	273	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V I <sub>D</sub> = 24 A, V <sub>DS</sub> = 520 V		-	46	-	nC
Gate-Drain Charge	$Q_{gd}$			-	79	-	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD} = 520 \text{ V}, I_{D} = 6 \text{ A}, V_{GS} = 10 \text{ V}, R_{g} = 9.1 \Omega$		-	47	94	- ns
Rise Time	t <sub>r</sub>			-	87	131	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	156	234	
Fall Time	t <sub>f</sub>			=.	103	206	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		=	0.64	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	47	
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	139	A
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 24 A, V <sub>GS</sub> = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	$T_J = 25 \text{ °C, } I_F = I_S = 24 \text{ A,}$ $dI/dt = 100 \text{ A/µs, } V_R = 25 \text{ V}$		-	753	1506	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	14	28	μC
Reverse Recovery Current	I <sub>RRM</sub>			_	28	-	A

#### Notes

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ . b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .



### TYPCIAL CHARACTERISTICS (25 °C, unless otherwise noted)

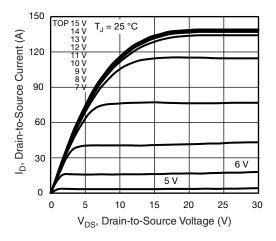


Fig. 1 - Typical Output Characteristics

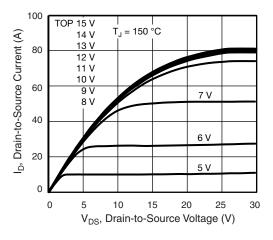


Fig. 2 - Typical Output Characteristics

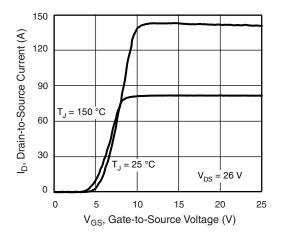


Fig. 3 - Typical Transfer Characteristics

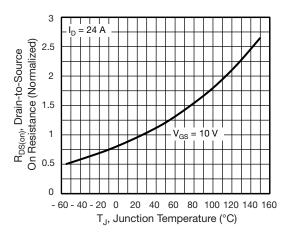


Fig. 4 - Normalized On-Resistance vs. Temperature

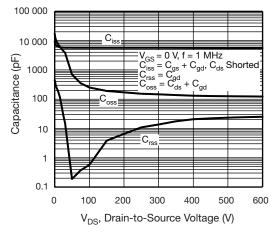


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

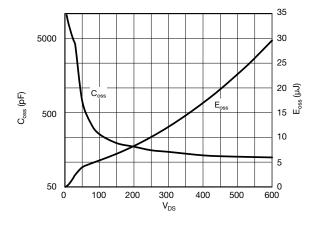


Fig. 6 - Coss and Eoss vs. VDS



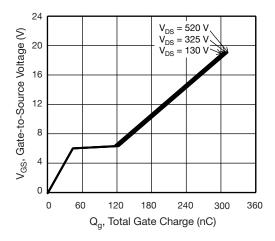


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

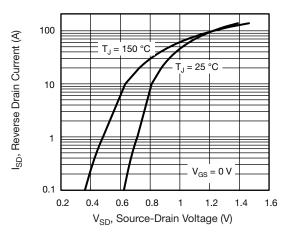


Fig. 8 - Typical Source-Drain Diode Forward Voltage

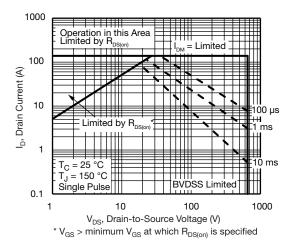


Fig. 9 - Maximum Safe Operating Area

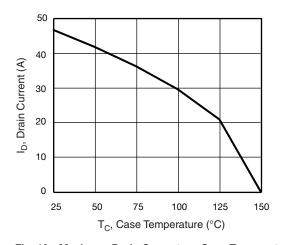


Fig. 10 - Maximum Drain Current vs. Case Temperature

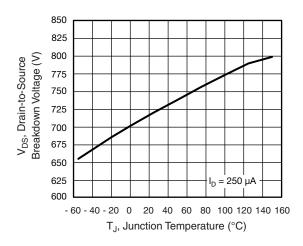


Fig. 11 - Temperature vs. Drain-to-Source Voltage



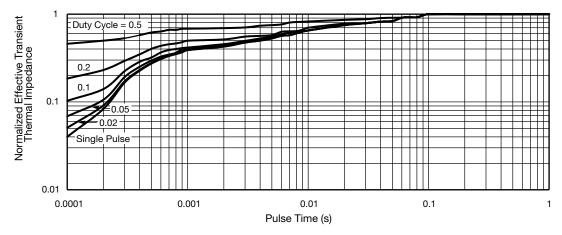


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

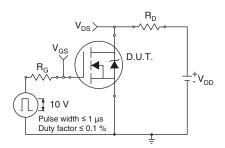


Fig. 13 - Switching Time Test Circuit

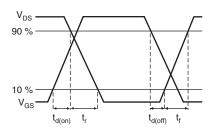


Fig. 14 - Switching Time Waveforms

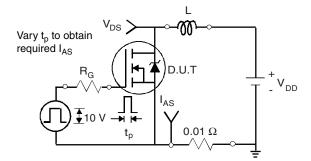


Fig. 15 - Unclamped Inductive Test Circuit

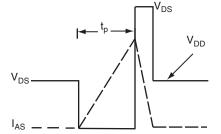


Fig. 16 - Unclamped Inductive Waveforms

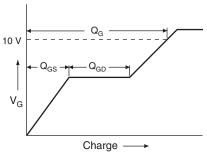


Fig. 17 - Basic Gate Charge Waveform

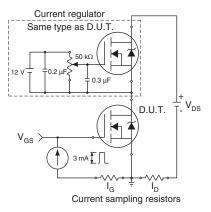
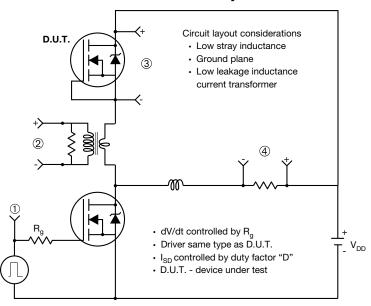


Fig. 18 - Gate Charge Test Circuit



## Peak Diode Recovery dV/dt Test Circuit



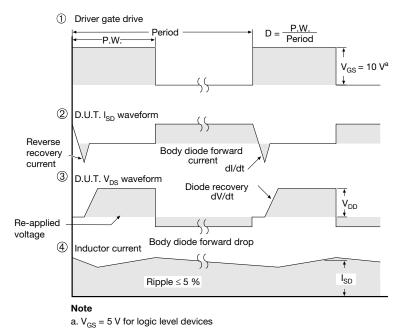


Fig. 19 - For N-Channel



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