

## Features

- 16 or 8-channel 12-Bit SAR ADC
  - Supporting Ranges from 0 to 2.5 V and 0 to 5 V
  - Programmable Out-of-Range Alarms
  - 1-MHz Sample Rate Serial Devices
- General Purpose I/O Ports (GPIOs)
- Low-Power SPI-Compatible Serial Interface
- Operating Temperature: -40°C to 125°C

## Applications

- Wireless Infrastructure
- PLC / DCS
- Battery Powered Systems
- General Purpose Monitor and Control

## Description

The TPC5120/TPC5121 products include capacitor-based SAR A/D converters with inherent sample and hold. The TPC5120 has 16-channel single-ended inputs and the TPC5121 has 8-channel single-ended inputs.

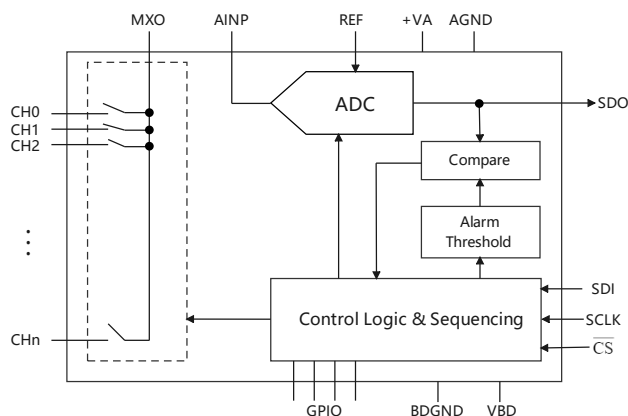
The devices accept a wide analog supply range from 2.7 V to 5.25 V. The ultra-low power consumption makes these devices suitable for battery-powered and isolated power-supply applications.

A wide 1.7-V to 5.25-V I/O supply range facilitates a glueless interface with the most used digital hosts. The serial interface is controlled by  $\overline{CS}$  and SCLK for easy connection with microprocessors and DSP.

The input signal is sampled with the falling edge of  $\overline{CS}$ . It uses SCLK for conversion, serial data output, and reading serial data in. The devices allow auto sequencing of preselected channels or manual selection of a channel for the next conversion cycle. There are two software selectable input ranges (0 V to VREF and 0 V to  $2 \times VREF$ ), individually configurable GPIOs (four in case of the TSSOP and one on the VQFN package devices), and two programmable alarm thresholds per channel. These features make the devices suitable for most data acquisition applications.

The devices offer an attractive power-down feature. This is extremely useful for power saving when the device is operated at lower conversion speeds.

## Functional Block Diagram



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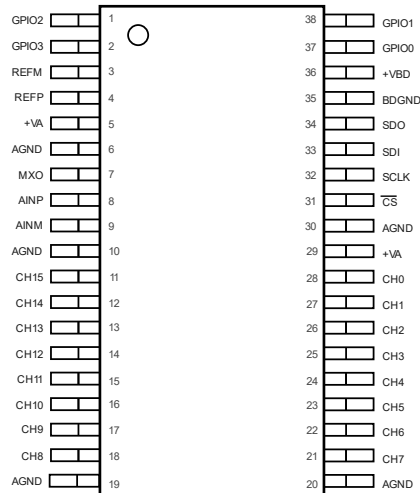
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## Revision History

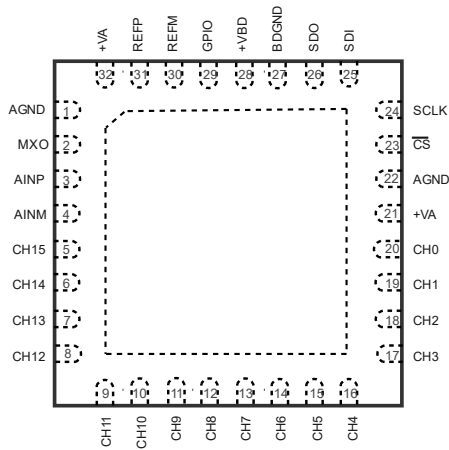
Date	Revision	Notes
2022-01-11	Rev.1.0	Version 1.0

## Pin Configuration and Functions

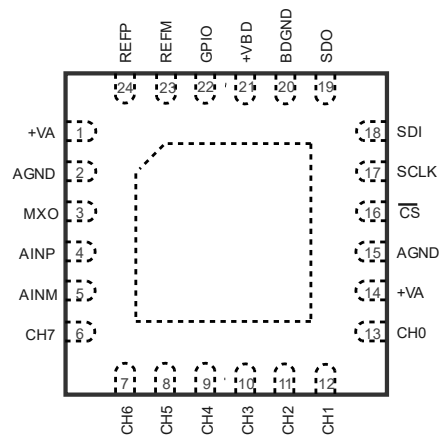
TPC5120  
TSSOP38 Package  
Top View



TPC5120  
QFN32 Package  
Top View



TPC5121  
QFN24 Package  
Top View



## Pin Functions

### TSSOP package

TPC5120		I/O	Description
Pin No.	Pin Name		
3	REFM	Analog input	Reference ground
4	REFP	Analog input	Reference input
8	AINP	Analog input	ADC input signal
9	AINM	Analog input	ADC input ground
7	MXO	Analog output	Multiplexer output
28	Ch0	Analog input	Analog channel for multiplexer
27	Ch1	Analog input	Analog channel for multiplexer
26	Ch2	Analog input	Analog channel for multiplexer
25	Ch3	Analog input	Analog channel for multiplexer
24	Ch4	Analog input	Analog channel for multiplexer
23	Ch5	Analog input	Analog channel for multiplexer
22	Ch6	Analog input	Analog channel for multiplexer
21	Ch7	Analog input	Analog channel for multiplexer
18	Ch8	Analog input	Analog channel for multiplexer
17	Ch9	Analog input	Analog channel for multiplexer
16	Ch10	Analog input	Analog channel for multiplexer
15	Ch11	Analog input	Analog channel for multiplexer
14	Ch12	Analog input	Analog channel for multiplexer
13	Ch13	Analog input	Analog channel for multiplexer
12	Ch14	Analog input	Analog channel for multiplexer
11	Ch15	Analog input	Analog channel for multiplexer
31	$\overline{CS}$	Digital input	Chip-select input pin; active low
32	SCLK	Digital input	Serial clock input pin
33	SDI	Digital input	Serial data input pin
34	SDO	Digital output	Serial data output pin
37	GPIO0	Digital I/O	General-purpose input or output
	Alarm	Digital output	Active high alarm output.
38	GPIO1	Digital I/O	General-purpose input or output
	Low alarm	Digital output	Active high output indicating low alarm
1	GPIO2	Digital I/O	General-purpose input or output
	Range	Digital input	Selects ADC input range: High (1) → Range 2 (0 to 2xVREF) / Low (0) → Range 1 (0 to VREF)
2	GPIO3	Digital I/O	General-purpose input or output
	PD	Digital input	Active low power-down input
5, 29	+V <sub>A</sub>	—	Analog power supply
6, 10, 19, 20, 30	AGND	—	Analog ground
36	+V <sub>BD</sub>	—	Digital I/O supply
35	BDGND	—	Digital ground
—	—	—	Pins internally not connected, do not float these pins, connect these pins to ground

**QFN Package**

Pin Number		Pin Name	I/O	Description
TPC5120	TPC5121			
31	24	REFP	Analog input	Reference input
30	23	REFM	Analog input	Reference ground
3	4	AINP	Analog input	ADC input signal
4	5	AINM	Analog input	ADC input ground
2	3	MXO	Analog output	Multiplexer output
20	13	Ch0	Analog input	Analog-input channel for multiplexer
19	12	Ch1	Analog input	Analog-input channel for multiplexer
18	11	Ch2	Analog input	Analog-input channel for multiplexer
17	10	Ch3	Analog input	Analog-input channel for multiplexer
16	9	Ch4	Analog input	Analog-input channel for multiplexer
15	8	Ch5	Analog input	Analog-input channel for multiplexer
14	7	Ch6	Analog input	Analog-input channel for multiplexer
13	6	Ch7	Analog input	Analog-input channel for multiplexer
12	—	Ch8	Analog input	Analog-input channel for multiplexer
11	—	Ch9	Analog input	Analog-input channel for multiplexer
10	—	Ch10	Analog input	Analog-input channel for multiplexer
9	—	Ch11	Analog input	Analog-input channel for multiplexer
8	—	Ch12	Analog input	Analog-input channel for multiplexer
7	—	Ch13	Analog input	Analog-input channel for multiplexer
6	—	Ch14	Analog input	Analog-input channel for multiplexer
5	—	Ch15	Analog input	Analog-input channel for multiplexer
23	16	$\overline{\text{CS}}$	Digital input	Chip-select input pin; active low
24	17	SCLK	Digital input	Serial clock input pin
25	18	SDI	Digital input	Serial data input pin
26	19	SDO	Digital output	Serial data output pin
29	22	GPIO0	Digital I/O	General purpose input or output
		Alarm	Digital output	Active high alarm output.
21, 32	1, 14	+V <sub>A</sub>	—	Analog power supply
1, 22	2, 15	AGND	—	Analog ground
28	21	+V <sub>BD</sub>	—	Digital I/O supply
27	20	BDGND	—	Digital ground
—	—	—	—	Pins internally not connected, do not float these pins, connect these pins to ground

## Specifications

### Absolute Maximum Ratings <sup>(1)</sup>

Parameters	Min	Max	Unit
AINP or CHn to AGND	-0.3	$V_A + 0.3$	V
+V <sub>A</sub> to AGND, +V <sub>BD</sub> to BDGND	-0.3	7	V
Digital Input Voltage to BDGND	-0.3	7	V
Digital Output to BDGND	-0.3	$V_A + 0.3$	V
Input Current to any Pin except Supply Pins	-10	10	mA
Operating Temperature	-40	125	°C
Junction Temperature (T <sub>J</sub> Max)	150		°C
Storage Temperature (T <sub>sig</sub> )	-65	150	°C

\* (1): Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. The input and output voltage ratings may be exceeded if the input and output diode current ratings are observed.

### ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1.5	kV

### Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V <sub>A</sub>	Analog Power-supply Voltage	2.7		5.25	V
V <sub>BD</sub>	Digital I/O-supply Voltage	1.7	3.3	V <sub>VA</sub>	V
V <sub>REF</sub>	Reference Voltage	2	2.5	V <sub>A</sub>	V
f <sub>SCLK</sub>	SCLK Frequency		20		MHz
T <sub>A</sub>	Operating Temperature Range	-40		125	°C

### Thermal Information

Thermal Metric		TSSOP38	Unit
R <sub>θJA</sub>	Junction-to-ambient Thermal Resistance	83.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) Thermal Resistance	29.8	°C/W
R <sub>θJB</sub>	Junction-to-board Thermal Resistance	44.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top Characterization parameter	2.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board Characterization parameter	44.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) Thermal Resistance	N/A	°C/W

### Electrical Characteristics

All test conditions:  $+V_A = 2.7\text{ V to }5.25\text{ V}$ ,  $+V_{BD} = 1.7\text{ V to }V_A$ ,  $V_{REF} = 2.5\text{ V} \pm 0.1\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$ ,  $f_{\text{sample}} = 1\text{ MHz}$ , unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>ANALOG INPUT</b>					
Full-scale Input Span	Range 1	0		$V_{REF}$	V
	Range 2 while $2V_{REF} \leq +V_A$	0		$2*V_{REF}$	V
Absolute Input Range	Range 1	-0.2		$V_{REF}+0.2$	V
	Range 2 while $2V_{REF} \leq +V_A$	-0.2		$2*V_{REF}+0.2$	V
Input Capacitance			22		pF
Input Leakage Current	$T_A = 25^\circ\text{C}$		30		nA
<b>SYSTEM PERFORMANCE</b>					
Resolution			12		Bits
No Missing Code Resolution		12			Bits
Integral linearity	$F_{\text{sample}} = 750\text{ kHz}$	-1	$\pm 0.4$	1	LSB <sup>3</sup>
	$F_{\text{sample}} = 1\text{ MHz}$	-1.5		1.5	LSB <sup>3</sup>
Differential linearity	$F_{\text{sample}} = 750\text{ kHz}$	-0.99	$\pm 0.5$	1	LSB <sup>3</sup>
	$F_{\text{sample}} = 1\text{ MHz}$	-0.99		1.5	LSB <sup>3</sup>
Offset Error		-4	$\pm 0.5$	4	LSB
Total Unadjusted Error (TUE)			$\pm 3$		LSB
Gain Error	TPC5120	-2	$\pm 1$	2	LSB
	TPC5121, Gain=1X	-2.5	$\pm 1$	2.5	LSB
	TPC5121, Gain=2X	-3	$\pm 1$	3	LSB
<b>SAMPLING DYNAMICS</b>					
Conversion Time	20 MHz sclk			800	ns
Acquisition Time		300			ns
Maximum Throughput Rate	20 MHz sclk			1	MHz
Aperture Delay			5		ns
<b>DYNAMIC CHARACTERISTICS</b>					
Total Harmonic Distortion	100 kHz, -1 dB input		-82		dB
Signal-to-noise Ratio	100 kHz, -1 dB input		71		dB
Signal-to-noise + Distortion	100 kHz, -1 dB input		70		dB
Small Signal Bandwidth	At -3 dB		47		MHz
Channel-to-channel Crosstalk	All off-channel with 100 kHz, Full-scale input to the channel being sampled with DC input (isolation crosstalk).		-80		
	From previously sampled to channel with 100 kHz, full-scale input to the channel being sampled with DC input (memory crosstalk).		-80		



### Electrical Characteristics (Continued)

All test conditions:  $+V_A = 2.7\text{ V to }5.25\text{ V}$ ,  $+V_{BD} = 1.7\text{ V to }V_A\text{ V}$ ,  $V_{REF} = 2.5\text{ V} \pm 0.1\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$ ,  $f_{\text{sample}} = 1\text{ MHz}$ , unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Unit
<b>Internal REFERENCE Output (TPC5121)</b>						
V <sub>REF</sub> Reference Voltage at REFP			2.48	2.5	2.52	V
<b>EXTERNAL REFERENCE INPUT</b>						
V <sub>REF</sub> Reference Voltage at REFP			2	2.5	V <sub>A</sub>	V
Reference Resistance				16		kΩ
<b>ALARM SETTING</b>						
Higher Threshold Range			0		FFC	Hex
Lower Threshold Range			0		FFC	Hex
<b>DIGITAL INPUT/OUTPUT</b>						
Logic Family		CMOS				
Logic Level	V <sub>IH</sub>		0.7*(+V <sub>BD</sub> )			V
	V <sub>IL</sub>	+V <sub>BD</sub> = 5 V			0.3*V <sub>BD</sub>	V
	V <sub>OH</sub>	At I <sub>source</sub> = 200 μA	V <sub>BD</sub> - 0.2			V
	V <sub>OL</sub>	At I <sub>sink</sub> = 200 μA			0.4	V
Data Format MSB First			MSB First			
<b>POWER SUPPLY REQUIREMENTS</b>						
+V <sub>A</sub> Supply Voltage			2.7	3.3	5.5	V
+V <sub>BD</sub> Supply Voltage			1.7	3.3	5.5	V
Supply Current (Normal Mode)		1-MHz throughput		3.8		mA
		static state		1.65		mA
Power-down State Supply Current				10		μA
+V <sub>BD</sub> Supply Current		+V <sub>A</sub> = 5.5 V, f <sub>s</sub> = 1 MHz		10		μA
Power-up Time				1		μs
Invalid Conversions after Power up or Reset				1		Numbers
<b>TEMPERATURE RANGE</b>						
Specified Performance			-40		125	°C

### Timing Requirements

Parameter	Conditions	Min.	Typ	Max.	Unit
$t_{conv}$	Conversion time	+V <sub>BD</sub> = 1.8 V		16	SCLK
		+ V <sub>BD</sub> = 3 V		16	
		+ V <sub>BD</sub> = 5 V		16	
$t_q$	Minimum quiet sampling time needed from bus 3-state to start of next conversion	+ V <sub>BD</sub> = 1.8 V	40		ns
		+ V <sub>BD</sub> = 3 V	40		
		+ V <sub>BD</sub> = 5 V	40		
$t_{d1}$	Delay time, $\overline{CS}$ low to first data (DO-15) out	+ V <sub>BD</sub> = 1.8 V		38	ns
		+ V <sub>BD</sub> = 3 V		27	
		+ V <sub>BD</sub> = 5 V		17	
$t_{su1}$	Setup time, $\overline{CS}$ low to first rising edge of SCLK	+ V <sub>BD</sub> = 1.8 V	8		ns
		+ V <sub>BD</sub> = 3 V	6		
		+ V <sub>BD</sub> = 5 V	4		
$t_{d2}$	Delay time, SCLK falling to SDO next data bit valid	+ V <sub>BD</sub> = 1.8 V		35	ns
		+ V <sub>BD</sub> = 3 V		27	
		+ V <sub>BD</sub> = 5 V		17	
$t_{h1}$	Hold time, SCLK falling to SDO data bit valid	+ V <sub>BD</sub> = 1.8 V	7		ns
		+ V <sub>BD</sub> = 3 V	5		
		+ V <sub>BD</sub> = 5 V	3		
$t_{d3}$	Delay time, 16 <sup>th</sup> SCLK falling edge to SDO 3-state	+ V <sub>BD</sub> = 1.8 V		26	ns
		+ V <sub>BD</sub> = 3 V		22	
		+ V <sub>BD</sub> = 5 V		13	
$t_{su2}$	Setup time, SDI valid to the rising edge of SCLK	+ V <sub>BD</sub> = 1.8 V	2		ns
		+ V <sub>BD</sub> = 3 V	3		
		+ V <sub>BD</sub> = 5 V	4		
$t_{h2}$	Hold time, the rising edge of SCLK to SDI valid	+ V <sub>BD</sub> = 1.8 V	12		ns
		+ V <sub>BD</sub> = 3 V	10		
		+ V <sub>BD</sub> = 5 V	6		
$t_{w1}$	Pulse duration $\overline{CS}$ high	+ V <sub>BD</sub> = 1.8 V	20		ns
		+ V <sub>BD</sub> = 3 V	20		
		+ V <sub>BD</sub> = 5 V	20		
$t_{d4}$	Delay time $\overline{CS}$ high to SDO 3-state	+ V <sub>BD</sub> = 1.8 V		24	ns
		+ V <sub>BD</sub> = 3 V		21	
		+ V <sub>BD</sub> = 5 V		12	
$t_{wh}$	Pulse duration SCLK high	+ V <sub>BD</sub> = 1.8 V	20		ns
		+ V <sub>BD</sub> = 3 V	20		
		+ V <sub>BD</sub> = 5 V	20		
$t_{wl}$	Pulse duration SCLK low	+ V <sub>BD</sub> = 1.8 V	20		ns
		+ V <sub>BD</sub> = 3 V	20		
		+ V <sub>BD</sub> = 5 V	20		
Frequency SCLK		+ V <sub>BD</sub> = 1.8 V		20	MHz
		+ V <sub>BD</sub> = 3 V		20	
		+ V <sub>BD</sub> = 5 V		20	

### Typical Performance Characteristics

All test condition is  $V_{DD} = 3.3\text{ V}$ ,  $T_A = +25^\circ\text{C}$ ,  $R_L = 150\ \Omega$  to GND, unless otherwise noted.

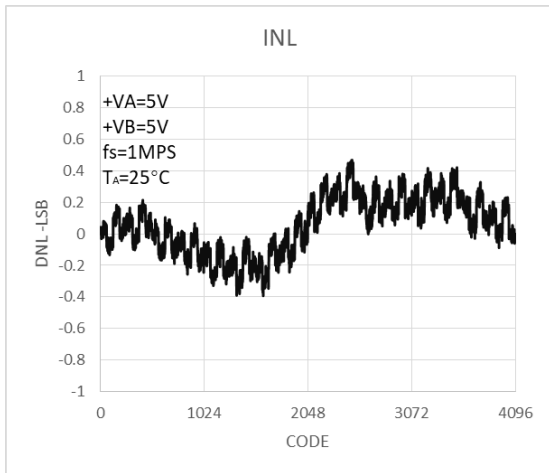


Figure 1. INL

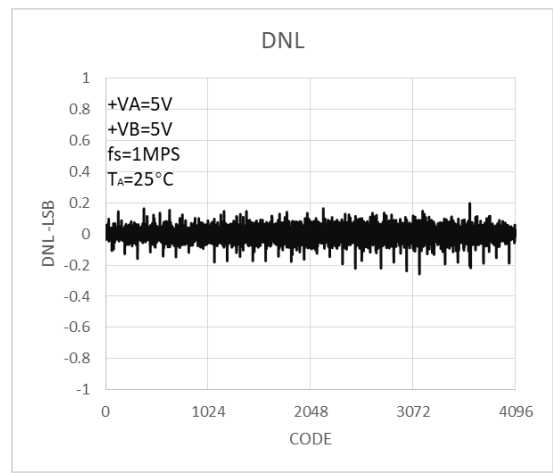


Figure 2. DNL

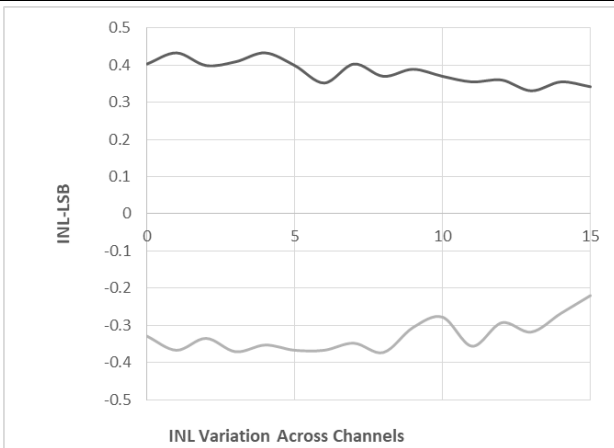


Figure 3. INL across Channels

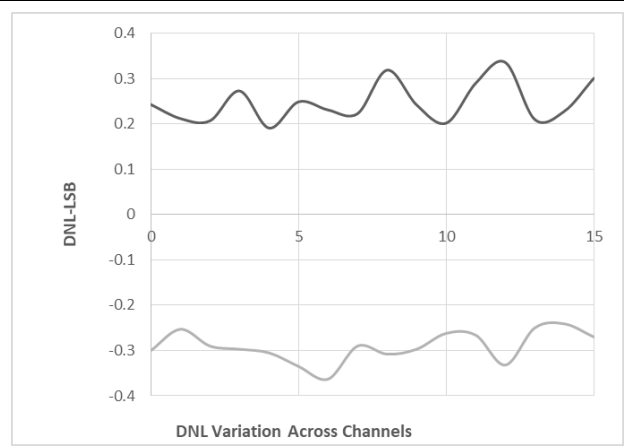


Figure 4. DNL across Channels

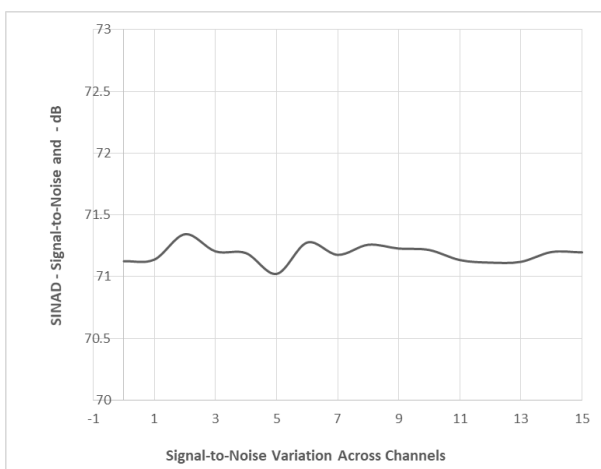


Figure 5. SNR across Channels

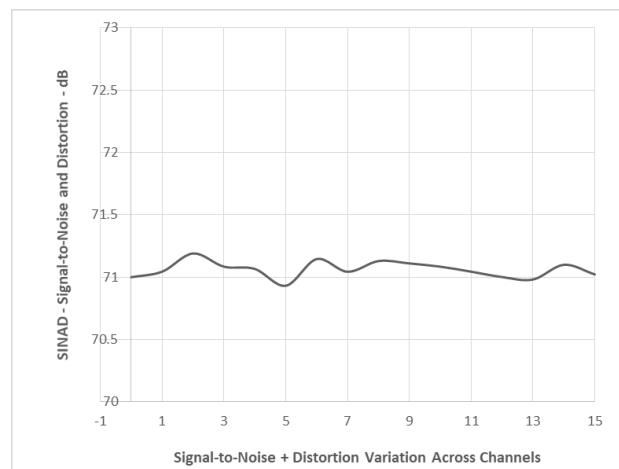


Figure 6. SINAD across Channels

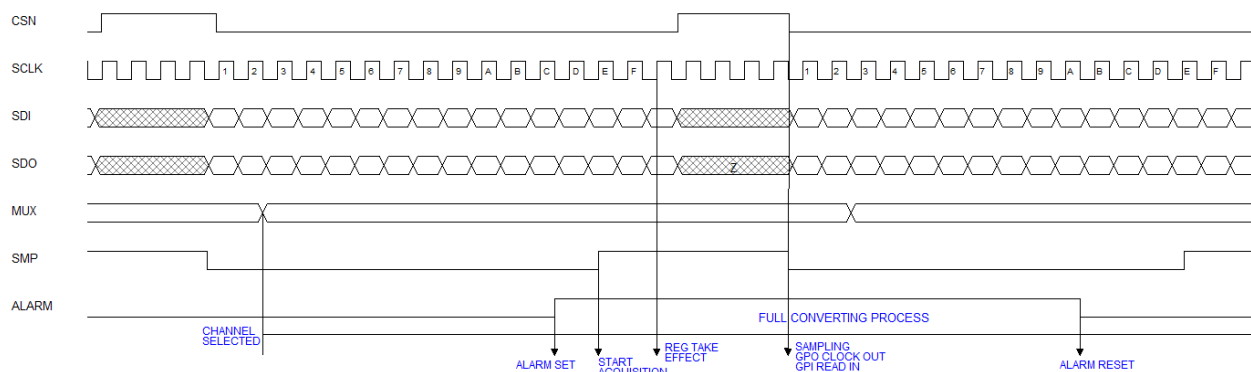
## Detail description

### Overview

The TPC512x series of products are 12-bit multichannel, high-speed, low-power, real-time-converting, capacitor-based, and successive approximation register (SAR) analog-to-digital converters (ADC) that use external references.

The architecture is based on capacitor charge redistribution, which inherently includes a sample/hold function. The sampling point can be controlled with great precision in time by CSN's falling edge.

The analog inputs to the TPC512x are provided to CHx input channels, all input channels share a common reference ground (AINM). The TPC512x has a multiplexer breakout feature which allows to connect the signal conditioning circuit between the multiplexer output (MXO) and the ADC input (AINP). This feature enables the use of common signal conditioning block for the input signal which exhibits similar performance characteristics.



**Figure 7**

The TPC512x can be programmed to select a channel manually or can be programmed into the auto channel select mode to sweep through the input channels automatically.

Each frame begins with the falling edge of CSN. With the falling edge of CSN, the input signal from the selected channel is sampled, and the conversion process is initiated. While the conversion is in progress, the device outputs data at the same time. The 16-bit data word contains a 4-bit head data (which could be configured as channel address or GPIO status), followed by a 12-bit conversion result in MSB first format.

The device outputs DO15 (first bit of 4-bit head data) on the falling edge of CSN, and outputs DO14~DO0 on the subsequent falling edge of SCLK.

If the user configures the input channel to CHx in [N-2]<sup>th</sup> frame. The device selects CHx on the 2nd SCLK falling edge in the [N-1]<sup>th</sup> frame. The device starts the acquisition phase of CHx on the 14th SCLK rising edge in the [N-1]<sup>th</sup> frame. The device ends the acquisition phase and samples the CHx signal on the CSN falling edge in the [N]<sup>th</sup> frame. And the device outputs the conversion result on the subsequent SCLK falling edge in the [N]<sup>th</sup> frame.

The device offers a 1X/2X input range feature. There are two ways to change the input range. The input range can be changed to 2X by writing DI06 = 1 in the mode control register; in this case, the register is written in on the 16th SCLK rising edge of this frame. And because the input range change is implemented by changing the sampling capacitor. The register takes effect in the acquisition phase in the next frame and affects the output conversion data in the third frame.

Another way to change the input range is through GPIO in the case of the TSSOP packaged devices. GPIO2 can act as the RangeSel input. The RangeSel signal takes effect in the next acquisition phase.

The TSSOP packaged devices have four General Purpose IO(GPIO) pins while QFN versions have only one GPIO. These four pins can be individually programmed as GPO or GPI. It is also possible to use them for pre-assigned functions. GPO data can be written into the device through the SDI line. The device refreshes the GPO data on the CSN falling edge as per the SDI data written in the previous frame.

Similarly, the device latches the GPI status on the CSN falling edge and outputs the GPI data on the SDO line in the same frame starting with the CSN falling edge.

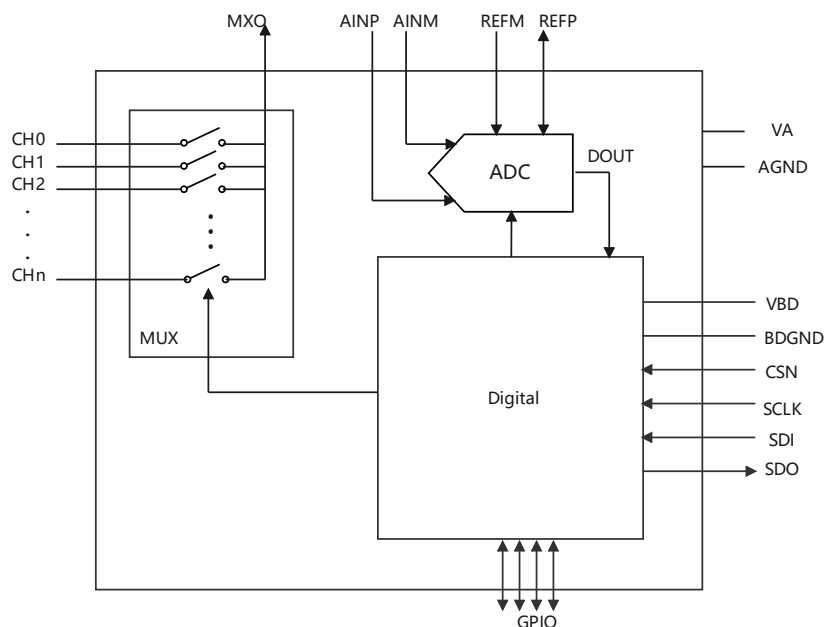
The device has two (high and low) programmable alarm thresholds per channel. If the input crosses these limits, the device flags out an alarm on GPIO0/GPIO1 depending on the GPIO program register setting. The alarm is asserted (under the alarm conditions) on the 12th SCLK falling edge in the same frame when data conversion is in progress. The alarm outputs are reset on the 10th falling edge of SCLK in the next frame.

The device offers a power-down feature to save power when not in use. There are two ways to power down the device. It can be powered down by writing DI05 = 1 in the mode control register; in this case the device powers down on the 16th falling edge of SCLK in the next frame. The device will power up again with DI05 = 0 in the mode control register.

E.g. if the user configures mode control register DI05 = 1 in the [N-2]<sup>th</sup> frame. The register writes in on the 16<sup>th</sup> SCLK rising edge in the [N-2]<sup>th</sup> frame. ADC works properly in the [N-1]<sup>th</sup> frame. The device powers down ADC on the 16th SCLK falling edge in the [N-1]<sup>th</sup> frame. The device goes into power-down mode in the [N]<sup>th</sup> frame. And if the user configures mode control register DI05 = 0 in the [N+1]<sup>th</sup> frame. The register writes in on the 16th SCLK rising edge in the [N+1]<sup>th</sup> frame, and the device powers on in the [N+1]<sup>th</sup> frame. After 1 frame analog settling time, the ADC works properly in the [N+2]<sup>th</sup> frame.

Another way to power down the device is through GPIO in the case of the TSSOP packaged devices. GPIO3 can act as the PDN input. This is an asynchronous and active low input. The device powers down instantaneously after GPIO3(PDN) = 0.

### Functional block diagram

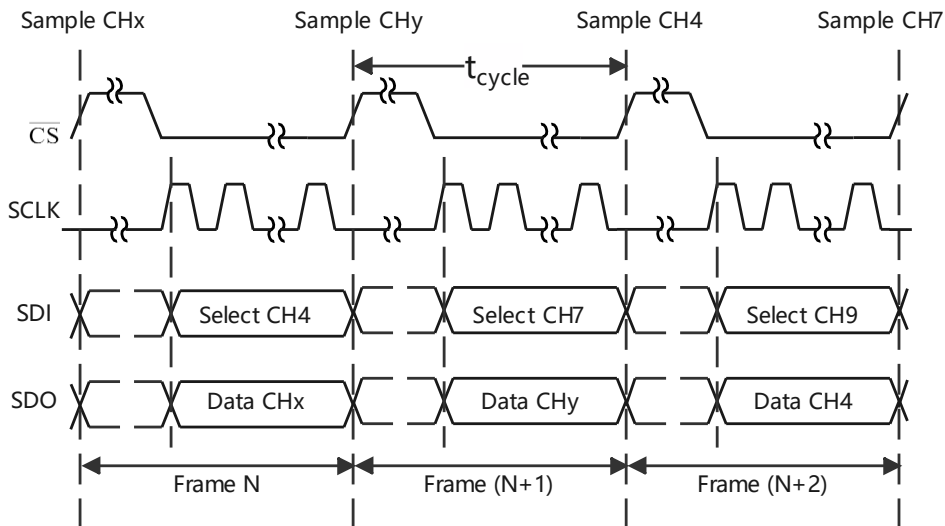


**Figure 8 Functional Block Diagram**

## Feature description

### Device Functional Modes

#### Channel Sequencing Modes

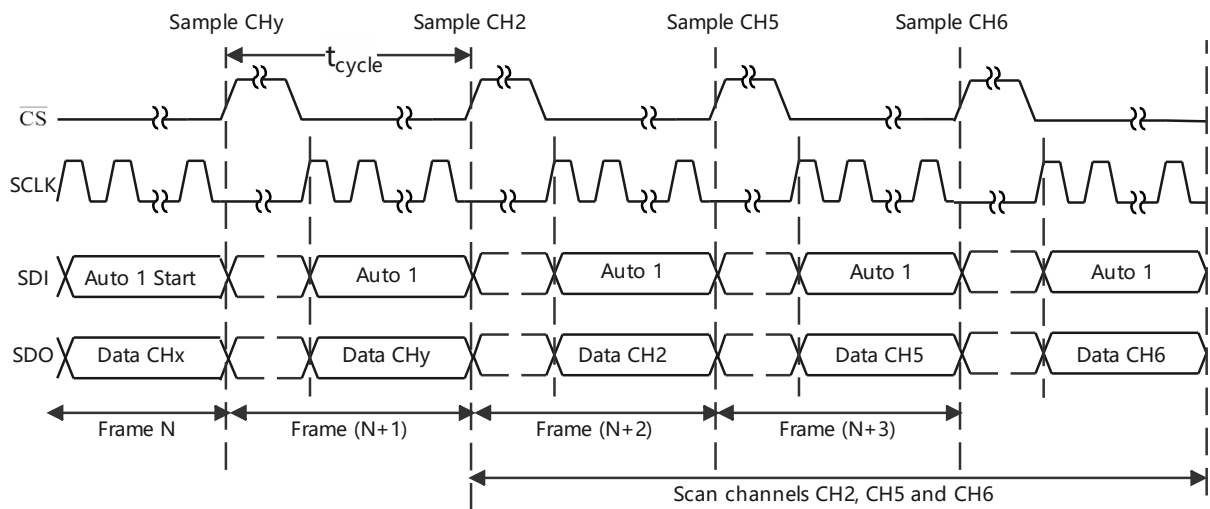


**Figure 9 Example Manual Mode Timing Diagram**

**Table 1 Mode Control Register Settings for Manual Mode**

Bits	Reset State	Logic State	Function										
DI15-12	0001	0001	Selects Manual Mode										
DI11	0	1	Enables programming of bits DI06-00.										
		0	Device retains values of DI06-00 from the previous frame.										
DI10-07	0000	This four-bit data represents the address of the next channel to be selected in the next frame. DI10: MSB and DI07: LSB. For example, 0000 represents channel-0, 0001 represents channel-1 and so forth.											
DI06	0	0	Selects 0 to $V_{REF}$ input range (Range 1)										
		1	Selects 0 to $2XV_{REF}$ input range (Range 2)										
DI05	0	0	Device normal operation (no power-down)										
		1	Device powers down on 16th SCLK falling edge										
DI04	0	0	SDO outputs the current channel address of the channel on DO15..12 followed by 12 bit conversion result on DO11..00.										
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.										
			<table border="1" style="width: 100%; text-align: center;"> <tr> <td>DOI5</td> <td>DOI4</td> <td>DOI3</td> <td>DOI2</td> </tr> <tr> <td>GPIO3 <sup>(1)</sup></td> <td>GPIO2 <sup>(1)</sup></td> <td>GPIO1 <sup>(1)</sup></td> <td>GPIO0 <sup>(1)</sup></td> </tr> </table>	DOI5	DOI4	DOI3	DOI2	GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>		
DOI5	DOI4	DOI3	DOI2										
GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>										
DI03-00	0000	GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below											
		<table border="1" style="width: 100%; text-align: center;"> <tr> <td>DI03</td> <td>DI02</td> <td>DI01</td> <td>DI00</td> </tr> <tr> <td>GPIO3 <sup>(1)</sup></td> <td>GPIO2 <sup>(1)</sup></td> <td>GPIO1 <sup>(1)</sup></td> <td>GPIO0 <sup>(1)</sup></td> </tr> </table>				DI03	DI02	DI01	DI00	GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>
		DI03	DI02	DI01	DI00								
GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>										
<table border="1" style="width: 100%; text-align: center;"> <tr> <td>DI03</td> <td>DI02</td> <td>DI01</td> <td>DI00</td> </tr> <tr> <td>GPIO3 <sup>(1)</sup></td> <td>GPIO2 <sup>(1)</sup></td> <td>GPIO1 <sup>(1)</sup></td> <td>GPIO0 <sup>(1)</sup></td> </tr> </table>				DI03	DI02	DI01	DI00	GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>		
DI03	DI02	DI01	DI00										
GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>										

**Note:** (1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.



**Figure 10 Example Auto-1 Mode Timing Diagram**

**Table 2 Mode Control Register Settings for Auto-1 Mode**

Bits	Reset State	Logic State	Function			
DI15-12	0001	0010	Selects Auto-1 Mode			
DI11	0	1	Enables programming of bits DI10-00.			
		0	Device retains values of DI10-00 from the previous frame.			
DI10	0	1	The channel counter is reset to the lowest programmed channel in the Auto-1 Program Register			
		0	The channel counter increments every conversion (No reset)			
DI09-07	000	xxx	Do not care			
DI06	0	0	Selects 0 to $V_{REF}$ input range (Range 1)			
		1	Selects 0 to $2xV_{REF}$ input range (Range 2)			
DI05	0	0	Device normal operation (no power-down)			
		1	Device powers down on the 16th SCLK falling edge			
DI04	0	0	SDO outputs current channel address of the channel on DO15..12 followed by 12-bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>
DI03-00	0000	GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below				
			DI03	DI02	DI01	DI00
			GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>

**Note:** (1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

**Table 3 Program Register Settings for Auto-1 Mode**

Bits	Reset State	Logic State	Function
<b>FRAME 1</b>			
DI15-12	NA	1000	Device enters the Auto-1 program sequence. Device programming is done in the next frame.
DI11-00	NA	Do not care	
<b>FRAME 2</b>			
DI15-00	All 1s	1 (individual bit)	A particular channel is programmed to be selected in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits, for example, DI15 → Ch15, DI14 → Ch14 ... DI00 → Ch00
		0 (individual bit)	A particular channel is programmed to be skipped in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits, for example DI15 → Ch15, DI14 → Ch14 ... DI00 → Ch00



**Table 4 Mapping of Channels to SDI Bits for 16, 12, 8, 4 Channel Devices**

Device *	SDI Bits															
	DI1 5	DI1 4	DI1 3	DI1 2	DI1 1	DI1 0	DI0 9	DI0 8	DI0 7	DI0 6	DI0 5	DI0 4	DI0 3	DI0 2	DI0 1	DI0 0
16 Chan	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
12 Chan	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
8 Chan	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
4 Chan	X	X	X	X	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0

**Note:**\* When operating in Auto-1 mode, the device only scans the channels programmed to be selected.

**Table 5 Mode Control Register Settings for Auto-2 Mode**

Bits	Reset State	Logic State	Function								
DI15-12	0001	0011	Selects Auto-2 Mode								
DI11	0	1	Enables programming of bits DI10-00.								
		0	Device retains values of DI10-00 from the previous frame.								
DI10	0	1	Channel number is reset to Ch-00.								
		0	Channel counter increments every conversion. (No reset).								
DI09-07	000	xxx	Do not care								
DI06	0	0	Selects $V_{REF}$ i/p range (Range 1)								
		1	Selects $2xV_{REF}$ i/p range (Range 2)								
DI05	0	0	Device normal operation (no power-down)								
		1	Device powers down on the 16th SCLK falling edge								
DI04	0	0	SDO outputs the current channel address of the channel on DO15..12 followed by the 12-bit conversion result on DO11..00.								
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.								
			<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DO15</td> <td style="width: 25%;">DO14</td> <td style="width: 25%;">DO13</td> <td style="width: 25%;">DO12</td> </tr> <tr> <td>GPIO3 <sup>(1)</sup></td> <td>GPIO2 <sup>(1)</sup></td> <td>GPIO1 <sup>(1)</sup></td> <td>GPIO0 <sup>(1)</sup></td> </tr> </table>	DO15	DO14	DO13	DO12	GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>
DO15	DO14	DO13	DO12								
GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>								
DI03-00	0000		GPIO data for the channels configured as output. Device ignores data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below:								
			<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DI03</td> <td style="width: 25%;">DI02</td> <td style="width: 25%;">DI01</td> <td style="width: 25%;">DI00</td> </tr> <tr> <td>GPIO3 <sup>(1)</sup></td> <td>GPIO2 <sup>(1)</sup></td> <td>GPIO1 <sup>(1)</sup></td> <td>GPIO0 <sup>(1)</sup></td> </tr> </table>	DI03	DI02	DI01	DI00	GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>
DI03	DI02	DI01	DI00								
GPIO3 <sup>(1)</sup>	GPIO2 <sup>(1)</sup>	GPIO1 <sup>(1)</sup>	GPIO0 <sup>(1)</sup>								

**Note:** (1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

**Table 6 Program Register Settings for Auto-2 Mode**

Bits	Reset State	Logic State	Function
DI15-12	NA	1001	Auto-2 program register is selected for programming
DI11-10	NA		Do not care
DI09-06	NA	aaaa	This 4-bit data represents the address of the last channel in the scanning sequence. During device operation in Auto-2 mode, the channel counter starts at CH-00 and increments every frame until it equals "aaaa". The channel counter rolls over to CH-00 in the next frame.
DI05-00	NA		Do not care

**Table 7 Continued Operation in a Selected Mode**

Bits	Reset State	Logic State	Function
DI15-12	0001	0000	The device continues to operate in the selected mode. In Auto-1 and Auto-2 modes the channel counter increments normally, whereas in the Manual mode it continues with the last selected channel. The device ignores data on DI11-DI00 and continues operating as per the previous settings. This feature is provided so that SDI can be held low when no changes are required in the Mode Control Register settings.
DI11-00	All '0'	Device ignores these bits when DI15-12 is set to 0000 logic state	

## Programming

### Digital Output

As described previously in Overview, the digital output of the devices is SPI compatible. The following tables list the output codes corresponding to various analog input voltages.

**Table 8 Ideal Input Voltages and Output Codes**

Description		Analog Value	Digital Output	
Full-scale range	Range 1 → $V_{REF}$	Range 2 → $2 \times V_{REF}$	Straight Binary	
Least significant bit (LSB)	$V_{REF} / 4096$	$2V_{REF} / 4096$	BINARY CODE	HEX CODE
Full scale	$V_{REF} - 1 \text{ LSB}$	$2V_{REF} - 1 \text{ LSB}$	1111 1111 1111	FFF
Midscale	$V_{REF} / 2$	$V_{REF}$	1000 0000 0000	800
Midscale – 1 LSB	$V_{REF} / 2 - 1 \text{ LSB}$	$V_{REF} - 1 \text{ LSB}$	0111 1111 1111	7FF
Zero	0 V	0 V	0000 0000 0000	000

**Table 9 GPIO Program Register Settings**

Bits	Reset State	Logic State	Function
DI15-12	NA	0100	Device selects GPIO Program Registers for programming.
DI11-10	00	00	Do not program these bits to any logic state other than '00'
DI09	0	1	Device resets all registers in the next $\overline{CS}$ frame to the reset state shown in the corresponding tables (it also resets itself).
		0	Device normal operation
DI08	0	1	Device configures GPIO3 as the device power-down input.
		0	GPIO3 remains general purpose I or O. Program 0 for QFN packaged devices.
DI07	0	1	Device configures GPIO2 as device range input.
		0	GPIO2 remains general purpose I or O. Program 0 for QFN packaged devices.
DI06-04	000	000	GPIO1 and GPIO0 remain general purpose I or O. Valid setting for QFN packaged devices.
		xx1	Device configures GPIO0 as a 'high or low' alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.
		010	Device configures GPIO0 as a high alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.
		100	Device configures GPIO1 as a low alarm output. This is an active high output. GPIO0 remains general purpose I or O. Setting is not allowed for QFN packaged devices.
		110	Device configures GPIO1 as a low alarm output and GPIO0 as a high alarm output. These are active high outputs. Setting is not allowed for QFN-packaged devices.
<b>Note:</b> The following settings are valid for GPIO which are not assigned a specific function through bits DI08..04			
DI03	0	1	GPIO3 pin is configured as a general-purpose output. Program 1 for QFN-packaged devices.
		0	GPIO3 pin is configured as a general-purpose input. The setting is not allowed for QFN packaged devices.
DI02	0	1	GPIO2 pin is configured as a general-purpose output. Program 1 for QFN-packaged devices.
		0	GPIO2 pin is configured as a general-purpose input. The setting is not allowed for QFN-packaged devices.
DI01	0	1	GPIO1 pin is configured as a general-purpose output. Program 1 for QFN packaged devices.

		0	GPIO1 pin is configured as a general-purpose input. The setting is not allowed for QFN packaged devices.
DI00	0	1	GPIO0 pin is configured as a general-purpose output. Valid setting for QFN packaged devices.
		0	GPIO0 pin is configured as a general-purpose input. Valid setting for QFN packaged devices.

**Table 10 Grouping of Alarm Program Registers**

Group No.	Registers	Applicable for Device
0	High and low alarms for channels 0, 1, 2, and 3	TPC5120
1	High and low alarms for channels 4, 5, 6, and 7	TPC5120, TPC5121
2	High and low alarms for channels 8, 9, 10, and 11	TPC5120
3	High and low alarms for channels 12, 13, 14, and 15	TPC5120

**Table 11 Alarm Program Register Settings**

Bits	Reset State	Logic State	Function
<b>FRAME 1</b>			
DI15-12	NA	1100	Device enters 'alarm programming sequence' for group 0
		1101	Device enters 'alarm programming sequence' for group 1
		1110	Device enters 'alarm programming sequence' for group 2
		1111	Device enters 'alarm programming sequence' for group 3
Note: DI15-12 = 11bb is the alarm programming request for group bb. Here 'bb' represents the alarm programming group number in binary format.			
DI11-14	NA		Do not care
<b>FRAME 2 AND ONWARDS</b>			
DI15-14	NA	cc	Where "cc" represents the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number "bbcc". "bb" is programmed in the first frame.
DI13	NA	1	High alarm register selection
		0	Low alarm register selection
DI12	NA	0	Continue the alarm programming sequence in the next frame
		1	Exit Alarm Programming in the next frame. Note: If the alarm programming sequence is not terminated using this feature, then the device will remain in the alarm programming sequence state and all SDI data will be treated as alarm thresholds.
DI11-10	NA	xx	Do not care
DI09-00	All ones for high alarm register and all zeros for low alarm register		This 10-bit data represents the alarm threshold. The 10-bit alarm threshold is compared with the upper 10-bit word of the 12-bit conversion result. The device sets off an alarm when the conversion result is higher (High Alarm) or lower (Low Alarm) than this number. For 10-bit devices, all 10 bits of the conversion result are compared with the set threshold. For 8-bit devices, all 8 bits of the conversion result are compared with DI09 to DI02 and DI00, and 01 are 'do not care'.

## Register Maps

Address	Type	Default	Register Name
4'b0000	W	12'h000	Continued Operation in a Selected Mode
4'b0001	R/W	12'h000	Manual Mode Control Register
4'b0010	R/W	12'h000	Auto-1 Mode Control Register
4'b0011	R/W	12'h000	Auto-2 Mode Control Register
4'b0100	R/W	12'h000	GPIO Program Register
4'b0101	/	12'h000	Reserved and forbidden to read/write.
4'b0110	/	12'h000	Reserved and forbidden to read/write.
4'b0111	R/W	12'h000	Reference enable. This register is only for TPC5121. Reserved for TPC5120.
4'b1000	R/W	16'hfff	Auto-1 Mode Program Register
4'b1001	R/W	12'h3c0	Auto-2 Mode Program Register
4'b1100	W		Group 0 Alarm Program Register
2'b00	R/W	10'h3ff	Channel 0 High Alarm Register
	R/W	10'h000	Channel 0 Low Alarm Register
2'b01	R/W	10'h3ff	Channel 1 High Alarm Register
	R/W	10'h000	Channel 1 Low Alarm Register
2'b10	R/W	10'h3ff	Channel 2 High Alarm Register
	R/W	10'h000	Channel 2 Low Alarm Register
2'b11	R/W	10'h3ff	Channel 3 High Alarm Register
	R/W	10'h000	Channel 3 Low Alarm Register
4'b1101	W		Group 1 Alarm Program Register
2'b00	R/W	10'h3ff	Channel 4 High Alarm Register
	R/W	10'h000	Channel 4 Low Alarm Register
2'b01	R/W	10'h3ff	Channel 5 High Alarm Register
	R/W	10'h000	Channel 5 Low Alarm Register
2'b10	R/W	10'h3ff	Channel 6 High Alarm Register
	R/W	10'h000	Channel 6 Low Alarm Register
2'b11	R/W	10'h3ff	Channel 7 High Alarm Register
	R/W	10'h000	Channel 7 Low Alarm Register
4'b1110	W		Group 2 Alarm Program Register
2'b00	R/W	10'h3ff	Channel 8 High Alarm Register
	R/W	10'h000	Channel 8 Low Alarm Register
2'b01	R/W	10'h3ff	Channel 9 High Alarm Register
	R/W	10'h000	Channel 9 Low Alarm Register
2'b10	R/W	10'h3ff	Channel 10 High Alarm Register
	R/W	10'h000	Channel 10 Low Alarm Register
2'b11	R/W	10'h3ff	Channel 11 High Alarm Register
	R/W	10'h000	Channel 11 Low Alarm Register
4'b1111	W		Group 3 Alarm Program Register
2'b00	R/W	10'h3ff	Channel 12 High Alarm Register
	R/W	10'h000	Channel 12 Low Alarm Register
2'b01	R/W	10'h3ff	Channel 13 High Alarm Register
	R/W	10'h000	Channel 13 Low Alarm Register

2'b10	R/W	10'h3ff	Channel 14 High Alarm Register
	R/W	10'h000	Channel 14 Low Alarm Register
2'b11	R/W	10'h3ff	Channel 15 High Alarm Register
	R/W	10'h000	Channel 15 Low Alarm Register

## Register Identification

**Table 12**

Manual Mode Control Register (4'b0001)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	ManuLSBEn	ManuChnl[3]	ManuChnl[2]	ManuChnl[1]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ManuChnl[0]	ManuRangSel	ManuPd	ManuGPIOEn	ManuGPIOData[3]	ManuGPIOData[2]	ManuGPIOData[1]	ManuGPIOData[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

**Table 13**

Auto-1 Mode Control Register (4'b0010)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	Auto1LSBEn	Auto1ChnlRst	NA	NA
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NA	Auto1RangSel	Auto1Pd	Auto1GPIOEn	Auto1GPIOData[3]	Auto1GPIOData[2]	Auto1GPIOData[1]	Auto1GPIOData[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

**Table 14**

Auto-2 Mode Control Register (4'b0011)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	Auto2LSBEn	Auto2ChnlRst	NA	NA
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NA	Auto2RangSel	Auto2Pd	Auto2GPIOEn	Auto2GPIOData[3]	Auto2GPIOData[2]	Auto2GPIOData[1]	Auto2GPIOData[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

**Table 15**

RefEn Register (4'b0111)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	NA	NA	NA	NA
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NA	NA	NA	NA	NA	NA	RefEn	NA
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1

Note: This register is only for TPC5121.

**Table 16**

GPIO Program Register (4'b0100)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	1'b0	1'b0	GPIORegRst	GPIO3PdlIn

1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GPIO2Rangeln	GPIO10Cfg[2]	GPIO10Cfg[1]	GPIO10Cfg[0]	GPIO3Cfg	GPIO2Cfg	GPIO1Cfg	GPIO0Cfg
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

**Table 17**

Auto-1 Mode Program Register (4'b1000)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Auto1Chnl[15]	Auto1Chnl[14]	Auto1Chnl[13]	Auto1Chnl[12]	Auto1Chnl[11]	Auto1Chnl[10]	Auto1Chnl[9]	Auto1Chnl[8]
1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Auto1Chnl[7]	Auto1Chnl[6]	Auto1Chnl[5]	Auto1Chnl[4]	Auto1Chnl[3]	Auto1Chnl[2]	Auto1Chnl[1]	Auto1Chnl[0]
1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1

**Table 18**

<b>Auto-2 Program Register (4'b1001)</b>							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	NA	NA	Auto2Chnl[3]	Auto2Chnl[2]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Auto2Chnl[1]	Auto2Chnl[0]	NA	NA	NA	NA	NA	NA
1'b1	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

**Table 19**

<b>Group0 Alarm Program Register (4'b1100)</b>							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
ChnlNumLSB[1]	ChnlNumLSB[0]	HiAlarmRegSel	AlarmPgCont	NA	NA	AlarmTh[9]	AlarmTh[8]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AlarmTh[7]	AlarmTh[6]	AlarmTh[5]	AlarmTh[4]	AlarmTh[3]	AlarmTh[2]	AlarmTh[1]	AlarmTh[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

**Table 20**

<b>Group1 Alarm Program Register (4'b1101)</b>							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
ChnlNumLSB[1]	ChnlNumLSB[0]	HiAlarmRegSel	AlarmPgCont	NA	NA	AlarmTh[9]	AlarmTh[8]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AlarmTh[7]	AlarmTh[6]	AlarmTh[5]	AlarmTh[4]	AlarmTh[3]	AlarmTh[2]	AlarmTh[1]	AlarmTh[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

**Table 21**

<b>Group2 Alarm Program Register (4'b1110)</b>							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
ChnlNumLSB[1]	ChnlNumLSB[0]	HiAlarmRegSel	AlarmPgCont	NA	NA	AlarmTh[9]	AlarmTh[8]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AlarmTh[7]	AlarmTh[6]	AlarmTh[5]	AlarmTh[4]	AlarmTh[3]	AlarmTh[2]	AlarmTh[1]	AlarmTh[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

**Table 22**

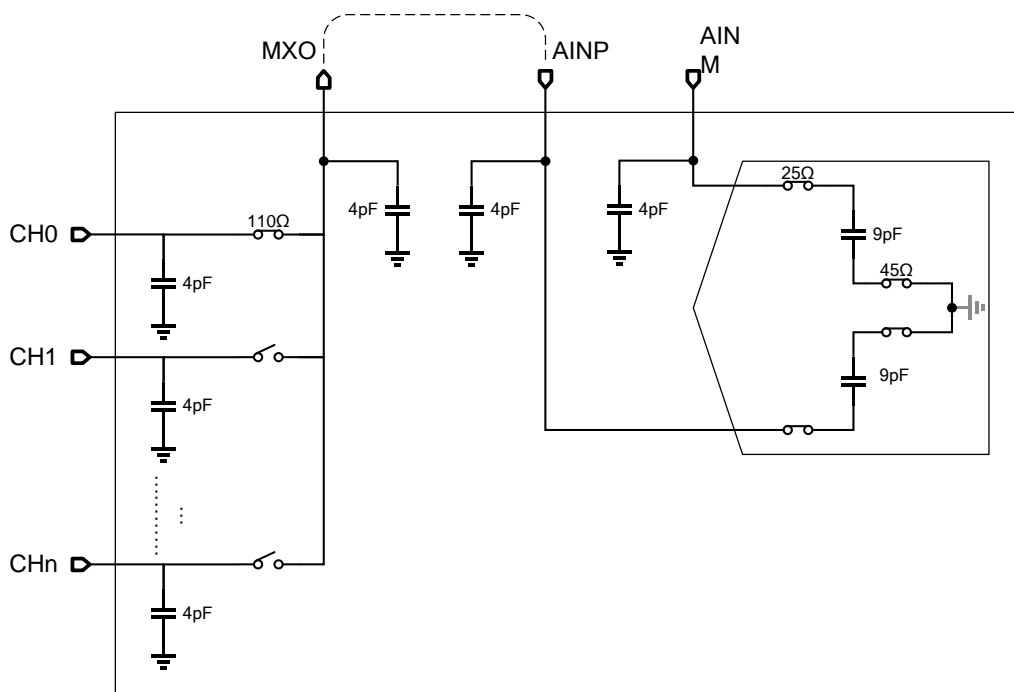
<b>Group3 Alarm Program Register (4'b1111)</b>							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
ChnlNumLSB[1]	ChnlNumLSB[0]	HiAlarmRegSel	AlarmPgCont	NA	NA	AlarmTh[9]	AlarmTh[8]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AlarmTh[7]	AlarmTh[6]	AlarmTh[5]	AlarmTh[4]	AlarmTh[3]	AlarmTh[2]	AlarmTh[1]	AlarmTh[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0



**Table 23**

RefEn & FullDifEn Register (4'b0111)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	NA	NA	NA	NA
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NA	NA	NA	NA	NA	NA	RefEn	Reserved
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1

## Application Information



In general application, the converting process is as below:

1. Multiplexer switch is close (meanwhile, the sampling switch is open, and ADC is in the conversion phase), channel input source charges the parasitic capacitor of MXO/AINP.
2. The sampling switch is close, and the 12-pF sampling capacitor, which is charged to the previously converted channel, is recharged to the current converting channel.
3. The sampling switch opens again. The sampling capacitor holds the signal, and the device goes into the conversion phase.
4. While the conversion is in progress, the device outputs data at the same time. And because the sampling switch is open, the multiplexer switch can switch to another channel freely on the 2nd SCLK rising edge in this phase.
5. Repeat 1~4.

## Analog Input

There are about 22-pF internal capacitors in total. These capacitors consist of pin parasitic capacitors and sampling capacitors. Before the multiplexer switch of the current converting channel close, these capacitors are charged to the previous channel signal. And these capacitors must settle to the current converting channel

signal before the sampling switch opens. Several methods can be adopted to achieve enough performance.

1. Low impedance input source.
2. Large enough CHx decouple capacitor.

Users can tradeoff between source character, performance, and sampling rate.

E.g. Assume source signal voltage 2 V, current saturation less than 1.5 V, source equivalent impedance 1 Kohms, 12-bit resolution requirement. If the previous channel is 0 V, and the 22-pF capacitor should be charged from 0 V to 1.5 V, and step should be higher than 1 V. Then  $C_{CHx} \times 2 V + 22 pF \times 0 V > (C_{CHx} + 22 pF) \times 1.5 V$ ,  $C_{CHx} > 66 pF$ , leave some guard band, 150-pF decouple capacitor should be added to CHx. In order to calculate easily, all internal capacitor is charged in the Acquisition phase. At the beginning of the Acquisition phase, charge balance between channel decouple capacitor and internal capacitor, the initial voltage is  $(C_{CHx} \times 2 V + C_{int} \times 2 V) \div (C_{CHx} + C_{int}) = 1.7 V$ , and the final voltage is 2 V,  $\tau = 1 k\Omega \times (150 pF + 22 pF) = 172 ns$ , and settle err is less than 1LSB=610  $\mu V$ , the Acquisition time should be longer than  $\tau \times \ln((2 V - 1.7 V)/610 \mu V) = 1.06 \mu s$ .

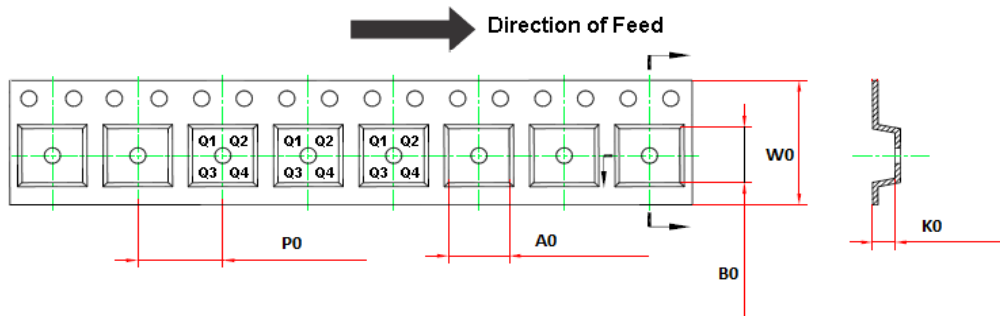
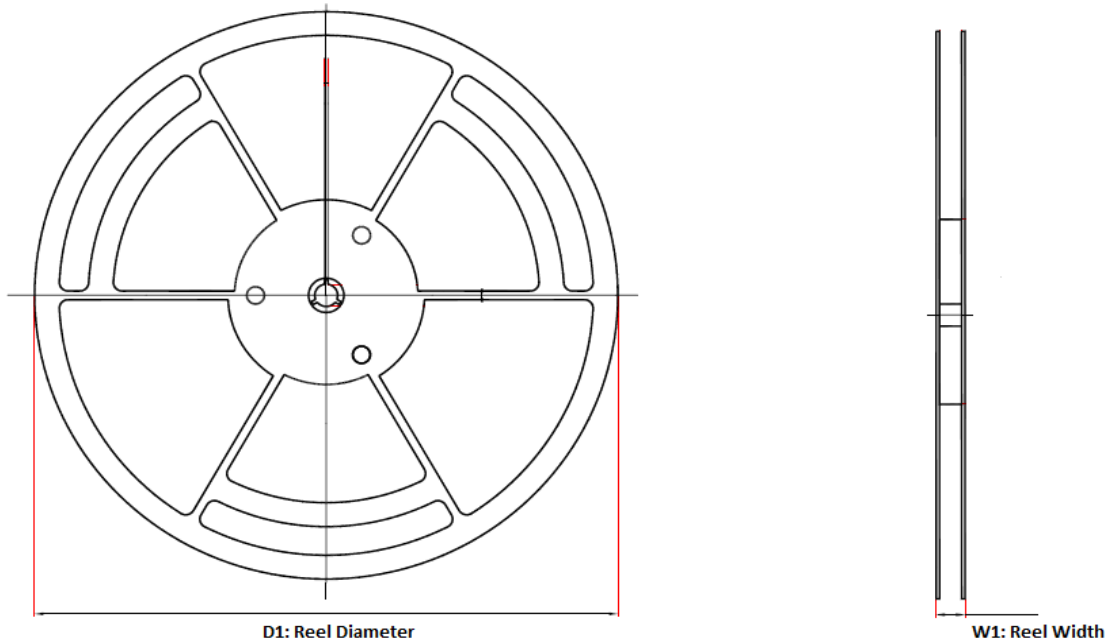
## Reference

The TPC512x can operate with an external 2 V ~ V<sub>A</sub> reference. A clean, low-noise, low-output impedance, and well-decoupled reference voltage on the REFP pin is required to ensure the good performance of the converter. A 10-uf ceramic decoupling capacitor is required between the REFP and REFM pins of the converter. The capacitor should be placed as close as possible to the pins of the device. The connection between REFM and ground should be solid and should be avoided sharing any common path with other devices. Because the reference input resistance of this device is about 16 Kohms, the sum of reference output resistance and total parasitic resistance of REFP and REFM should be less than 4 ohms (which is easy to achieve with careful layout).

## SPI Interface

The device converts input and outputs conversion results simultaneously. In order to reduce the effect of SPI output flipping, the drive capability of this device is weaker than other parts. So lighter SDO capacitive loading is required (less than 20 pF) in the high-speed application.

### Tape and Reel Information



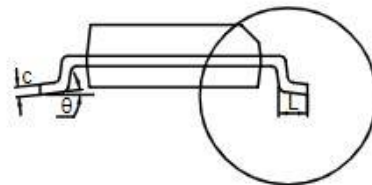
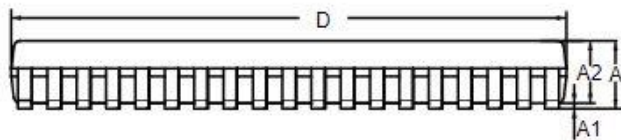
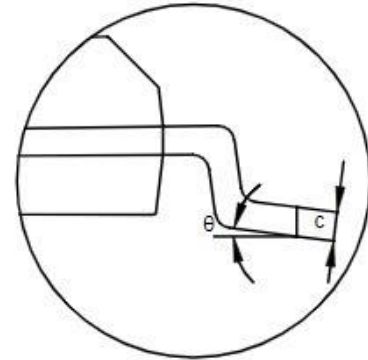
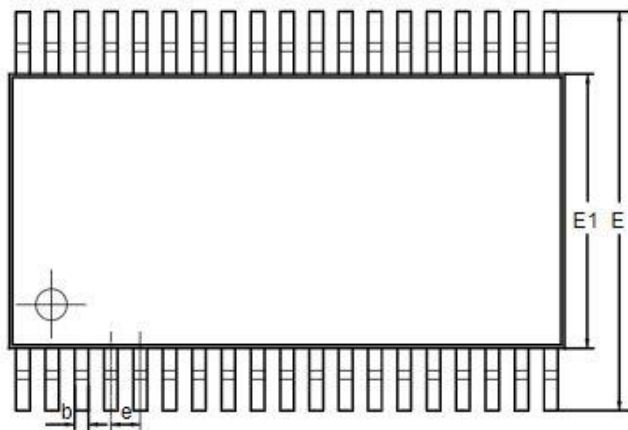
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC5120S16-TS7R-S	TSSOP38	329	16.4	6.8	10.25	1.6	8	16	Q1
TPC5120S16-QFBR	QFN5X5-32	330	16	5.2	5.2	1.1	8	12	Q1
TPC5121S08-QF8R	QFN4X4-24	330	16	4.35	4.35	1.1	8	12	Q1

## Package Information

### TSSOP38

#### Package Outline Dimensions

#### TS7(TSSOP-38-A)

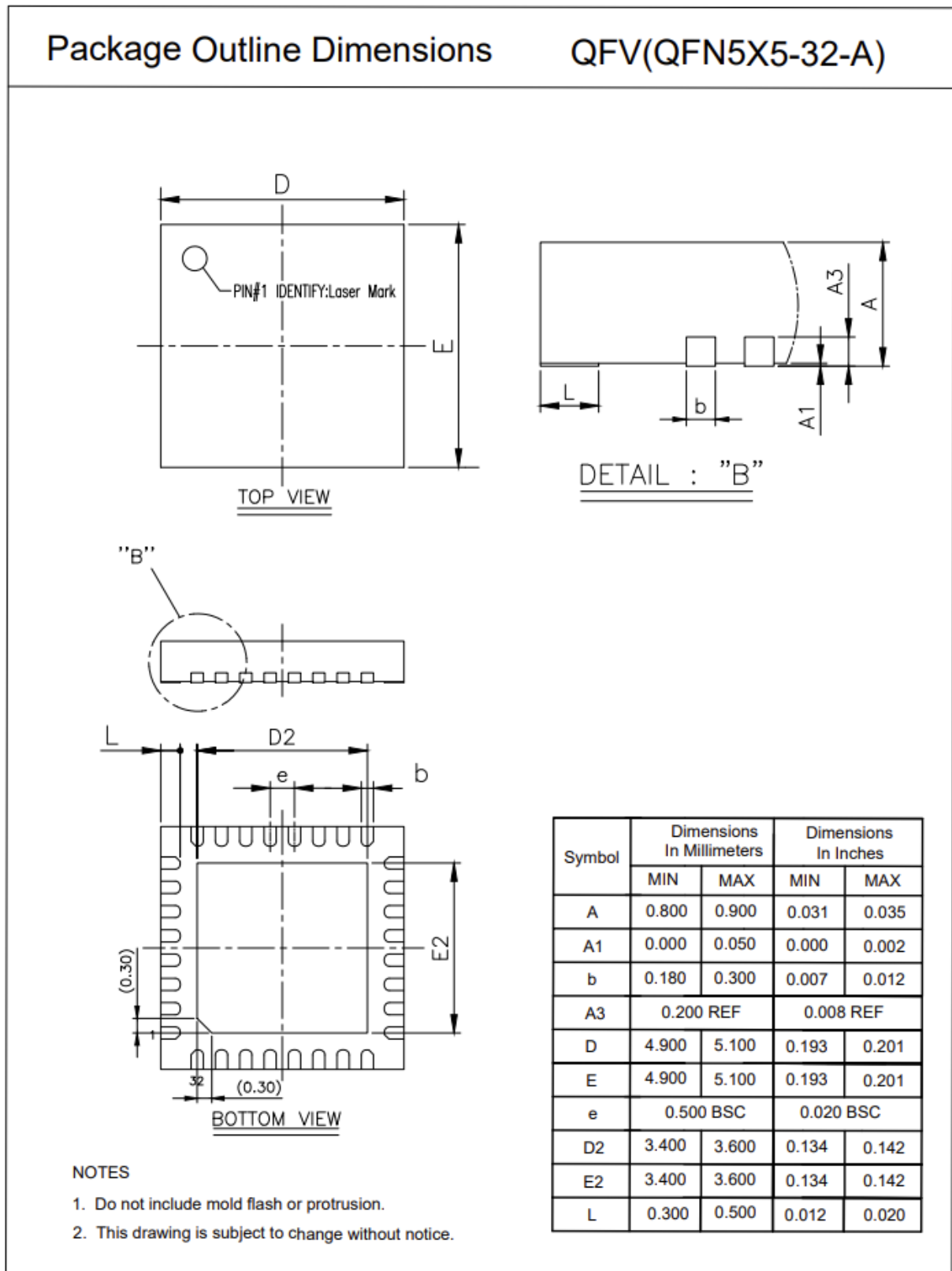


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.500 BSC		0.020 BSC	
L	0.450	0.750	0.018	0.030
$\theta$	0	$8^\circ$	0	$8^\circ$

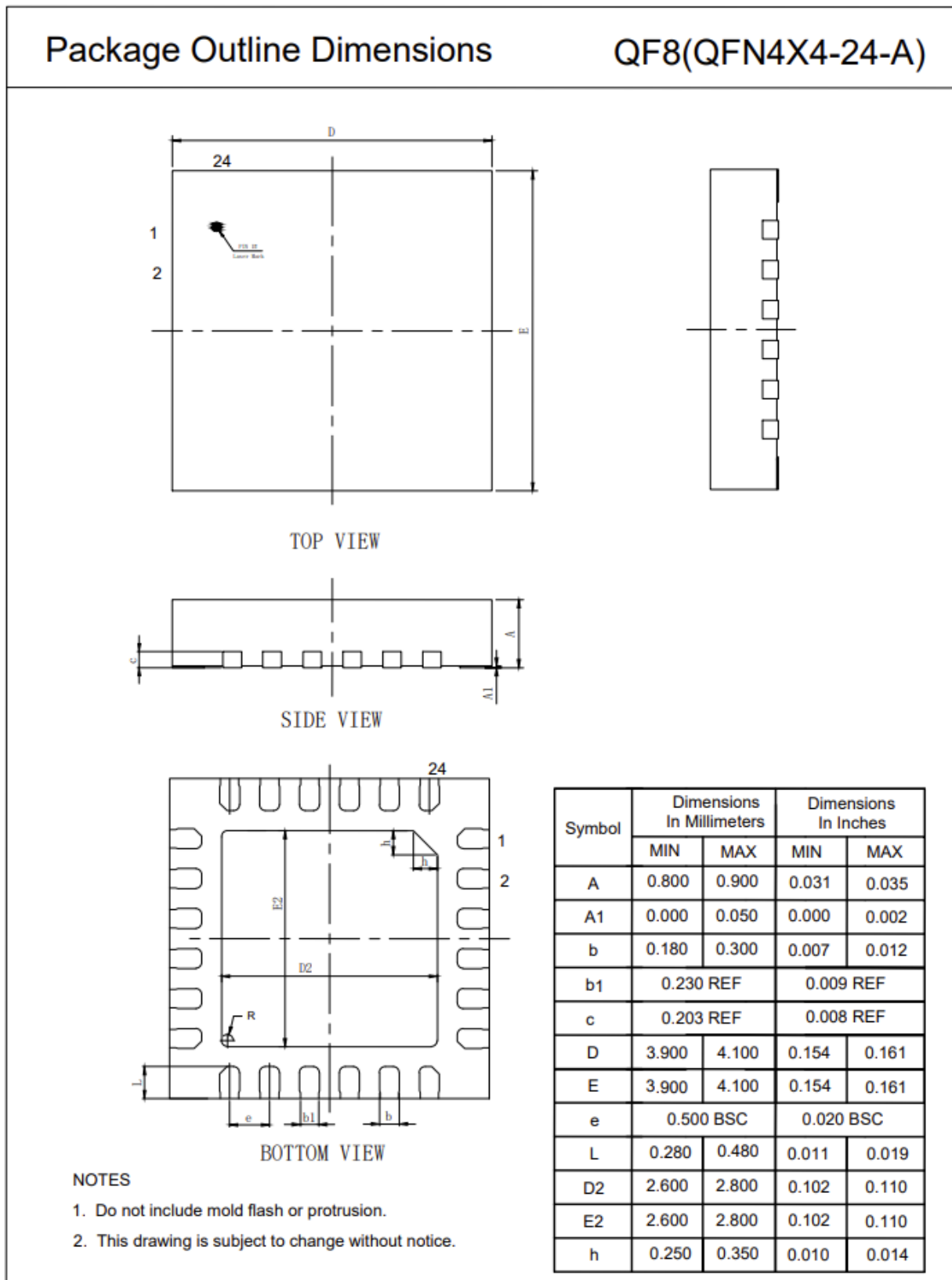
#### NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

QFN5X5-32



QFN4X4-24



## Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC5120S16-TS7R-S	-40 to 125°C	TSSOP38	5120	MSL3	Tape reel, 3000	Green
TPC5120S16-QFBR	-40 to 125°C	QFN5X5-32	5120	MSL3	Tape reel, 3000	Green
TPC5121S08-QF8R	-40 to 125°C	QFN4X4-24	5121	MSL3	Tape reel, 3000	Green

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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