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# ASM330LHHXG1

Datasheet

## High-accuracy 6-axis automotive inertial measurement unit (IMU) with embedded machine learning core and dual operating modes


**LGA-14L**
**Typ: 2.5 x 3.0 x 0.83 mm³**

| Product status link |
|---|
| ASM330LHHXG1 |

| Product summary | |
|---|---|
| **Order code** | ASM330LHHXG1TR |
| **Temp. range [°C]** | -40 to +125 |
| **Package** | LGA-14L (2.5 x 3.0 x 0.83 mm³) |
| **Packing** | Tape and reel |

| Product resources |
|---|
| AN5985 (device application note) |
| AN5986 (finite state machine) |
| AN5987 (machine learning core) |
| TN0018 (design and soldering) |

| Product labels |
|---|
| SUSTAINABLE TECHNOLOGY, LONGEVITY 15 YEARS COMMITMENT |

## Features

- AEC-Q100 qualified
- Android Auto™ compliant and CarPlay® compliant
- Extended temperature range from -40 to +125°C
- Embedded compensation for high stability over temperature
- Accelerometer user-selectable full scale up to ±16 *g*
- Extended gyroscope range from ±125 to ±4000 dps
- Dual operating modes: high-performance and low-power mode
- I²C, MIPI I3C℠, and SPI serial interfaces
- Six-channel synchronized output to enhance the accuracy of dead-reckoning algorithms
- Programmable finite state machine
- Machine learning core
- Smart programmable interrupts
- Embedded 3 KB FIFO available to underload host processor
- ECOPACK and RoHS compliant

## Applications

- Dead reckoning (DR)
- Vehicle-to-everything (V2X)
- Telematics, e-tolling
- Antitheft systems
- Impact detection and crash reconstruction
- Motion-activated functions
- Driving comfort
- Vibration monitoring and compensation

## Description

The ASM330LHHXG1 is a 6-axis IMU featuring a 3-axis digital accelerometer and a 3-axis digital gyroscope with an extended temperature range up to +125°C, designed to address automotive nonsafety applications.

ST's family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes to serve both the automotive and consumer markets. The ASM330LHHXG1 is AEC-Q100 compliant and industrialized through a dedicated MEMS production flow to meet automotive reliability standards. All the parts are fully tested with respect to temperature to ensure the highest quality level.

The sensing elements are manufactured using ST's proprietary micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The ASM330LHHXG1 has a full-scale acceleration range of ±2/±4/±8/±16 g and a wide angular rate range of ±125/±250/±500/±1000/±2000/±4000 dps that enables its usage in a broad range of automotive applications.

The device supports dual operating modes: high-performance mode and low-power mode.

All the design aspects of the ASM330LHHXG1 have been optimized to reach superior output stability, extremely low noise, and full data synchronization to the benefit of sensor-assisted applications like dead reckoning and sensor fusion.

The ASM330LHHXG1 is available in an overmolded 14-lead plastic, land grid array (LGA) package.

# 1 Overview

The ASM330LHHXG1 is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

This device is suitable for telematics and dead-reckoning applications as well as vehicle-to-vehicle (V2X) and impact detection as a result of its high stability over temperature and time, combined with superior sensing precision.

Supporting dual operating modes, the device has enhanced flexibility versus application requirements, leveraging on multiple voltage and multiple ODR selections. The device also includes digital features like a finite state machine and an ST proprietary machine learning core, allowing defined motion pattern detection or some complex algorithms run in the application processor to be moved to the MEMS sensor with the advantage of consistent reduction in power consumption.

The event-detection interrupts enable efficient and reliable motion-activated functions, implementing hardware recognition of free-fall events, 6D orientation, activity or inactivity, and wake-up events.

Like the entire portfolio of MEMS sensor modules, the ASM330LHHXG1 leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The ASM330LHHXG1 is available in a small plastic, land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultracompact solutions.

# 2 Embedded low-power features

The ASM330LHHXG1 has been designed to feature the following on-chip functions:

- 3 KB data buffering
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable)
  - Free-fall
  - Wake-up
  - 6D orientation
  - Activity/inactivity recognition
  - Stationary/motion detection
- Specific IP blocks with negligible power consumption and high performance
  - Finite state machine (FSM) for accelerometer, gyroscope, and external sensors
  - Machine learning core (MLC) for accelerometer, gyroscope, and external sensors
- Sensor hub
  - Up to six total sensors: two internal (accelerometer and gyroscope) and four external sensors

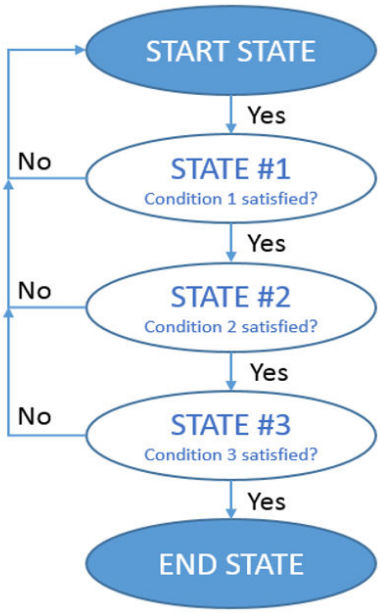
## 2.1 Finite state machine

The ASM330LHHXG1 can be configured to generate interrupt signals activated by user-defined motion patterns. To do this, up to 16 embedded finite state machines can be programmed independently for motion detection such as vehicle status (stationary or moving), antitheft alarms, and shock detection.

### Definition of finite state machine

A state machine is a mathematical abstraction used to design logic connections. It is a behavioral model composed of a finite number of states and transitions between states, similar to a flow chart in which one can inspect the way logic runs when certain conditions are met. The state machine begins with a start state, goes to different states through transitions dependent on the inputs, and can finally end in a specific state (called stop state). The current state is determined by the past states of the system. The figure below shows a generic state machine.

**Figure 1. Generic state machine**



### Finite state machine in the ASM330LHHXG1

The ASM330LHHXG1 works as a combo accelerometer-gyroscope sensor, generating acceleration and angular rate output data. It is also possible to connect an external sensor (magnetometer) by using the sensor hub feature (mode 2). These data can be used as input of up to 16 programs in the embedded finite state machine (Figure 2. State machine in the ASM330LHHXG1).

All 16 finite state machines are independent: each one has its dedicated memory area and it is independently executed. An interrupt is generated when the end state is reached or when some specific command is performed.

**Figure 2. State machine in the ASM330LHHXG1**

## 2.2 Machine learning core

The ASM330LHHXG1 embeds a dedicated core for machine learning processing that provides system flexibility, allowing some algorithms run in the application processor to be moved to the MEMS sensor with the advantage of consistent reduction in power consumption.

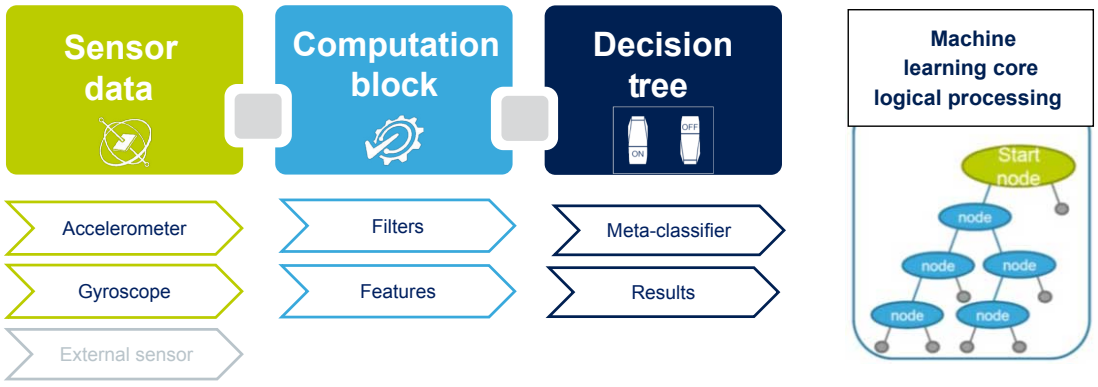
Machine learning core logic allows identifying if a data pattern (for example motion, pressure, temperature, magnetic data, and so forth) matches a user-defined set of classes. Typical examples of applications could be activity detection like running, walking, driving, and so forth.

The ASM330LHHXG1 machine learning core works on data patterns coming from the accelerometer and gyroscope sensors, but it is also possible to connect and process external sensor data (like magnetometer) by using the sensor hub feature (mode 2).

The input data can be filtered using a dedicated configurable computation block containing filters and features computed in a fixed time window defined by the user.

Machine learning processing is based on logical processing composed of a series of configurable nodes characterized by "if-then-else" conditions where the "feature" values are evaluated against defined thresholds.

**Figure 3. Machine learning core in the ASM330LHHXG1**



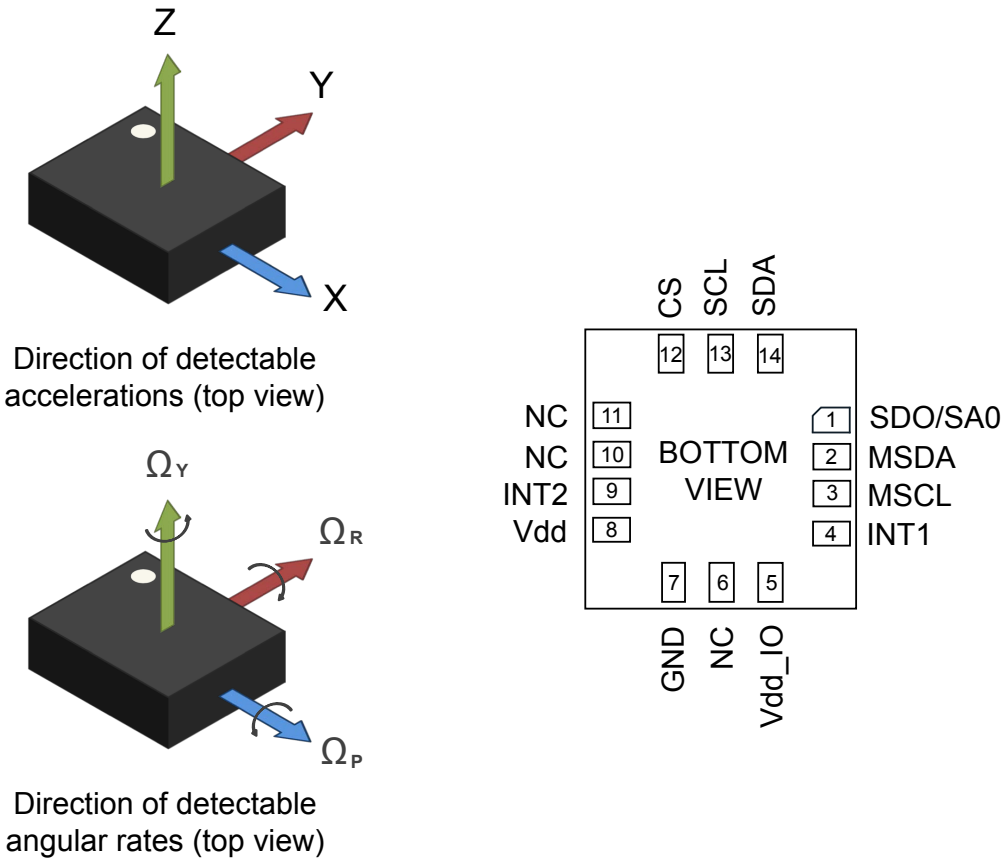

The ASM330LHHXG1 can be configured to run up to 8 flows simultaneously and independently and every flow can generate up to 256 results. The total number of nodes can be up to 512.

The results of the machine learning processing are available in dedicated output registers readable from the application processor at any time.

The ASM330LHHXG1 machine learning core can be configured to generate an interrupt when a change in the result occurs.

# 3 Pin description

**Figure 4. Pin connections**

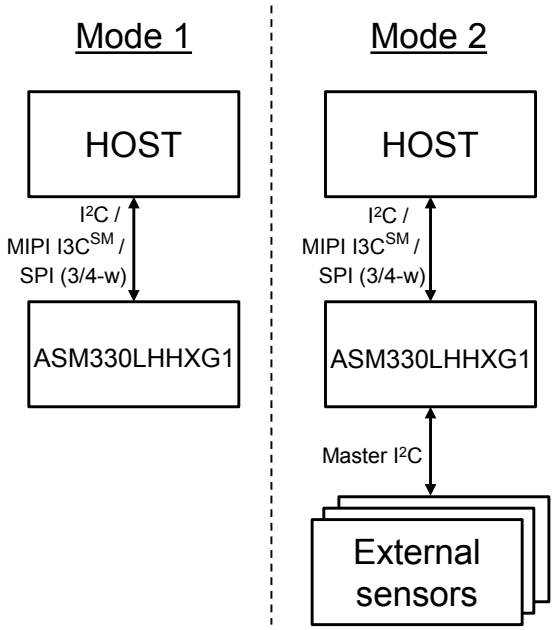


## 3.1 Pin connections

The ASM330LHHXG1 offers flexibility to connect the pins in order to have two different mode connections and functionalities. In detail:

- **Mode 1:** I²C / MIPI I3C$^{SM}$ slave interface or SPI (3- and 4-wire) serial interface is available
- **Mode 2:** I²C / MIPI I3C$^{SM}$ slave interface or SPI (3- and 4-wire) serial interface and I²C master interface for external sensor connections are available

**Figure 5. ASM330LHHXG1 connection modes**



In the following table, each mode is described for the pin connections and function.

**Table 1. Pin description**

| Pin# | Name | Mode 1 function | Mode 2 function |
|---|---|---|---|
| 1 | SDO/SA0 | SPI 4-wire interface serial data output (SDO)<br>I²C least significant bit of the device address (SA0)<br>MIPI I3C℠ least significant bit of the static address (SA0) | SPI 4-wire interface serial data output (SDO)<br>I²C least significant bit of the device address (SA0)<br>MIPI I3C℠ least significant bit of the static address (SA0) |
| 2 | MSDA | Connect to Vdd_IO or GND | I²C master serial data (MSDA) |
| 3 | MSCL | Connect to Vdd_IO or GND | I²C master serial clock (MSCL) |
| 4 | INT1 | Programmable interrupt in I²C and SPI | |
| 5 | Vdd_IO(1) | Power supply for I/O pins | |
| 6 | NC | Connect to Vdd_IO or GND or leave unconnected | |
| 7 | GND | 0 V supply | |
| 8 | Vdd(1) | Power supply | |
| 9 | INT2 | Programmable interrupt 2 (INT2) / Data enabled (DEN) | Programmable interrupt 2 (INT2) / Data enabled (DEN) /<br>I²C master external synchronization signal (MDRDY) |
| 10 | NC | Leave unconnected(2) | Leave unconnected(2) |
| 11 | NC | Leave unconnected(2) | Leave unconnected(2) |
| 12 | CS | I²C/MIPI I3C℠/SPI mode selection<br>(1: SPI idle mode / I²C/MIPI I3C℠ communication enabled;<br>0: SPI communication mode / I²C/MIPI I3C℠ disabled) | I²C/MIPI I3C℠/SPI mode selection<br>(1: SPI idle mode / I²C/MIPI I3C℠ communication enabled;<br>0: SPI communication mode / I²C/MIPI I3C℠ disabled) |
| 13 | SCL | I²C/MIPI I3C℠ serial clock (SCL)<br>SPI serial port clock (SPC) | I²C/MIPI I3C℠ serial clock (SCL)<br>SPI serial port clock (SPC) |
| 14 | SDA | I²C/MIPI I3C℠ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) | I²C/MIPI I3C℠ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |

1. *Vdd_IO: Recommended 100 nF filter capacitor. Vdd: Recommended 100 nF plus 10 µF capacitors.*
2. *Leave pin electrically unconnected and soldered to PCB.*

# 4 Module specifications

## 4.1 Mechanical characteristics

@Vdd = 3.0 V, T = -40°C to +125°C, up to gyroscope FS = ±2000 dps unless otherwise noted.
The product is factory calibrated at 3.0 V. The operational power supply range is from 1.71 V to 3.6 V.

**Table 2. Mechanical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| LA_FS | Linear acceleration measurement range | | | ±2 | | *g* |
| | | | | ±4 | | |
| | | | | ±8 | | |
| | | | | ±16 | | |
| G_FS | Angular rate measurement range | | | ±125 | | dps |
| | | | | ±250 | | |
| | | | | ±500 | | |
| | | | | ±1000 | | |
| | | | | ±2000 | | |
| | | | | ±4000 | | |
| LA_So | Linear acceleration sensitivity | @LA_FS = ±2 *g* | | 0.061 | | mg/LSB |
| | | @LA_FS = ±4 *g* | | 0.122 | | |
| | | @LA_FS = ±8 *g* | | 0.244 | | |
| | | @LA_FS = ±16 *g* | | 0.488 | | |
| G_So | Angular rate sensitivity | @G_FS = ±125 dps | | 4.37 | | mdps/LSB |
| | | @G_FS = ±250 dps | | 8.75 | | |
| | | @G_FS = ±500 dps | | 17.5 | | |
| | | @G_FS = ±1000 dps | | 35.0 | | |
| | | @G_FS = ±2000 dps | | 70.0 | | |
| | | @G_FS = ±4000 dps | | 140.0 | | |
| LA_TySo% | Linear acceleration sensitivity tolerance(2) | @25°C | | ±2 | | % |
| G_TySo% | Angular rate sensitivity tolerance(2) | @25°C | | ±2 | | % |
| LA_So% | Linear acceleration sensitivity tolerance - long term(3) | | -6 | | +6 | % |
| G_So% | Angular rate sensitivity tolerance - long term(3) | | -10 | | +10 | % |
| LA_SoDr | Linear acceleration sensitivity change vs. temperature | | | ±100 | | ppm/°C |
| G_SoDr | Angular rate sensitivity change vs. temperature | | | ±70 | | ppm/°C |
| LA_TyOff | Linear acceleration zero-*g* level offset accuracy(2) | @25°C | | ±20 | | mg |
| LA_Off | Linear acceleration offset accuracy - long term(3) | | -210 | | +210 | mg |
| G_TyOff | Angular rate zero-rate level accuracy(2) | @25°C | | ±2 | | dps |
| G_Off | Angular rate offset accuracy - long term(3) | | -10 | | +10 | dps |
| LA_TCOff | Linear acceleration zero-*g* level change vs. temperature | | | ±0.10 | | mg/°C |
| G_TCOff | Angular rate typical zero-rate level change vs. temperature | | | ±0.005 | | dps/°C |
| LA_Cx | Linear acceleration cross-axis sensitivity | @25°C | | ±1 | | % |

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| G_Cx | Angular rate cross-axis sensitivity | @25°C | | ±1 | | % |
| An | Acceleration noise density(4)(6) | @LA_FS = ±2 *g*<br>@25°C | | 60 | 200 | µg/√Hz |
| AnRMS | Acceleration RMS noise in low-power mode(5) | | | 1.8 | | mg(RMS) |
| Rn | Rate noise density(4)(6) | @25°C | | 5 | 12 | mdps/√Hz |
| RnRMS | Gyroscope RMS noise in low-power mode(5) | | | 90 | | mdps(RMS) |
| XL_NL | Accelerometer nonlinearity(7) | Best-fit straight line | | 0.5 | | %FS |
| G_NL | Gyroscope nonlinearity(7) | Best-fit straight line | | 0.01 | | % FS |
| VRW | Velocity random walk(7) | @25°C | | 0.03 | | m/sec/√h |
| XL_BI | Accelerometer bias instability(7) | @25°C | | 40 | | µ*g* |
| ARW | Angular random walk(7) | @25°C | | 0.21 | | °/√h |
| G_BI | Gyroscope bias instability(7) | @25°C | | 3 | | °/h |
| LA_ODR | Linear acceleration output data rate | | | 1.6(8)<br>12.5<br>26<br>52<br>104<br>208<br>416<br>833<br>1667<br>3333<br>6667 | | Hz |
| G_ODR | Angular rate output data rate | | | 12.5<br>26<br>52<br>104<br>208<br>416<br>833<br>1667<br>3333<br>6667 | | Hz |
| Vst | Linear acceleration self-test output change(9)(10)(11) | | 40 | | 1700 | mg |
| | Angular rate self-test output change(12)(13) | FS = ±250 dps | 20 | | 80 | dps |
| | | FS = ±2000 dps | 150 | | 700 | dps |
| Top | Operating temperature range | | -40 | | +125 | °C |

1. *Typical specifications are not guaranteed.*
2. *Values after factory calibration test and trimming at T = 25°C.*
3. *Long term includes the following conditions: post solder, drift in temperature in the range [-40°C to +125°C] and over life.*
4. *Max. values from design and characterization at ambient temperature (T = 25°C).*
5. *RMS noise is the same for all ODRs.*
6. *Noise density is the same for all ODRs.*
7. *Based on characterization data on a limited number of samples. Not measured during final test for production.*

8. *This ODR is available when the accelerometer is in low-power mode.*
9. *Accelerometer self-test limits are full-scale independent.*
10. *The sign of the linear acceleration self-test output change is defined by the STx_XL bits in a dedicated register for all axes.*
11. *The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 0.061 mg at ±2 g full scale.*
12. *The angular rate self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 70 mdps at ±2000 dps full scale.*
13. *The sign of the angular rate self-test output change is defined by the STx_G bits in a dedicated register for all axes.*

## 4.2 Electrical characteristics

@Vdd = 3.0 V, T = -40°C to +125°C, up to gyroscope FS = ±2000 dps unless otherwise noted.

**Table 3. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | | 1.71 | | 3.6 | V |
| Vdd_IO | Power supply for I/O | | 1.62 | | 3.6 | V |
| GA_Idd | Gyroscope and accelerometer current consumption | ODR = 1.6 kHz | | 1.3 | 1.7 | mA |
| LA_IddHP | Accelerometer current consumption in high-performance mode | ODR = 1.6 kHz | | 360 | 750 | µA |
| LA_IddLM | Accelerometer current consumption in low-power mode | ODR = 52 Hz @25°C | | 50 | 500 | µA |
| | | ODR = 12.5 Hz @25°C(3) | | 14 | | µA |
| | | ODR = 1.6 Hz @25°C(3) | | 7 | | µA |
| | | Vdd = 1.71 V, ODR = 52 Hz @25°C | | 40 | 500 | µA |
| | | Vdd = 1.71 V, ODR = 12.5 Hz @25°C(3) | | 11 | | µA |
| | | Vdd = 1.71 V, ODR = 1.6 Hz @25°C(3) | | 5.5 | | µA |
| LC_IddLM | Current consumption in low-power mode, combo | ODR = 52 Hz | | 530 | 1000 | µA |
| | | ODR = 12.5 Hz @25°C(3) | | 475 | | µA |
| | | Vdd = 1.71 V, ODR = 52 Hz | | 520 | 1000 | µA |
| | | Vdd = 1.71 V, ODR = 12.5 Hz @25°C(3) | | 470 | | µA |
| IddPD | Gyroscope and accelerometer current consumption during power-down | @25°C | | 5 | 13 | µA |
| Ton | Turn-on time(2) | | | 35 | | ms |
| $V_{IH}$(3) | Digital high-level input voltage | | 0.7 * Vdd_IO | | | V |
| $V_{IL}$(3) | Digital low-level input voltage | | | | 0.3 * Vdd_IO | V |
| $V_{OH}$(3) | High-level output voltage | $I_{OH}$ = 4 mA(4) | Vdd_IO - 0.2 | | | V |
| $V_{OL}$(3) | Low-level output voltage | $I_{OL}$ = 4 mA(4) | | | 0.2 | V |
| Top | Operating temperature range | | -40 | | +125 | °C |

1. *Typical specifications are not guaranteed.*
2. *Time to obtain stable sensitivity (within ±5% of final value) switching from power-down to normal operation*
3. *Evaluated by characterization - not tested in production*
4. *4 mA is the minimum driving capability, that is, the minimum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels $V_{OH}$ and $V_{OL}$.*

## 4.3 Temperature sensor characteristics

@Vdd = 3.0 V, T = 25°C unless otherwise noted. The product is factory calibrated at 3.0 V.

**Table 4. Temperature sensor characteristics**

| Symbol | Parameter | Test condition | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| TODR(2) | Temperature refresh rate | | | 52 | | Hz |
| Toff | Temperature offset(3) | | -15 | | +15 | °C |
| TSen | Temperature sensitivity | | | 256 | | LSB/°C |
| TST | Temperature stabilization time(4) | | | | 500 | µs |
| T_ADC_res | Temperature ADC resolution | | | 16 | | bit |
| Top | Operating temperature range | | -40 | | +125 | °C |

1. *Typical specifications are not guaranteed.*
2. *When the accelerometer is in low-power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.*
3. *The output of the temperature sensor is 0 LSB (typ.) at 25°C.*
4. *Time from power ON to valid output data. Based on characterization.*

## 4.4 Communication interface characteristics

### 4.4.1 SPI - serial peripheral interface

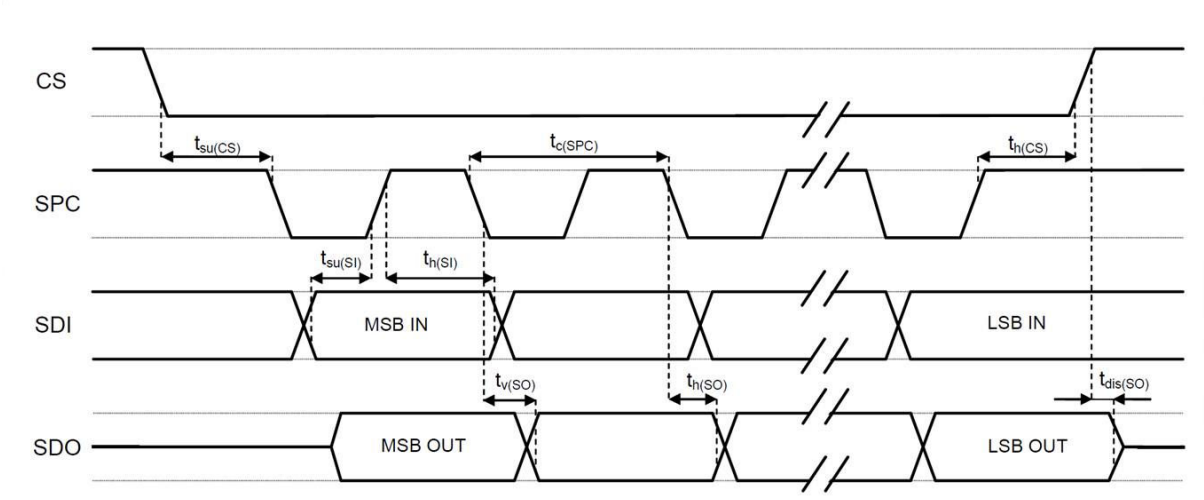
Subject to general operating conditions for Vdd and Top.

**Table 5. SPI slave timing values (in mode 3)**

| Symbol | Parameter | Value(1) | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{c(SPC)}$ | SPI clock cycle | 100 | | ns |
| $f_{c(SPC)}$ | SPI clock frequency | | 10 | MHz |
| $t_{su(CS)}$ | CS setup time | 5 | | ns |
| $t_{h(CS)}$ | CS hold time | 20 | | |
| $t_{su(SI)}$ | SDI input setup time | 5 | | |
| $t_{h(SI)}$ | SDI input hold time | 15 | | |
| $t_{v(SO)}$ | SDO valid output time | | 50 | |
| $t_{h(SO)}$ | SDO output hold time | 5 | | |
| $t_{dis(SO)}$ | SDO output disable time | | 50 | |

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*

**Figure 6. SPI slave timing diagram (in mode 3)**




*Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both input and output ports.*

### 4.4.2 I²C - inter-IC control interface

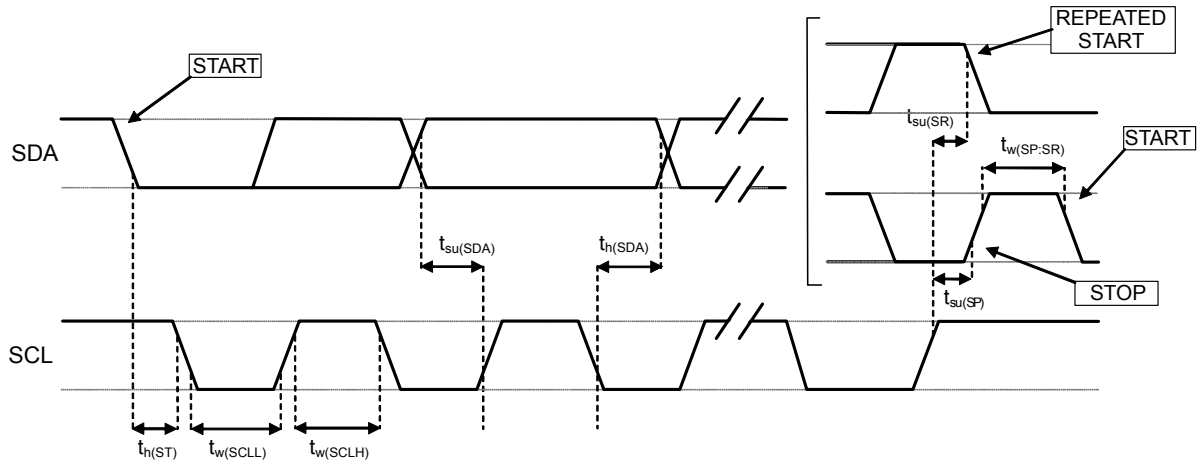
Subject to general operating conditions for Vdd and Top.

**Table 6. I²C slave timing values**

| Symbol | Parameter | I²C standard mode(1) | | I²C fast mode(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | 3.45 | 0 | 0.9 | µs |
| $t_{h(ST)}$ | START condition hold time | 4 | | 0.6 | | |
| $t_{su(SR)}$ | Repeated START condition setup time | 4.7 | | 0.6 | | |
| $t_{su(SP)}$ | STOP condition setup time | 4 | | 0.6 | | |
| $t_{w(SP:SR)}$ | Bus free time between STOP and START condition | 4.7 | | 1.3 | | |

1. *Data based on standard I²C protocol requirement, not tested in production.*

**Figure 7. I²C slave timing diagram**




*Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both ports.*

**Table 7. I²C high-speed mode specifications at 1 MHz**

| | Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Fast mode plus[1] | $f_{SCL}$ | SCL clock frequency | 0 | 1 | MHz |
| | $t_{HD;STA}$ | Hold time (repeated) START condition | 260 | - | ns |
| | $t_{LOW}$ | Low period of the SCL clock | 500 | - | |
| | $t_{HIGH}$ | High period of the SCL clock | 260 | - | |
| | $t_{SU;STA}$ | Setup time for a repeated START condition | 260 | - | |
| | $t_{HD;DAT}$ | Data hold time | 0 | - | |
| | $t_{SU;DAT}$ | Data setup time | 50 | - | |
| | $t_{rDA}$ | Rise time of SDA signal | - | 120 | |
| | $t_{fDA}$ | Fall time of SDA signal | - | 120 | |
| | $t_{rCL}$ | Rise time of SCL signal | 20*Vdd/5.5 | 120 | |
| | $t_{fCL}$ | Fall time of SCL signal | 20*Vdd/5.5 | 120 | |
| | $t_{SU;STO}$ | Setup time for STOP condition | 260 | - | |
| | $C_b$ | Capacitive load for each bus line | - | 550 | pF |
| | $t_{VD;DAT}$ | Data valid time | - | 450 | ns |
| | $t_{VD;ACK}$ | Data valid acknowledge time | - | 450 | |
| | $V_{nL}$ | Noise margin at low level | 0.1Vdd | - | V |
| | $V_{nH}$ | Noise margin at high level | 0.2Vdd | - | |
| | $t_{SP}$ | Pulse width of spikes that must be suppressed by the input filter | 0 | 50 | ns |

1. *Data based on characterization, not tested in production*

## 4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 8. Absolute maximum ratings**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |
| Sg | Acceleration *g* for 0.3 ms | 3000 | *g* |
| ESD | Electrostatic discharge protection (HBM) | 2 | kV |
| Vin | Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | -0.3 to Vdd_IO +0.3 | V |

*Note: Supply voltage on any pin should never exceed 4.8 V.*

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 4.6 Terminology

### 4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky), and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see Table 2).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see Table 2).

### 4.6.2 Zero-*g* and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0*g* on both the X-axis and Y-axis, whereas the Z-axis measures 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Linear acceleration zero-*g* level change vs. temperature” in Table 2. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see Table 2).

# 5 Digital interfaces

## 5.1 I²C/SPI interface

The registers embedded inside the ASM330LHHXG1 may be accessed through both the I²C and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped onto the same pins. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to Vdd_IO).

**Table 9. Serial interface pin description**

| Pin name | Pin description |
|---|---|
| CS | Enable SPI<br>I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled;<br>0: SPI communication mode / I²C disabled) |
| SCL/SPC | I²C serial clock (SCL)<br>SPI serial port clock (SPC) |
| SDA/SDI/SDO | I²C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| SDO/SA0 | SPI serial data output (SDO)<br>I²C less significant bit of the device address |

### 5.1.1 I²C serial interface

The ASM330LHHXG1 I²C is a bus slave. The I²C is employed to write the data to the registers, whose content can also be read back.

The relevant I²C terminology is provided in the table below.

**Table 10. I²C terminology**

| Term | Description |
|---|---|
| Transmitter | The device that sends data to the bus |
| Receiver | The device that receives data from the bus |
| Master | The device that initiates a transfer, generates clock signals, and terminates a transfer |
| Slave | The device addressed by the master |

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I²C interface is implemented with fast mode (400 kHz) I²C standards as well as with the standard mode.

In order to disable the I²C block, (I2C_disable) = 1 must be written in CTRL4_C (13h).

#### 5.1.1.1 *I²C operation*

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the ASM330LHHXG1 is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is 1 (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is 0 (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the ASM330LHHXG1 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The increment of the address is configured by CTRL3_C (12h) (IF_INC).

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 11 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 11. SAD + read/write patterns**

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W |
|---|---|---|---|---|
| Read | 110101 | 0 | 1 | 11010101 (D5h) |
| Write | 110101 | 0 | 0 | 11010100 (D4h) |
| Read | 110101 | 1 | 1 | 11010111 (D7h) |
| Write | 110101 | 1 | 0 | 11010110 (D6h) |

**Table 12. Transfer when master is writing one byte to slave**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | |

**Table 13. Transfer when master is writing multiple bytes to slave**

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | | SAK | |

**Table 14. Transfer when master is receiving (reading) one byte of data from slave**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | SR | SAD + R | | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

**Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave**

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD+W | | SUB | | SR | SAD+R | | | MAK | | MAK | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver does not acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

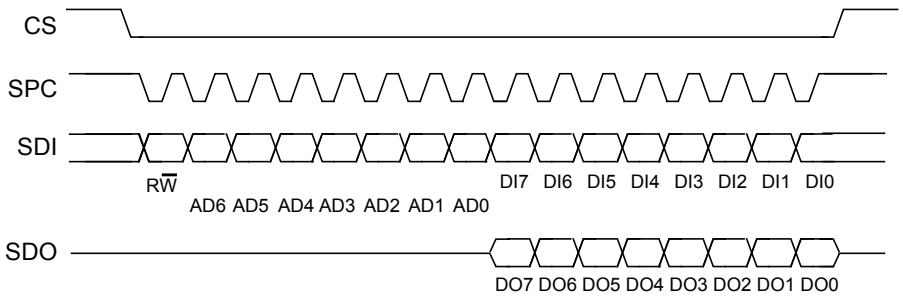
In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

### 5.1.2 SPI bus interface

The ASM330LHHXG1 SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface communicates to the application using four wires: **CS**, **SPC**, **SDI**, and **SDO**.

**Figure 8. Read and write protocol (in mode 3)**




**CS** enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0**: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip drives **SDO** at the start of bit 8.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

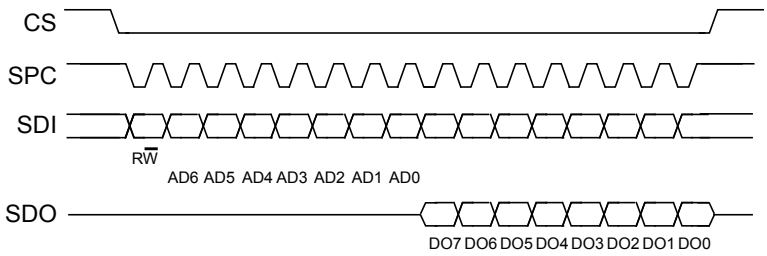
**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of eight clock periods are added. When the CTRL3_C (12h) (IF_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3_C (12h) (IF_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

#### 5.1.2.1 *SPI read*

**Figure 9. SPI read protocol (in mode 3)**




The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

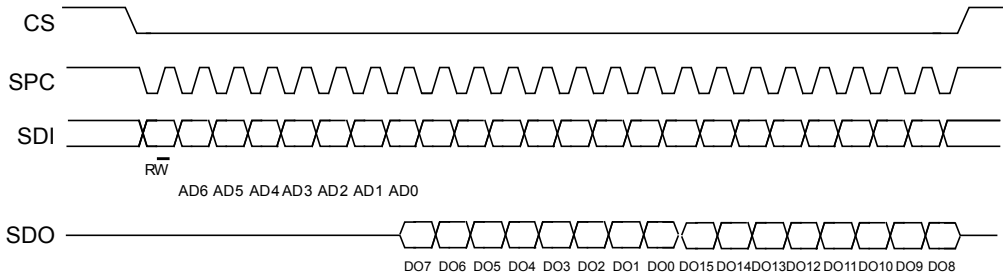
**bit 0**: READ bit. The value is 1.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

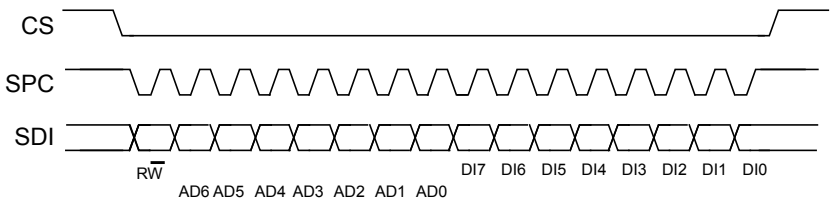
**bit 16-...**: data DO(...-8). Further data in multiple byte reads.

**Figure 10. Multiple byte SPI read protocol (2-byte example) (in mode 3)**



#### 5.1.2.2 *SPI write*

**Figure 11. SPI write protocol (in mode 3)**




The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

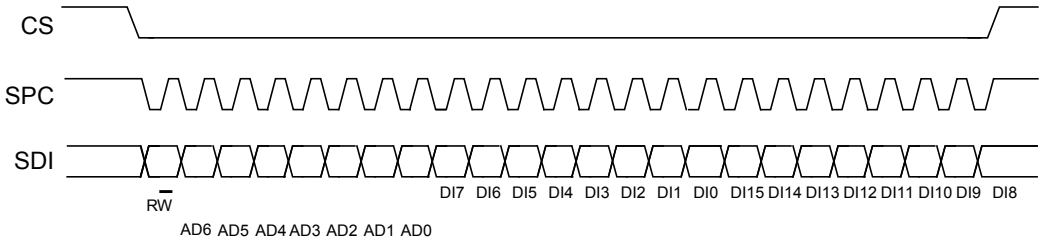
**bit 0**: WRITE bit. The value is 0.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

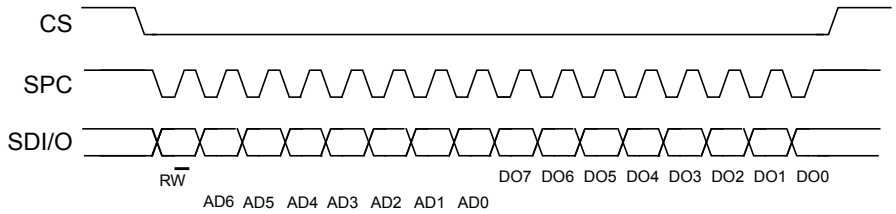
**Figure 12. Multiple byte SPI write protocol (2-byte example) (in mode 3)**



#### 5.1.2.3 *SPI read in 3-wire mode*

A 3-wire mode is entered by setting the CTRL3_C (12h) (SIM) bit equal to 1 (SPI serial interface mode selection).

**Figure 13. SPI read protocol in 3-wire mode (in mode 3)**




The SPI read command is performed with 16 clock pulses:

**bit 0**: READ bit. The value is 1.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

## 5.2 MIPI I3C℠ interface

### 5.2.1 MIPI I3C℠ slave interface

The ASM330LHHXG1 interface includes a MIPI I3C℠ SDR only slave interface with MIPI I3C℠ SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- Error detection and recovery methods

Refer to Section 5.3 I²C/I3C coexistence in ASM330LHHXG1 for details concerning the choice of the interface when powering up the device.

### 5.2.2 MIPI I3C℠ CCC supported commands

The list of MIPI I3C℠ CCC commands supported by the device is detailed in the following table.

**Table 16. MIPI I3C℠ CCC commands**

| Command | Command code | Default | Description |
|---|---|---|---|
| ENTDAA | 0x07 | | DAA procedure |
| SETDASA | 0x87 | | Assign dynamic address using static address 0x6B/0x6A depending on SDO pin |
| ENEC | 0x80 / 0x00 | | Slave activity control (direct and broadcast) |
| DISEC | 0x81/ 0x01 | | Slave activity control (direct and broadcast) |
| ENTAS0 | 0x82 / 0x02 | | Enter activity state (direct and broadcast) |
| ENTAS1 | 0x83 / 0x03 | | Enter activity state (direct and broadcast) |
| ENTAS2 | 0x84 / 0x04 | | Enter activity state (direct and broadcast) |
| ENTAS3 | 0x85 / 0x05 | | Enter activity state (direct and broadcast) |
| RSTDAA | 0x86 / 0x06 | | Reset the assigned dynamic address (direct and broadcast) |
| SETMWL | 0x89 / 0x08 | | Define maximum write length during private write (direct and broadcast) |
| SETMRL | 0x8A / 0x09 | | Define maximum read length during private read (direct and broadcast) |
| SETNEWDA | 0x88 | | Change dynamic address |
| GETMWL | 0x8B | 0x00<br>0x08<br>(2 byte) | Get maximum write length during private write |
| GETMRL | 0x8C | 0x00<br>0x10<br>0x09<br>(3 byte) | Get maximum read length during private read |
| GETPID | 0x8D | 0x02<br>0x08<br>0x00<br>0x6B<br>0x10<br>0x0B | Device ID register |
| GETBCR | 0x8E | 0x07<br>(1 byte) | Bus characteristics register |
| GETDCR | 0x8F | 0x00 | MIPI I3C℠ device characteristics register |
| GETSTATUS | 0x90 | 0x00<br>0x00<br>(2 byte) | Status register |
| GETMXDS | 0x94 | 0x00<br>0x38<br>(2 byte) | Return max data speed(1) |

1. *Bits[5:3] are set to "111" which indicates that Tsco is greater than 12 nsec. To calculate the effective bus frequency, Tsco should be used together with line capacitance, number of slaves and stubs (if present).*

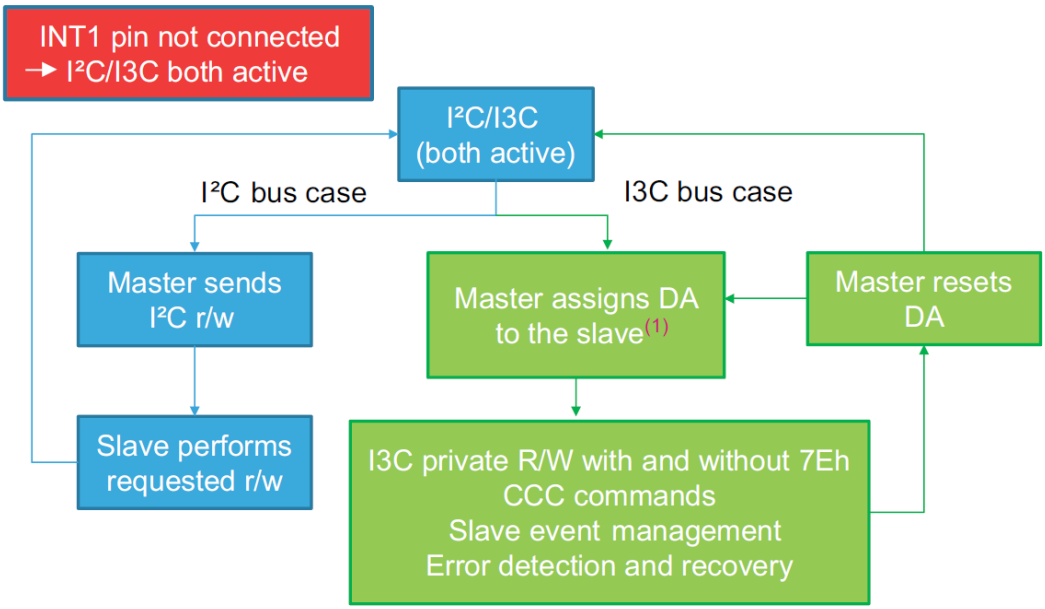
## 5.3 I²C/I3C coexistence in ASM330LHHXG1

In the ASM330LHHXG1, the SDA and SCL lines are common to both I²C and I3C. The I²C bus requires antispike filters on the SDA and SCL pins that are not compatible with I3C timing.

The device can be connected to both I²C and I3C or only to the I3C bus depending on the connection of the INT1 pin when the device is powered up:

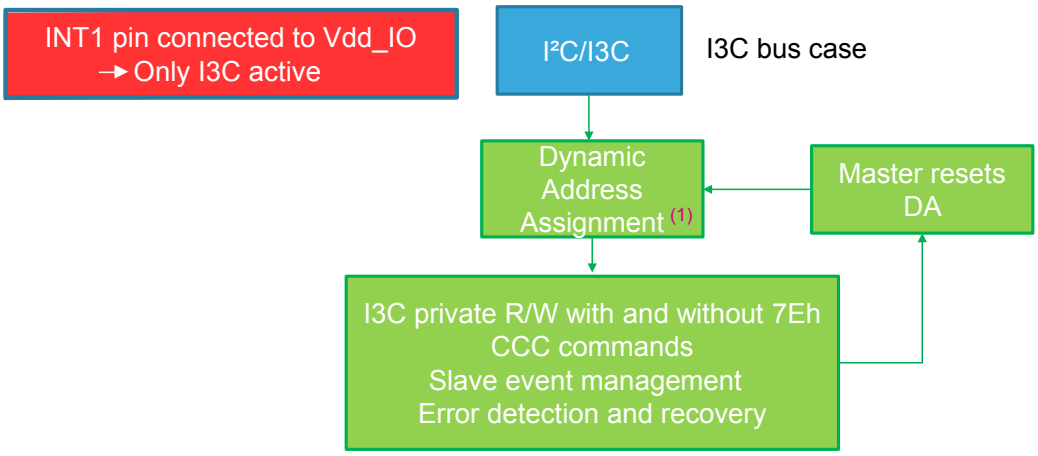
- INT1 pin floating (internal pull-down): I²C/I3C both active, see Figure 14
- INT1 pin connected to Vdd_IO: only I3C active, see Figure 15

**Figure 14. I²C and I3C both active (INT1 pin not connected)**




1. *Address assignment (DAA or ENTDA) must be performed with I²C fast mode plus timing. When the slave is addressed, the I²C slave is disabled and the timing is compatible with I3C specifications.*

**Figure 15. Only I3C active (INT1 pin connected to Vdd_IO)**




1. *When the slave is I3C only, the I²C slave is always disabled. The address can be assigned using I3C SDR timing.*

## 5.4 Master I²C interface

If the ASM330LHHXG1 is configured in mode 2, a master I²C line is available. The master serial interface is mapped to the following dedicated pins.

**Table 17. Master I²C pin details**

| Pin name | Pin description |
|---|---|
| MSCL | I²C master serial clock |
| MSDA | I²C master serial data |
| MDRDY | I²C master external synchronization signal |

# 6 Functionality

## 6.1 Operating modes

In the ASM330LHHXG1, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The ASM330LHHXG1 has three operating modes available:

- Only accelerometer active and gyroscope in power-down or sleep mode
- Only gyroscope active and accelerometer in power-down
- Both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power-down by writing ODR_XL[3:0] in CTRL1_XL (10h) while the gyroscope is activated from power-down by writing ODR_G[3:0] in CTRL2_G (11h). For combo mode the ODRs are totally independent.

*Note:* *If the accelerometer is to be activated in high-performance operating mode while the gyroscope is already running (that is, the gyroscope is not in power-down mode), proceed as follows:*

1. *Disable the accelerometer high-performance operating mode (set the XL_HM_MODE bit to 1 in the CTRL6_C (15h) register).*
2. *Write the CTRL1_XL (10h) register to 50h.*
3. *Read the OUTZ_H_A (2Dh) register to clear the XLDA bit in the STATUS_REG (1Eh) register.*
4. *Wait the duration of 1/ODR_XL or wait until the XLDA bit in the STATUS_REG (1Eh) register becomes equal to 1.*
5. *Enable the accelerometer high-performance operating mode (set the XL_HM_MODE bit to 0 in the CTRL6_C (15h) register).*
6. *Write the CTRL1_XL (10h) register to the desired value.*

## 6.2 Gyroscope power modes

In the ASM330LHHXG1, the gyroscope can be configured in two different operating modes: low-power and high-performance mode. The operating mode selected depends on the value of the G_HM_MODE bit in CTRL7_G (16h). If G_HM_MODE is set to 0, high-performance mode is valid for all ODRs (from 12.5 Hz up to 6667 Hz).

To enable low-power mode, the G_HM_MODE bit has to be set to 1. Low-power mode is available for ODRs equal to 12.5 Hz, 26 Hz, 52 Hz, 104 Hz and 208 Hz.

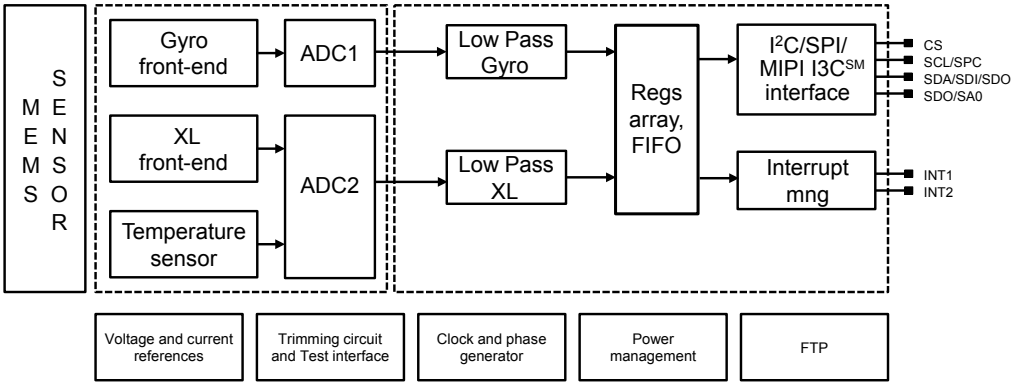
## 6.3 Accelerometer power modes

In the ASM330LHHXG1, the accelerometer can be configured in two different operating modes: low-power and high-performance mode. The operating mode selected depends on the value of the XL_HM_MODE bit in CTRL6_C (15h). If XL_HM_MODE is set to 0, high-performance mode is valid for all ODRs (from 12.5 Hz up to 6667 Hz).

To enable low-power mode, the XL_HM_MODE bit has to be set to 1. Low-power mode is available for ODRs equal to 1.6 Hz, 12.5 Hz, 26 Hz, 52 Hz, 104 Hz and 208 Hz.

## 6.4 Block diagram of filters

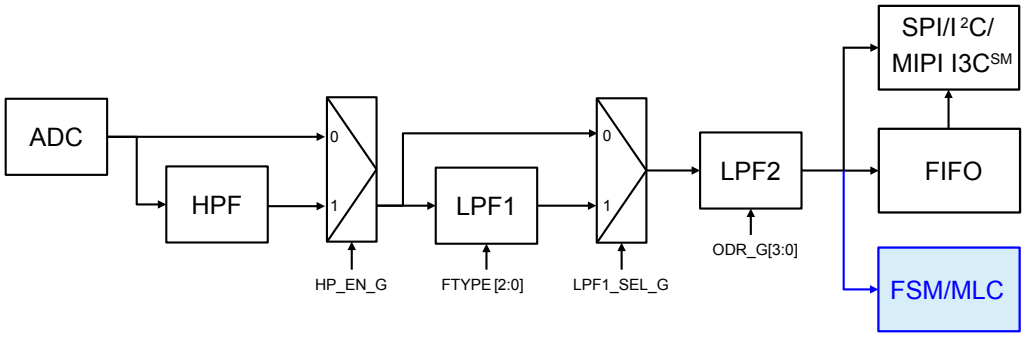
Figure 16. **Block diagram of filters**



### 6.4.1 Block diagram of the gyroscope filter

The gyroscope filtering chain appears below.

**Figure 17. Gyroscope filtering chain**




The gyroscope ODR is selectable from 12.5 Hz up to 6667 Hz. A low-pass filter (LPF1) is available, for more details about the filter characteristics see Table 59. Gyroscope LPF1 bandwidth selection. The digital LPF2 filter cannot be configured by the user and its cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

Data can be acquired from the output registers and FIFO.

**Table 18. Gyroscope LPF2 bandwidth selection**

| Gyroscope ODR [Hz] | LPF2 cutoff [Hz] |
|---|---|
| 12.5 | 4.3 |
| 26 | 8.3 |
| 52 | 16.7 |
| 104 | 33 |
| 208 | 67 |
| 417 | 133 |
| 833 | 267 |
| 1667 | 539 |
| 3333 | 1137 |
| 6667 | 3333 |

### 6.4.2 Block diagrams of the accelerometer filters

In the ASM330LHHXG1, the filtering chain for the accelerometer part is composed of the following:

- Digital filter (LPF1)
- Composite filter

Details of the block diagram appear in the following figure.

**Figure 18. Accelerometer chain**

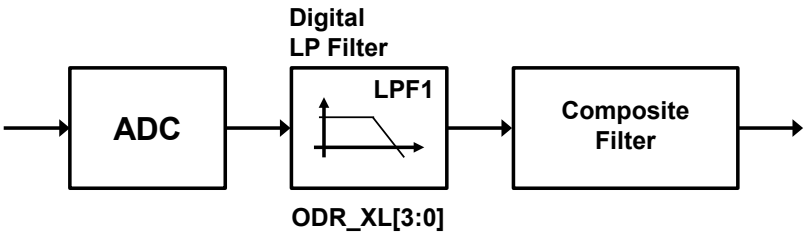
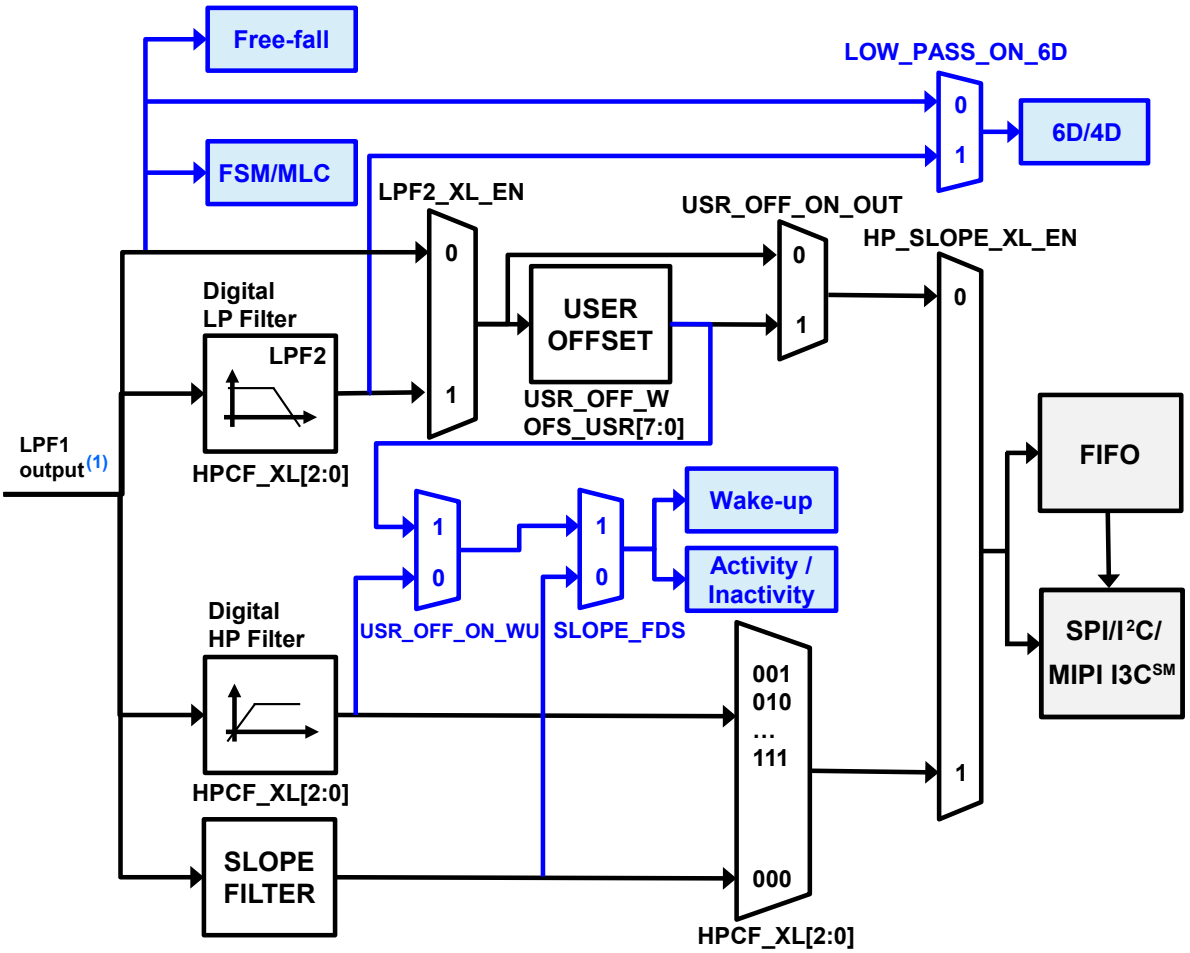



**Figure 19. Accelerometer composite filter**




1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode and ODR up to 833 Hz. This value is equal to 780 Hz when the accelerometer is in low-power mode.*

## 6.5 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The ASM330LHHXG1 embeds 3 KB of data in FIFO to store the following data:

- Gyroscope
- Accelerometer
- External sensors (up to 4)
- Timestamp
- Temperature

Writing data in the FIFO can be configured to be triggered by the:

- Accelerometer / gyroscope data-ready signal
- Sensor hub data-ready signal

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: accelerometer, gyroscope and temperature sensor batch rates can be selected by the user. Writing external sensor data in FIFO can be triggered by the accelerometer data-ready signal or by an external sensor interrupt. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO_DATA_OUT_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (batch data rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

The programmable FIFO watermark threshold can be set in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h) using the WTM[8:0] bits. To monitor the FIFO status, dedicated registers (FIFO_STATUS1 (3Ah), FIFO_STATUS2 (3Bh)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1_CTRL (0Dh) and INT2_CTRL (0Eh).

The FIFO buffer can be configured according to six different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO_MODE_[2:0] bits in the FIFO_CTRL4 (0Ah) register.

### 6.5.1 Bypass mode

In bypass mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

### 6.5.2 FIFO mode

In FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, bypass mode should be selected by writing FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0]) to 000. After this reset command, it is possible to restart FIFO mode by writing FIFO_CTRL4 (0Ah) (FIFO_MODE_[2:0]) to 001.

The FIFO buffer memorizes up to 3 KB of data but the depth of the FIFO can be resized by setting the WTM[8:0] bits in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h). If the STOP_ON_WTM bit in FIFO_CTRL2 (08h) is set to 1, FIFO depth is limited up to the WTM[8:0] bits in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h).

### 6.5.3 Continuous mode

Continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag FIFO_STATUS2 (3Bh)(FIFO_WTM_IA) is asserted when the number of unread samples in FIFO is greater than or equal to FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h) (WTM[8:0]).

It is possible to route the FIFO_WTM_IA flag to the INT1 pin by writing in register INT1_CTRL (0Dh) (INT1_FIFO_TH) = 1 or to the INT2 pin by writing in register INT2_CTRL (0Eh)(INT2_FIFO_TH) = 1.

A full-flag interrupt can be enabled, INT1_CTRL (0Dh)(INT1_FIFO_FULL) = 1 or INT2_CTRL (0Eh) (INT2_FIFO_FULL) = 1, in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the FIFO_OVR_IA flag in FIFO_STATUS2 (3Bh) is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in FIFO_STATUS1 (3Ah) and FIFO_STATUS2 (3Bh)(DIFF_FIFO_[9:0]).

### 6.5.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 1, FIFO operates in FIFO mode.

When the selected trigger bit is equal to 0, FIFO operates in continuous mode.

### 6.5.5 Bypass-to-continuous mode

In bypass-to-continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 100), data measurement storage inside FIFO operates in continuous mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

### 6.5.6 Bypass-to-FIFO mode

n bypass-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 111), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

### 6.5.7 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (FIFO_DATA_OUT_TAG (78h), in order to identify the sensor, and 6 bytes of fixed data (FIFO_DATA_OUT registers from (79h) to (7Eh)).

The DIFF_FIFO_[9:0] field in the FIFO_STATUS1 (3Ah) and FIFO_STATUS2 (3Bh) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

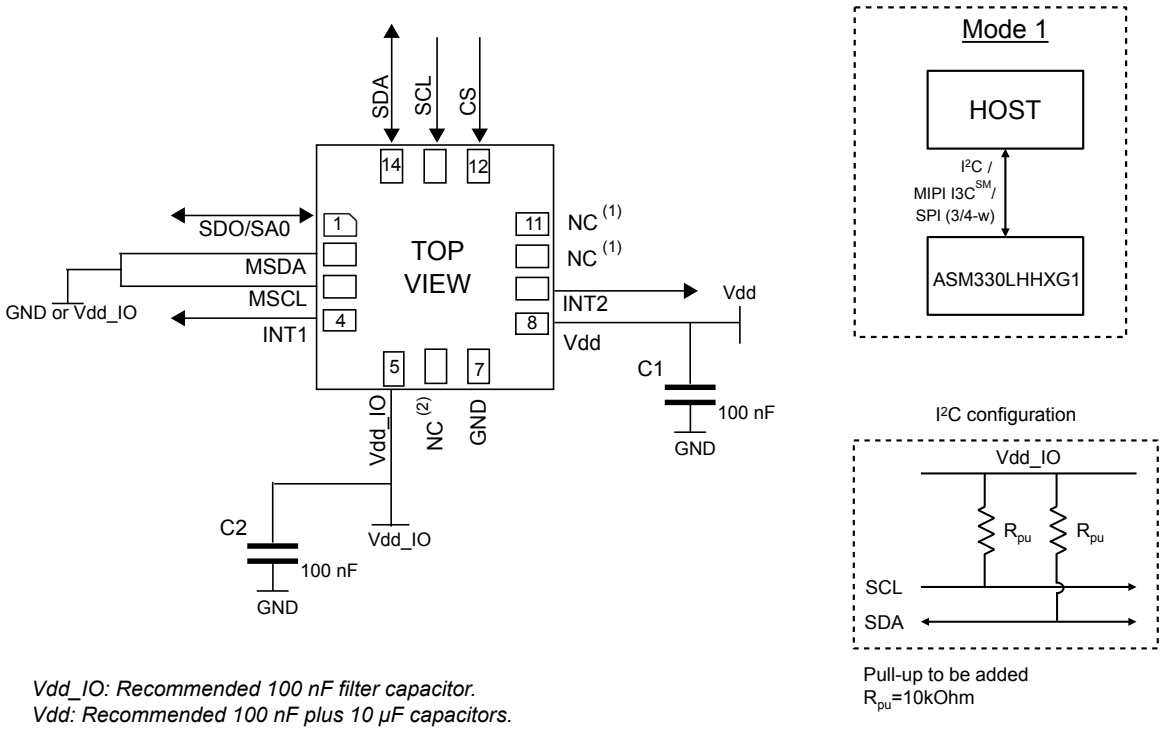
In addition, it is possible to configure a counter of the batch events of accelerometer or gyroscope sensors. The flag COUNTER_BDR_IA in FIFO_STATUS2 (3Bh) alerts that the counter reaches a selectable threshold (CNT_BDR_TH_[10:0] field in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch)). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the TRIG_COUNTER_BDR bit in COUNTER_BDR_REG1 (0Bh). As for the other FIFO status events, the flag COUNTER_BDR_IA can be routed to the INT1 or INT2 pins by asserting the corresponding bits (INT1_CNT_BDR of INT1_CTRL (0Dh) and INT2_CNT_BDR of INT2_CTRL (0Eh)).

Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the ODR_CHG_EN bit in FIFO_CTRL2 (08h).

# 7 Application hints

## 7.1 ASM330LHHXG1 electrical connections in mode 1

**Figure 20. ASM330LHHXG1 electrical connections in mode 1**




*Vdd_IO: Recommended 100 nF filter capacitor.*
*Vdd: Recommended 100 nF plus 10 µF capacitors.*

1. *Leave pin electrically unconnected and soldered to PCB.*
2. *Connect to Vdd_IO or GND or leave unconnected and soldered to PCB.*

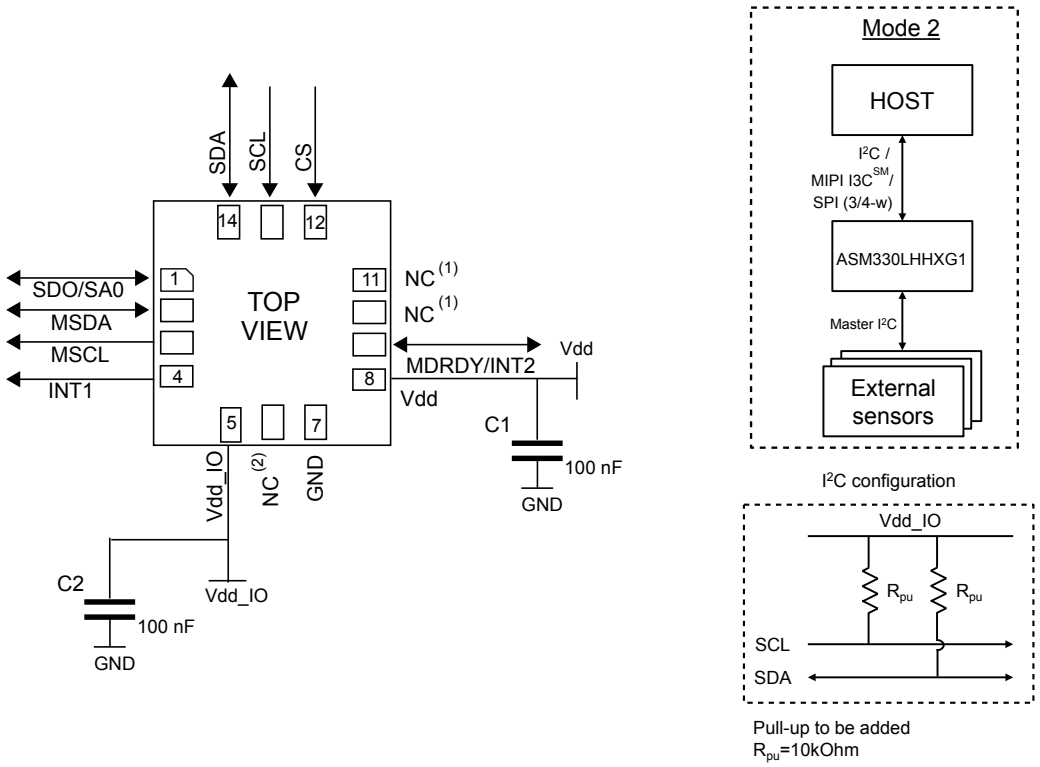
The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C℠ primary interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C℠ primary interface.

## 7.2 ASM330LHHXG1 electrical connections in mode 2

Figure 21. **ASM330LHHXG1 electrical connections in mode 2**




1. *Leave pin electrically unconnected and soldered to PCB.*
2. *Connect to Vdd_IO or GND or leave unconnected and soldered to PCB.*

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C℠ primary interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C℠ primary interface.

**Table 19. Internal pin status**

| Pin # | Name | Mode 1 function | Mode 2 function | Pin status mode 1 | Pin status mode 2 |
|---|---|---|---|---|---|
| 1 | SDO | SPI 4-wire interface serial data output (SDO) | SPI 4-wire interface serial data output (SDO) | Default: input without pull-up<br>Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h). | Default: input without pull-up<br>Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h). |
| | SA0 | I²C least significant bit of the device address (SA0)<br>MIPI I3C℠ least significant bit of the static address (SA0) | I²C least significant bit of the device address (SA0)<br>MIPI I3C℠ least significant bit of the static address (SA0) | | |
| 2 | MSDA | Connect to Vdd_IO or GND | I²C master serial data (MSDA) | Default: input without pull-up<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register MASTER_CONFIG (14h).<br>(see Note to enable pull-up) | Default: input without pull-up<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register MASTER_CONFIG (14h).<br>(see Note to enable pull-up) |
| 3 | MSCL | Connect to Vdd_IO or GND | I²C master serial clock (MSCL) | Default: input without pull-up<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register MASTER_CONFIG (14h).<br>(see Note to enable pull-up) | Default: input without pull-up<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register MASTER_CONFIG (14h).<br>(see Note to enable pull-up) |
| 4 | INT1 | Programmable interrupt 1.<br>If device is used as MIPI I3C℠ pure slave, this pin must be set to 1. | Programmable interrupt 1.<br>If device is used as MIPI I3C℠ pure slave, this pin must be set to 1. | Default: input with pull-down(1)<br>Pull-down is disabled if bit PD_DIS_INT1 = 1 in register I3C_BUS_AVB (62h). | Default: input with pull-down(1)<br>Pull-down is disabled if bit PD_DIS_INT1 = 1 in register I3C_BUS_AVB (62h). |
| 5 | Vdd_IO | Power supply for I/O pins | Power supply for I/O pins | | |
| 6 | NC | Connect to Vdd_IO or GND or leave unconnected | Connect to Vdd_IO or GND or leave unconnected | | |
| 7 | GND | 0 V supply | 0 V supply | | |
| 8 | Vdd | Power supply | Power supply | | |
| 9 | INT2 | Programmable interrupt 2 (INT2) / Data enabled (DEN) | Programmable interrupt 2 (INT2) / Data enabled (DEN)/<br>I²C master external synchronization signal (MDRDY) | Default: output forced to ground | Default: output forced to ground |
| 10 | NC | Leave unconnected | Leave unconnected | | |
| 11 | NC | Leave unconnected | Leave unconnected | | |
| 12 | CS | I²C and MIPI I3C℠/SPI mode selection<br>(1:SPI idle mode / I²C and MIPI I3C℠ communication enabled;<br>0: SPI communication mode / I²C and MIPI I3C℠ disabled) | I²C and MIPI I3C℠/SPI mode selection<br>(1:SPI idle mode / I²C and MIPI I3C℠ communication enabled;<br>0: SPI communication mode / I²C and MIPI I3C℠ disabled) | Default: input with pull-up<br>Pull-up is disabled if bit I2C_disable = 1 in register CTRL4_C (13h) and I3C_disable = 1 in register CTRL9_XL (18h). | Default: input with pull-up<br>Pull-up is disabled if bit I2C_disable = 1 in register CTRL4_C (13h) and I3C_disable = 1 in register CTRL9_XL (18h). |
| 13 | SCL | I²C/MIPI I3C℠ serial clock (SCL) / SPI serial port clock (SPC) | I²C/MIPI I3C℠ serial clock (SCL) / SPI serial port clock (SPC) | Default: input without pull-up | Default: input without pull-up |
| 14 | SDA | I²C/MIPI I3C℠ serial data (SDA) /<br>SPI serial data input (SDI) /<br>3-wire interface serial data output (SDO) | I²C/MIPI I3C℠ serial data (SDA) /<br>SPI serial data input (SDI) /<br>3-wire interface serial data output (SDO) | Default: input without pull-up | Default: input without pull-up |

1. *INT1 must be set to 0 or left unconnected during power-on if the I²C/SPI interfaces are used.*

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on Vdd_IO.

*Note: The procedure to enable the pull-up on pins 2 and 3 is as follows:*

*1. From the primary I²C/I3C/SPI interface: write 40h in register at address 01h (enable access to the sensor hub registers)*

*2. From the primary I²C/I3C/SPI interface: write 08h in register at address 14h (enable the pull-up on pins 2 and 3)*

*3. From the primary I²C/I3C/SPI interface: write 00h in register at address 01h (disable access to the sensor hub registers)*

# 8 Register map

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

**Table 20. Registers address map**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| FUNC_CFG_ACCESS | R/W | 01 | 00000001 | 00000000 | |
| PIN_CTRL | R/W | 02 | 00000010 | 00111111 | |
| RESERVED | - | 03-06 | | | Reserved |
| FIFO_CTRL1 | R/W | 07 | 00000111 | 00000000 | |
| FIFO_CTRL2 | R/W | 08 | 00001000 | 00000000 | |
| FIFO_CTRL3 | R/W | 09 | 00001001 | 00000000 | |
| FIFO_CTRL4 | R/W | 0A | 00001010 | 00000000 | |
| COUNTER_BDR_REG1 | R/W | 0B | 00001011 | 00000000 | |
| COUNTER_BDR_REG2 | R/W | 0C | 00001100 | 00000000 | |
| INT1_CTRL | R/W | 0D | 00001101 | 00000000 | |
| INT2_CTRL | R/W | 0E | 00001110 | 00000000 | |
| WHO_AM_I | R | 0F | 00001111 | 01101011 | |
| CTRL1_XL | R/W | 10 | 00010000 | 00000000 | |
| CTRL2_G | R/W | 11 | 00010001 | 00000000 | |
| CTRL3_C | R/W | 12 | 00010010 | 00000100 | |
| CTRL4_C | R/W | 13 | 00010011 | 00000000 | |
| CTRL5_C | R/W | 14 | 00010100 | 00000000 | |
| CTRL6_C | R/W | 15 | 00010101 | 00000000 | |
| CTRL7_G | R/W | 16 | 00010110 | 00000000 | |
| CTRL8_XL | R/W | 17 | 00010111 | 00000000 | |
| CTRL9_XL | R/W | 18 | 00011000 | 11100000 | |
| CTRL10_C | R/W | 19 | 00011001 | 00000000 | |
| ALL_INT_SRC | R | 1A | 00011010 | output | |
| WAKE_UP_SRC | R | 1B | 00011011 | output | |
| RESERVED | - | 1C | | | Reserved |
| D6D_SRC | R | 1D | 00011101 | output | |
| STATUS_REG | R | 1E | 00011110 | output | |
| RESERVED | - | 1F | | | Reserved |
| OUT_TEMP_L | R | 20 | 00100000 | output | |
| OUT_TEMP_H | R | 21 | 00100001 | output | |
| OUTX_L_G | R | 22 | 00100010 | output | |
| OUTX_H_G | R | 23 | 00100011 | output | |
| OUTY_L_G | R | 24 | 00100100 | output | |
| OUTY_H_G | R | 25 | 00100101 | output | |
| OUTZ_L_G | R | 26 | 00100110 | output | |

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| OUTZ_H_G | R | 27 | 00100111 | output | |
| OUTX_L_A | R | 28 | 00101000 | output | |
| OUTX_H_A | R | 29 | 00101001 | output | |
| OUTY_L_A | R | 2A | 00101010 | output | |
| OUTY_H_A | R | 2B | 00101011 | output | |
| OUTZ_L_A | R | 2C | 00101100 | output | |
| OUTZ_H_A | R | 2D | 00101101 | output | |
| RESERVED | - | 2E-34 | | | Reserved |
| EMB_FUNC_STATUS_MAINPAGE | R | 35 | 00110101 | output | |
| FSM_STATUS_A_MAINPAGE | R | 36 | 00110110 | output | |
| FSM_STATUS_B_MAINPAGE | R | 37 | 00110111 | output | |
| MLC_STATUS_MAINPAGE | R | 38 | 00111000 | output | |
| STATUS_MASTER_MAINPAGE | R | 39 | 00111001 | output | |
| FIFO_STATUS1 | R | 3A | 00111010 | output | |
| FIFO_STATUS2 | R | 3B | 00111011 | output | |
| RESERVED | - | 3C-3F | | | Reserved |
| TIMESTAMP0_REG | R | 40 | 01000000 | output | |
| TIMESTAMP1_REG | R | 41 | 01000001 | output | |
| TIMESTAMP2_REG | R | 42 | 01000010 | output | |
| TIMESTAMP3_REG | R | 43 | 01000011 | output | |
| RESERVED | - | 44-55 | | | Reserved |
| INT_CFG0 | R/W | 56 | 01010110 | 00000000 | |
| RESERVED | - | 57 | | | Reserved |
| INT_CFG1 | R/W | 58 | 01011000 | 00000000 | |
| THS_6D | R/W | 59 | 01011001 | 00000000 | |
| RESERVED | - | 5A | | | Reserved |
| WAKE_UP_THS | R/W | 5B | 01011011 | 00000000 | |
| WAKE_UP_DUR | R/W | 5C | 01011100 | 00000000 | |
| FREE_FALL | R/W | 5D | 01011101 | 00000000 | |
| MD1_CFG | R/W | 5E | 01011110 | 00000000 | |
| MD2_CFG | R/W | 5F | 01011111 | 00000000 | |
| RESERVED | - | 60-61 | | 00000000 | Reserved |
| I3C_BUS_AVB | R/W | 62 | 01100010 | 00000000 | |
| INTERNAL_FREQ_FINE | R | 63 | 01100011 | output | |
| RESERVED | - | 64-72 | | | Reserved |
| X_OFS_USR | R/W | 73 | 01110011 | 00000000 | |
| Y_OFS_USR | R/W | 74 | 01110100 | 00000000 | |
| Z_OFS_USR | R/W | 75 | 01110101 | 00000000 | |
| RESERVED | - | 76-77 | | | Reserved |
| FIFO_DATA_OUT_TAG | R | 78 | 01111000 | output | |

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| FIFO_DATA_OUT_X_L | R | 79 | 01111001 | output | |
| FIFO_DATA_OUT_X_H | R | 7A | 01111010 | output | |
| FIFO_DATA_OUT_Y_L | R | 7B | 01111011 | output | |
| FIFO_DATA_OUT_Y_H | R | 7C | 01111100 | output | |
| FIFO_DATA_OUT_Z_L | R | 7D | 01111101 | output | |
| FIFO_DATA_OUT_Z_H | R | 7E | 01111110 | output | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write data through the serial interface.

## 9.1 FUNC_CFG_ACCESS (01h)

Enable embedded functions register (R/W)

**Table 21. FUNC_CFG_ACCESS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FUNC_CFG_ACCESS | SHUB_REG_ACCESS | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 22. FUNC_CFG_ACCESS register description**

| | |
|---|---|
| FUNC_CFG_ACCESS | Enables access to the embedded functions configuration registers.<br>Default value: 0(1) |
| SHUB_REG_ACCESS | Enables access to the sensor hub (I²C master) registers.<br>Default value: 0(2) |

1. *Details concerning the embedded functions configuration registers are available in Section 10 Embedded functions register mapping and Section 11 Embedded functions register description.*
2. *Details concerning the sensor hub registers are available in Section 14 Sensor hub register mapping and Section 15 Sensor hub register description.*

## 9.2 PIN_CTRL (02h)

Enable SDO pin pull-up register (R/W)

**Table 23. PIN_CTRL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | SDO_PU_EN | 1(2) | 1(2) | 1(2) | 1(2) | 1(2) | 1(2) |

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

**Table 24. PIN_CTRL register description**

| | |
|---|---|
| SDO_PU_EN | Enables pull-up on SDO pin. Default value: 0<br>(0: SDO pin pull-up disconnected (default); 1: SDO pin with pull-up) |

## 9.3 FIFO_CTRL1 (07h)

FIFO control register 1 (R/W)

**Table 25. FIFO_CTRL1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WTM7 | WTM6 | WTM5 | WTM4 | WTM3 | WTM2 | WTM1 | WTM0 |

**Table 26. FIFO_CTRL1 register description**

| | |
|---|---|
| WTM[7:0] | FIFO watermark threshold, in conjunction with WTM8 in FIFO_CTRL2 (08h)<br>1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO<br>Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level. |

## 9.4 FIFO_CTRL2 (08h)

FIFO control register 2 (R/W)

**Table 27. FIFO_CTRL2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| STOP_ON_WTM | 0(1) | 0(1) | ODRCHG_EN | 0(1) | 0(1) | 0(1) | WTM8 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 28. FIFO_CTRL2 register**

| | |
|---|---|
| STOP_ON_WTM | Sensing chain FIFO stop values memorization at threshold level<br>(0: FIFO depth is not limited (default);<br>1: FIFO depth is limited to the threshold level, defined in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h) |
| ODRCHG_EN | Enables ODR CHANGE virtual sensor to be batched in FIFO |
| WTM8 | FIFO watermark threshold, in conjunction with WTM[7:0] in FIFO_CTRL1 (07h)<br>1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO<br>Watermark flag rises when the number of bytes written in FIFO is greater than or equal to the threshold level. |

## 9.5 FIFO_CTRL3 (09h)

FIFO control register 3 (R/W)

**Table 29. FIFO_CTRL3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BDR_GY_3 | BDR_GY_2 | BDR_GY_1 | BDR_GY_0 | BDR_XL_3 | BDR_XL_2 | BDR_XL_1 | BDR_XL_0 |

**Table 30. FIFO_CTRL3 register description**

| | |
|---|---|
| BDR_GY_[3:0] | Selects batch data rate (write frequency in FIFO) for gyroscope data.<br>(0000: gyroscope not batched in FIFO (default);<br>0001: 12.5 Hz;<br>0010: 26 Hz;<br>0011: 52 Hz;<br>0100: 104 Hz;<br>0101: 208 Hz;<br>0110: 417 Hz;<br>0111: 833 Hz;<br>1000: 1667 Hz;<br>1001: 3333 Hz;<br>1010: 6667 Hz;<br>1011: 6.5 Hz;<br>1100-1111: reserved) |
| BDR_XL_[3:0] | Selects batch data rate (write frequency in FIFO) for accelerometer data.<br>(0000: accelerometer not batched in FIFO (default);<br>0001: 12.5 Hz;<br>0010: 26 Hz;<br>0011: 52 Hz;<br>0100: 104 Hz;<br>0101: 208 Hz;<br>0110: 417 Hz;<br>0111: 833 Hz;<br>1000: 1667 Hz;<br>1001: 3333 Hz;<br>1010: 6667 Hz;<br>1011: 1.6 Hz;<br>1100-1111: reserved) |

## 9.6 FIFO_CTRL4 (0Ah)

FIFO control register 4 (R/W)

**Table 31. FIFO_CTRL4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DEC_TS_ BATCH_1 | DEC_TS_ BATCH_0 | ODR_T_ BATCH_1 | ODR_T_ BATCH_0 | 0(1) | FIFO_ MODE2 | FIFO_ MODE1 | FIFO_ MODE0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 32. FIFO_CTRL4 register description**

| | |
|---|---|
| DEC_TS_BATCH_[1:0] | Selects decimation for timestamp batching in FIFO. The write rate is the maximum rate between accelerometer and gyroscope BDR divided by decimation decoder.<br>(00: timestamp not batched in FIFO (default);<br>01: decimation 1: max(BDR_XL[Hz],BDR_GY[Hz]) [Hz];<br>10: decimation 8: max(BDR_XL[Hz],BDR_GY[Hz])/8 [Hz];<br>11: decimation 32: max(BDR_XL[Hz],BDR_GY[Hz])/32 [Hz]) |
| ODR_T_BATCH_[1:0] | Selects batch data rate (write frequency in FIFO) for temperature data<br>(00: temperature not batched in FIFO (default);<br>01: 1.6 Hz;<br>10: 12.5 Hz;<br>11: 52 Hz) |
| FIFO_MODE[2:0] | FIFO mode selection<br>(000: bypass mode: FIFO disabled;<br>001: FIFO mode: stops collecting data when FIFO is full;<br>010: reserved;<br>011: continuous-to-FIFO mode: continuous mode until trigger is deasserted, then FIFO mode;<br>100: bypass-to-continuous mode: bypass mode until trigger is deasserted, then continuous mode;<br>101: reserved;<br>110: continuous mode: if the FIFO is full, the new sample overwrites the older one;<br>111: bypass-to-FIFO mode: bypass mode until trigger is deasserted, then FIFO mode.) |

## 9.7 COUNTER_BDR_REG1 (0Bh)

Counter batch data rate register 1 (R/W)

**Table 33. COUNTER_BDR_REG1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| dataready_ pulsed | RST_COUNTER _BDR | TRIG_COUNTER _BDR | 0(1) | 0(1) | CNT_BDR_ TH_10 | CNT_BDR_ TH_9 | CNT_BDR_ TH_8 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 34. COUNTER_BDR_REG1 register description**

| | |
|---|---|
| dataready_pulsed | Enables pulsed data-ready mode<br>(0: data-ready latched mode (returns to 0 only after an interface reading) (default);<br>1: data-ready pulsed mode (the data ready pulses are 75 µs long) |
| RST_COUNTER_BDR | Resets the internal counter of batch events for a single sensor.<br>This bit is automatically reset to zero if it was set to 1. |
| TRIG_COUNTER_BDR | Selects the trigger for the internal counter of batch events between the accelerometer and gyroscope.<br>(0: accelerometer batch event;<br>1: gyroscope batch event) |
| CNT_BDR_TH_[10:8] | In conjunction with CNT_BDR_TH_[7:0] in COUNTER_BDR_REG2 (0Ch), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (3Bh) is set to 1. |

## 9.8 COUNTER_BDR_REG2 (0Ch)

Counter batch data rate register 2 (R/W)

**Table 35. COUNTER_BDR_REG2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CNT_BDR_ TH_7 | CNT_BDR_ TH_6 | CNT_BDR_ TH_5 | CNT_BDR_ TH_4 | CNT_BDR_ TH_3 | CNT_BDR_ TH_2 | CNT_BDR_ TH_1 | CNT_BDR_ TH_0 |

**Table 36. COUNTER_BDR_REG2 register description**

| | |
|---|---|
| CNT_BDR_TH_[7:0] | In conjunction with CNT_BDR_TH_[10:8] in COUNTER_BDR_REG1 (0Bh), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (3Bh) is set to 1. |

## 9.9 INT1_CTRL (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1 when the MIPI I3C℠ dynamic address is not assigned (I²C or SPI is used). Some bits can also be used to trigger an IBI (in-band interrupt) when the MIPI I3C℠ interface is used. The output of the pin is the OR combination of the signals selected here and in register MD1_CFG (5Eh).

**Table 37. INT1_CTRL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DEN_DRDY_flag | INT1_CNT_BDR | INT1_FIFO_FULL | INT1_FIFO_OVR | INT1_FIFO_TH | INT1_BOOT | INT1_DRDY_G | INT1_DRDY_XL |

**Table 38. INT1_CTRL register description**

| | |
|---|---|
| DEN_DRDY_flag | Sends DEN_DRDY (DEN stamped on sensor data flag) to the INT1 pin. |
| INT1_CNT_BDR | Enables COUNTER_BDR_IA interrupt on INT1. |
| INT1_FIFO_FULL | Enables FIFO full flag interrupt on the INT1 pin.<br>It can also be used to trigger an IBI when the MIPI I3C℠ interface is used. |
| INT1_FIFO_OVR | Enables FIFO overrun interrupt on the INT1 pin.<br>It can also be used to trigger an IBI when the MIPI I3C℠ interface is used. |
| INT1_FIFO_TH | Enables FIFO threshold interrupt on the INT1 pin.<br>It can also be used to trigger an IBI when the MIPI I3C℠ interface is used. |
| INT1_BOOT | Enables boot status on the INT1 pin. |
| INT1_DRDY_G | Enables gyroscope data-ready interrupt on the INT1 pin.<br>It can also be used to trigger an IBI when the MIPI I3C℠ interface is used. |
| INT1_DRDY_XL | Enables accelerometer data-ready interrupt on the INT1 pin.<br>It can also be used to trigger an IBI when the MIPI I3C℠ interface is used. |

## 9.10 INT2_CTRL (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2 when the MIPI I3C dynamic address is not assigned (I²C or SPI is used). Some bits can also be used to trigger an IBI when the MIPI I3C℠ interface is used. The output of the pin is the OR combination of the signals selected here and in register MD2_CFG (5Fh).

**Table 39. INT2_CTRL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | INT2_ CNT_BDR | INT2_ FIFO_FULL | INT2_ FIFO_OVR | INT2_ FIFO_TH | INT2_ DRDY_TEMP | INT2_ DRDY_G | INT2_ DRDY_XL |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 40. INT2_CTRL register description**

| | |
|---|---|
| INT2_CNT_BDR | Enables COUNTER_BDR_IA interrupt on the INT2 pin. |
| INT2_FIFO_FULL | Enables FIFO full flag interrupt on the INT2 pin. |
| INT2_FIFO_OVR | Enables FIFO overrun interrupt on the INT2 pin. |
| INT2_FIFO_TH | Enables FIFO threshold interrupt on the INT2 pin. |
| INT2_DRDY_TEMP | Enables temperature sensor data-ready interrupt on the INT2 pin.<br>It can be also used to trigger an IBI when the MIPI I3C℠ interface is used and INT2_ON_INT1 = 1 in CTRL4_C (13h). |
| INT2_DRDY_G | Enables gyroscope data-ready interrupt on the INT2 pin. |
| INT2_DRDY_XL | Enables accelerometer data-ready interrupt on the INT2 pin. |

## 9.11 WHO_AM_I (0Fh)

WHO_AM_I register (R). This is a read-only register. Its value is fixed at 6Bh.

**Table 41. Who_Am_I register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |

## 9.12 CTRL1_XL (10h)

Accelerometer control register 1 (R/W)

**Table 42. CTRL1_XL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ODR_XL3 | ODR_XL2 | ODR_XL1 | ODR_XL0 | FS1_XL | FS0_XL | LPF2_XL_EN | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 43. CTRL1_XL register description**

| | |
|---|---|
| ODR_XL[3:0] | Accelerometer ODR selection (see Table 44) |
| FS[1:0]_XL | Accelerometer full-scale selection. Default value: 00<br>(00: ±2 *g*; 01: ±16 *g*; 10: ±4 *g*; 11: ±8 *g*) |
| LPF2_XL_EN | Accelerometer high-resolution selection<br>(0: output from first stage digital filtering selected (default);<br>1: output from LPF2 second filtering stage selected) |

**Table 44. Accelerometer ODR register setting**

| ODR_XL3 | ODR_XL2 | ODR_XL1 | ODR_XL0 | ODR selection [Hz] when XL_HM_MODE = 1 in CTRL6_C (15h) | ODR selection [Hz] when XL_HM_MODE = 0 in CTRL6_C (15h) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Power-down | Power-down |
| 1 | 0 | 1 | 1 | 1.6 Hz (low power only) | N.A. |
| 0 | 0 | 0 | 1 | 12.5 Hz (low power) | 12.5 Hz (high performance) |
| 0 | 0 | 1 | 0 | 26 Hz (low power) | 26 Hz (high performance) |
| 0 | 0 | 1 | 1 | 52 Hz (low power) | 52 Hz (high performance) |
| 0 | 1 | 0 | 0 | 104 Hz (low power) | 104 Hz (high performance) |
| 0 | 1 | 0 | 1 | 208 Hz (low power) | 208 Hz (high performance) |
| 0 | 1 | 1 | 0 | 416 Hz (high performance) | 416 Hz (high performance) |
| 0 | 1 | 1 | 1 | 833 Hz (high performance) | 833 Hz (high performance) |
| 1 | 0 | 0 | 0 | 1667 Hz (high performance) | 1667 Hz (high performance) |
| 1 | 0 | 0 | 1 | 3333 Hz (high performance) | 3333 Hz (high performance) |
| 1 | 0 | 1 | 0 | 6667 Hz (high performance) | 6667 Hz (high performance) |
| 1 | 1 | x | x | Reserved | Reserved |

## 9.13 CTRL2_G (11h)

Gyroscope control register 2 (R/W)

**Table 45. CTRL2_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ODR_G3 | ODR_G2 | ODR_G1 | ODR_G0 | FS1_G | FS0_G | FS_125 | FS_4000 |

**Table 46. CTRL2_G register description**

| | |
|---|---|
| ODR_G[3:0] | Gyroscope output data rate selection. Default value: 0000<br>(Refer to Table 47) |
| FS[1:0]_G | Gyroscope chain full-scale selection<br>(00: ±250 dps;<br>01: ±500 dps;<br>10: ±1000 dps;<br>11: ±2000 dps) |
| FS_125 | Selects gyroscope chain full-scale ±125 dps<br>(0: FS selected through bits FS[1:0]_G;<br>1: FS set to ±125 dps) |
| FS_4000 | Selects gyroscope chain full-scale ±4000 dps<br>(0: FS selected through bits FS[1:0]_G or FS_125;<br>1: FS set to ±4000 dps) |

**Table 47. Gyroscope ODR configuration setting**

| ODR_G3 | ODR_G2 | ODR_G1 | ODR_G0 | ODR selection [Hz] when G_HM_MODE = 1 in CTRL7_G (16h) | ODR selection [Hz] when G_HM_MODE = 0 in CTRL7_G (16h) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Power-down | Power-down |
| 0 | 0 | 0 | 1 | 12.5 Hz (low power) | 12.5 Hz (high performance) |
| 0 | 0 | 1 | 0 | 26 Hz (low power) | 26 Hz (high performance) |
| 0 | 0 | 1 | 1 | 52 Hz (low power) | 52 Hz (high performance) |
| 0 | 1 | 0 | 0 | 104 Hz (low power) | 104 Hz (high performance) |
| 0 | 1 | 0 | 1 | 208 Hz (low power) | 208 Hz (high performance) |
| 0 | 1 | 1 | 0 | 416 Hz (high performance) | 416 Hz (high performance) |
| 0 | 1 | 1 | 1 | 833 Hz (high performance) | 833 Hz (high performance) |
| 1 | 0 | 0 | 0 | 1667 Hz (high performance) | 1667 Hz (high performance) |
| 1 | 0 | 0 | 1 | 3333 Hz (high performance) | 3333 Hz (high performance) |
| 1 | 0 | 1 | 0 | 6667 Hz (high performance) | 6667 Hz (high performance) |
| 1 | 0 | 1 | 1 | Reserved | Reserved |

## 9.14 CTRL3_C (12h)

Control register 3 (R/W)

**Table 48. CTRL3_C register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BOOT | BDU | H_LACTIVE | PP_OD | SIM | IF_INC | 0[1] | SW_RESET |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 49. CTRL3_C register description**

| | |
|---|---|
| BOOT | Reboots memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content)<br>Note: the accelerometer must be ON. This bit is automatically cleared. |
| BDU | Block data update. Default value: 0<br>(0: continuous update;<br>1: output registers are not updated until MSB and LSB have been read) |
| H_LACTIVE | Interrupt activation level. Default value: 0<br>(0: interrupt output pins active high; 1: interrupt output pins active low |
| PP_OD | Push-pull/open-drain selection on INT1 and INT2 pins. This bit must be set to 0 when H_LACTIVE is set to 1. Default value: 0<br>(0: push-pull mode; 1: open-drain mode) |
| SIM | SPI serial interface mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface) |
| IF_INC | Register address automatically incremented during a multiple byte access with a serial interface (I²C or SPI). Default value: 1<br>(0: disabled; 1: enabled) |
| SW_RESET | Software reset. Default value: 0<br>(0: normal mode; 1: reset device)<br>This bit is automatically cleared. |

## 9.15 CTRL4_C (13h)

Control register 4 (R/W)

**Table 50. CTRL4_C register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | SLEEP_G | INT2_on_INT1 | 0(1) | DRDY_MASK | I2C_disable | LPF1_SEL_G | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 51. CTRL4_C register description**

| | |
|---|---|
| SLEEP_G | Enables gyroscope sleep mode. Default value:0<br>(0: disabled; 1: enabled) |
| INT2_on_INT1 | Enables all interrupt signals available on the INT1 pin. Default value: 0<br>(0: interrupt signals divided between the INT1 and INT2 pins;<br>1: all interrupt signals in logic or on the INT1 pin) |
| DRDY_MASK | Enables data available<br>(0: disabled;<br>1: mask DRDY on pin (both accelerometer and gyroscope) until filter settling ends (accelerometer and gyroscope independently masked). |
| I2C_disable | Disables I²C interface. Default value: 0<br>(0: SPI, I²C, and MIPI I3C℠ interfaces enabled (default); 1: I²C interface disabled) |
| LPF1_SEL_G | Enables gyroscope digital LPF1; the bandwidth can be selected through FTYPE[2:0] in CTRL6_C (15h).<br>(0: disabled; 1: enabled) |

## 9.16 CTRL5_C (14h)

Control register 5 (R/W)

**Table 52. CTRL5_C register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | ROUNDING1 | ROUNDING0 | 0(1) | ST1_G | ST0_G | ST1_XL | ST0_XL |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 53. CTRL5_C register description**

| | |
|---|---|
| ROUNDING[1:0] | Circular burst mode (wraparound) read of the output registers. Default value: 00<br>(00: no wraparound;<br>01: accelerometer only;<br>10: gyroscope only;<br>11: gyroscope + accelerometer) |
| ST[1:0]_G | Enables angular rate sensor self-test. Default value: 00<br>(00: self-test disabled; other: refer to Table 54) |
| ST[1:0]_XL | Enables linear acceleration sensor self-test. Default value: 00<br>(00: self-test disabled; other: refer to Table 55) |

**Table 54. Angular rate sensor self-test mode selection**

| ST1_G | ST0_G | Self-test mode |
|---|---|---|
| 0 | 0 | Normal mode |
| 0 | 1 | Positive sign self-test |
| 1 | 0 | Not allowed |
| 1 | 1 | Negative sign self-test |

**Table 55. Linear acceleration sensor self-test mode selection**

| ST1_XL | ST0_XL | Self-test mode |
|---|---|---|
| 0 | 0 | Normal mode |
| 0 | 1 | Positive sign self-test |
| 1 | 0 | Negative sign self-test |
| 1 | 1 | Not allowed |

## 9.17 CTRL6_C (15h)

Control register 6 (R/W)

**Table 56. CTRL6_C register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TRIG_EN | LVL1_EN | LVL2_EN | XL_HM_MODE | USR_OFF_W | FTYPE_2 | FTYPE_1 | FTYPE_0 |

**Table 57. CTRL6_C register description**

| | |
|---|---|
| TRIG_EN | Enables DEN data edge-sensitive trigger mode. Refer to Table 58. |
| LVL1_EN | Enables DEN data level-sensitive trigger mode. Refer to Table 58. |
| LVL2_EN | Enables DEN level-sensitive latched mode. Refer toTable 58. |
| XL_HM_MODE | Disables high-performance operating mode for accelerometer. Default value: 0<br>(0: high-performance operating mode enabled;<br>1: high-performance operating mode disabled) |
| USR_OFF_W | Weight of XL user offset bits of registers X_OFS_USR (73h), Y_OFS_USR (74h), Z_OFS_USR (75h)<br>(0: $2^{-10}$ *g*/LSB;<br>1: $2^{-6}$ *g*/LSB) |
| FTYPE[2:0] | Gyroscope low-pass filter (LPF1) bandwidth selection. Table 59 shows the selectable bandwidth values. |

**Table 58. Trigger mode selection**

| TRIG_EN, LVL1_EN, LVL2_EN | Trigger mode |
|---|---|
| 100 | Edge-sensitive trigger mode is selected |
| 010 | Level-sensitive trigger mode is selected |
| 011 | Level-sensitive latched mode is selected |
| 110 | Level-sensitive FIFO mode is selected |

**Table 59. Gyroscope LPF1 bandwidth selection**

| FTYPE[2:0] | 12.5 Hz | 26 Hz | 52 Hz | 104 Hz | 208 Hz | 416 Hz | 833 Hz | 1667 Hz | 3333 Hz | 6667 Hz |
|---|---|---|---|---|---|---|---|---|---|---|
| 000 | 4.3 | 8.3 | 16.7 | 33 | 67 | 133 | 222 | 274 | 292 | 297 |
| 001 | 4.3 | 8.3 | 16.7 | 33 | 67 | 128 | 186 | 212 | 220 | 223 |
| 010 | 4.3 | 8.3 | 16.7 | 33 | 67 | 112 | 140 | 150 | 153 | 154 |
| 011 | 4.3 | 8.3 | 16.7 | 33 | 67 | 134 | 260 | 390 | 451 | 470 |
| 100 | 4.3 | 8.3 | 16.7 | 34 | 62 | 86 | 96 | 99 | NA | |
| 101 | 4.3 | 8.3 | 16.9 | 31 | 43 | 48 | 49 | 50 | NA | |
| 110 | 4.3 | 8.3 | 13.4 | 19 | 23 | 24.6 | 25 | 25 | NA | |
| 111 | 4.3 | 8.3 | 9.8 | 11.6 | 12.2 | 12.4 | 12.6 | 12.6 | NA | |

## 9.18 CTRL7_G (16h)

Control register 7 (R/W)

**Table 60. CTRL7_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| G_HM_MODE | HP_EN_G | HPM1_G | HPM0_G | 0(1) | 0(1) | USR_OFF_ON_OUT | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

| | |
|---|---|
| G_HM_MODE | Disables high-performance operating mode for gyroscope. Default: 0<br>(0: high-performance operating mode enabled;<br>1: high-performance operating mode disabled) |
| HP_EN_G | Enables gyroscope digital high-pass filter. The filter is enabled only if the gyroscope is in HP mode. Default value: 0<br>(0: HPF disabled; 1: HPF enabled) |
| HPM_G[1:0] | Gyroscope digital HP filter cutoff selection. Default: 00<br>(00: 16 mHz;<br>01: 65 mHz;<br>10: 260 mHz;<br>11: 1.04 Hz) |
| USR_OFF_ON_OUT | Enables accelerometer user offset correction block; it's valid for the low-pass path - see Figure 19 . Default value: 0<br>(0: accelerometer user offset correction block bypassed;<br>1: accelerometer user offset correction block enabled) |

## 9.19 CTRL8_XL (17h)

Control register 8 (R/W)

**Table 61. CTRL8_XL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| HPCF_XL_2 | HPCF_XL_1 | HPCF_XL_0 | HP_REF_MODE_XL | FASTSETTL_MODE_XL | HP_SLOPE_XL_EN | 0(1) | LOW_PASS_ON_6D |

1. *This bit must be set to 0 for the correct operation of the device.*

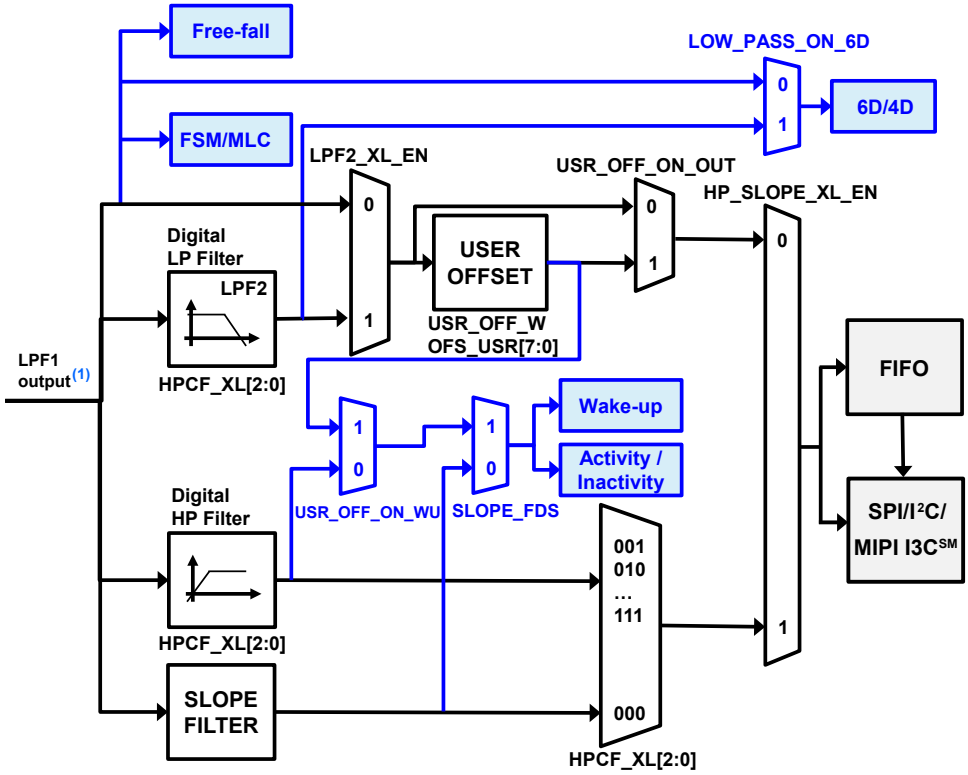
| | |
|---|---|
| HPCF_XL_[2:0] | Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to Table 62. |
| HP_REF_MODE_XL | Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be 1). Default value: 0(1)<br>(0: disabled, 1: enabled) |
| FASTSETTL_MODE_XL | Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the second samples after writing this bit. Active only during device exit from power- down mode. Default value: 0<br>(0: disabled, 1: enabled) |
| HP_SLOPE_XL_EN | Accelerometer slope filter / high-pass filter selection. Refer to Figure 22. |
| LOW_PASS_ON_6D | LPF2 on 6D function selection. Refer to Figure 22. Default value: 0<br>(0: ODR/2 low-pass filtered data sent to 6D interrupt function;<br>1: LPF2 output data sent to 6D interrupt function) |

1. *When enabled, the first output data have to be discarded.*

Table 62. **Accelerometer bandwidth configurations**

| Filter type | HP_SLOPE_ XL_EN | LPF2_XL_EN | HPCF_XL_[2:0] | Bandwidth |
|---|---|---|---|---|
| Low pass | 0 | 0 | - | ODR/2 |
| | | 1 | 000 | ODR/4 |
| | | | 001 | ODR/10 |
| | | | 010 | ODR/20 |
| | | | 011 | ODR/45 |
| | | | 100 | ODR/100 |
| | | | 101 | ODR/200 |
| | | | 110 | ODR/400 |
| | | | 111 | ODR/800 |
| High pass | 1 | - | 000 | SLOPE (ODR/4) |
| | | | 001 | ODR/10 |
| | | | 010 | ODR/20 |
| | | | 011 | ODR/45 |
| | | | 100 | ODR/100 |
| | | | 101 | ODR/200 |
| | | | 110 | ODR/400 |
| | | | 111 | ODR/800 |

Figure 22. **Accelerometer block diagram**




1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode and ODR up to 833 Hz. This value is equal to 780 Hz when the accelerometer is in low-power mode.*

## 9.20 CTRL9_XL (18h)

Control register 9 (R/W)

**Table 63. CTRL9_XL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DEN_X | DEN_Y | DEN_Z | DEN_XL_G | DEN_XL_EN | DEN_LH | I3C_disable | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 64. CTRL9_XL register description**

| | |
|---|---|
| DEN_X | DEN value stored in LSB of X-axis. Default value: 1<br>(0: DEN not stored in X-axis LSB; 1: DEN stored in X-axis LSB) |
| DEN_Y | DEN value stored in LSB of Y-axis. Default value: 1<br>(0: DEN not stored in Y-axis LSB; 1: DEN stored in Y-axis LSB) |
| DEN_Z | DEN value stored in LSB of Z-axis. Default value: 1<br>(0: DEN not stored in Z-axis LSB; 1: DEN stored in Z-axis LSB) |
| DEN_XL_G | DEN stamping sensor selection. Default value: 0<br>(0: DEN pin info stamped in the gyroscope axis selected by bits [7:5];<br>1: DEN pin info stamped in the accelerometer axis selected by bits [7:5]) |
| DEN_XL_EN | Extends DEN functionality to accelerometer sensor. Default value: 0<br>(0: disabled; 1: enabled) |
| DEN_LH | DEN active level configuration. Default value: 0<br>(0: active low; 1: active high) |
| I3C_disable | Disables MIPI I3C℠ communication protocol(1)<br>(0: SPI, I²C, MIPI I3C℠ interfaces enabled (default);<br>1: MIPI I3C℠ interface disabled) |

1. *It is recommended to set this bit to 1 during the initial device configuration phase, when the I3C interface is not used.*

## 9.21 CTRL10_C (19h)

Control register 10 (R/W)

**Table 65. CTRL10_C register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | TIMESTAMP_EN | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 66. CTRL10_C register description**

| | |
|---|---|
| TIMESTAMP_EN | Enables timestamp counter. Default value: 0<br>(0: disabled; 1: enabled)<br>The counter is readable in TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h). |

## 9.22 ALL_INT_SRC (1Ah)

Source register for all interrupts (R)

**Table 67. ALL_INT_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TIMESTAMP_ENDCOUNT | 0 | SLEEP_CHANGE_IA | D6D_IA | 0 | 0 | WU_IA | FF_IA |

**Table 68. ALL_INT_SRC register description**

| | |
|---|---|
| TIMESTAMP_ENDCOUNT | Alerts timestamp overflow within 6.4 ms |
| SLEEP_CHANGE_IA | Detects change event in activity/inactivity status. Default value: 0<br>(0: change status not detected; 1: change status detected) |
| D6D_IA | Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0<br>(0: change in position not detected; 1: change in position detected) |
| WU_IA | Wake-up event status. Default value: 0<br>(0: event not detected, 1: event detected) |
| FF_IA | Free-fall event status. Default value: 0<br>(0: event not detected, 1: event detected) |

## 9.23 WAKE_UP_SRC (1Bh)

Wake-up interrupt source register (R)

**Table 69. WAKE_UP_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | SLEEP_CHANGE_IA | FF_IA | SLEEP_STATE | WU_IA | X_WU | Y_WU | Z_WU |

**Table 70. WAKE_UP_SRC register description**

| | |
|---|---|
| SLEEP_CHANGE_IA | Detects change event in activity/inactivity status. Default value: 0<br>(0: change status not detected; 1: change status detected) |
| FF_IA | Free-fall event detection status. Default: 0<br>(0: free-fall event not detected; 1: free-fall event detected) |
| SLEEP_STATE | Sleep event status. Default value: 0<br>(0: sleep event not detected; 1: sleep event detected) |
| WU_IA | Wake-up event detection status. Default value: 0<br>(0: wake-up event not detected; 1: wake-up event detected.) |
| X_WU | Wake-up event detection status on X-axis. Default value: 0<br>(0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected) |
| Y_WU | Wake-up event detection status on Y-axis. Default value: 0<br>(0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected) |
| Z_WU | Wake-up event detection status on Z-axis. Default value: 0<br>(0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected) |

## 9.24 DRD_SRC (1Dh)

Portrait, landscape, face-up and face-down source register (R)

**Table 71. D6D_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DEN_DRDY | D6D_IA | ZH | ZL | YH | YL | XH | XL |

**Table 72. D6D_SRC register description**

| | |
|---|---|
| DEN_DRDY | DEN data-ready signal. It is set high when data output is related to the data coming from a DEN active condition. (1) |
| D6D_IA | Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0<br>(0: change position not detected; 1: change position detected) |
| ZH | Z-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected) |
| ZL | Z-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected) |
| YH | Y-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected) |
| YL | Y-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected) |
| XH | X-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected) |
| XL | X-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected) |

1. *The DEN data-ready signal can be latched or pulsed depending on the value of the dataready_pulsed bit of the COUNTER_BDR_REG1 (0Bh) register.*

## 9.25 STATUS_REG (1Eh)

Status register (R)

**Table 73. STATUS_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | TDA | GDA | XLDA |

**Table 74. STATUS_REG register description**

| | |
|---|---|
| TDA | Temperature new data available. Default: 0<br>(0: no set of data is available at temperature sensor output;<br>1: a new set of data is available at temperature sensor output) |
| GDA | Gyroscope new data available. Default value: 0<br>(0: no set of data available at gyroscope output;<br>1: a new set of data is available at gyroscope output) |
| XLDA | Accelerometer new data available. Default value: 0<br>(0: no set of data available at accelerometer output;<br>1: a new set of data is available at accelerometer output) |

## 9.26 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two's complement.

**Table 75. OUT_TEMP_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |

**Table 76. OUT_TEMP_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Temp15 | Temp14 | Temp13 | Temp12 | Temp11 | Temp10 | Temp9 | Temp8 |

**Table 77. OUT_TEMP register description**

| | |
|---|---|
| Temp[15:0] | Temperature sensor output data<br>The value is expressed as two's complement sign extended on the MSB. |

## 9.27 OUTX_H_G (23h), OUTX_L_G (22h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two’s complement.

**Table 78. OUTX_H_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 79. OUTX_L_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 80. OUTX_H_G, OUTX_L_G register description**

| | |
|---|---|
| D[15:0] | Gyroscope pitch axis output expressed in two's complement |

## 9.28 OUTY_H_G (25h), OUTY_L_G (24h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two’s complement.

**Table 81. OUTY_H_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 82. OUTY_L_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 83. OUTY_H_G, OUTY_L_G register description**

| | |
|---|---|
| D[15:0] | Gyroscope roll axis output expressed in two’s complement |

## 9.29 OUTZ_H_G (27h), OUTZ_L_G (26h)

Angular rate sensor pitch yaw (Z) angular rate output register (R). The value is expressed as a 16-bit word in two’s complement.

**Table 84. OUTZ_H_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 85. OUTZ_L_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 86. OUTZ_H_G, OUTZ_L_G register description**

| | |
|---|---|
| D[15:0] | Gyroscope yaw axis output expressed in two’s complement |

## 9.30 OUTX_H_A (29h), OUTX_L_A (28h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 87. OUTX_H_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 88. OUTX_L_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 89. OUTX_H_A, OUTX_L_A register description**

| | |
|---|---|
| D[15:0] | Accelerometer X-axis output expressed as two's complement |

## 9.31 OUTY_H_A (2Bh), OUTY_L_A (2Ah)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 90. OUTY_H_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 91. OUTY_L_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 92. OUTY_H_A, OUTY_L_A register description**

| | |
|---|---|
| D[15:0] | Accelerometer Y-axis output expressed as two's complement |

## 9.32 OUTZ_H_A (2Dh), OUTZ_L_A (2Ch)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 93. OUTZ_H_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 94. OUTZ_L_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 95. OUTZ_H_A, OUTZ_L_A register description**

| | |
|---|---|
| D[15:0] | Accelerometer Z-axis output expressed as two's complement |

## 9.33 EMB_FUNC_STATUS_MAINPAGE (35h)

Embedded function status register (R)

**Table 96. EMB_FUNC_STATUS_MAINPAGE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM_LC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 97. EMB_FUNC_STATUS_MAINPAGE register description**

| | |
|---|---|
| IS_FSM_LC | Interrupt status bit for FSM long counter timeout interrupt event.<br>(1: interrupt detected; 0: no interrupt) |

## 9.34 FSM_STATUS_A_MAINPAGE (36h)

Finite state machine status register (R)

**Table 98. FSM_STATUS_A_MAINPAGE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM8 | IS_FSM7 | IS_FSM6 | IS_FSM5 | IS_FSM4 | IS_FSM3 | IS_FSM2 | IS_FSM1 |

**Table 99. FSM_STATUS_A_MAINPAGE register description**

| | |
|---|---|
| IS_FSM8 | Interrupt status bit for FSM8 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM7 | Interrupt status bit for FSM7 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM6 | Interrupt status bit for FSM6 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM5 | Interrupt status bit for FSM5 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM4 | Interrupt status bit for FSM4 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM3 | Interrupt status bit for FSM3 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM2 | Interrupt status bit for FSM2 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM1 | Interrupt status bit for FSM1 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |

## 9.35 FSM_STATUS_B_MAINPAGE (37h)

Finite state machine status register (R)

**Table 100. FSM_STATUS_B_MAINPAGE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM16 | IS_FSM15 | IS_FSM14 | IS_FSM13 | IS_FSM12 | IS_FSM11 | IS_FSM10 | IS_FSM9 |

**Table 101. FSM_STATUS_B_MAINPAGE register description**

| | |
|---|---|
| IS_FSM16 | Interrupt status bit for FSM16 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM15 | Interrupt status bit for FSM15 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM14 | Interrupt status bit for FSM14 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM13 | Interrupt status bit for FSM13 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM12 | Interrupt status bit for FSM12 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM11 | Interrupt status bit for FSM11 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM10 | Interrupt status bit for FSM10 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM9 | Interrupt status bit for FSM9 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |

## 9.36 MLC_STATUS_MAINPAGE (38h)

Machine learning core status register (R)

**Table 102. MLC_STATUS_MAINPAGE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_MLC8 | IS_MLC7 | IS_MLC6 | IS_MLC5 | IS_MLC4 | IS_MLC3 | IS_MLC2 | IS_MLC1 |

**Table 103. MLC_STATUS_MAINPAGE register description**

| | |
|---|---|
| IS_MLC8 | Interrupt status bit for MLC8 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC7 | Interrupt status bit for MLC7 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC6 | Interrupt status bit for MLC6 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC5 | Interrupt status bit for MLC5 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC4 | Interrupt status bit for MLC4 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC3 | Interrupt status bit for MLC3 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC2 | Interrupt status bit for MLC2 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC1 | Interrupt status bit for MLC1 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |

## 9.37 STATUS_MASTER_MAINPAGE (39h)

Sensor hub source register (R)

**Table 104. STATUS_MASTER_MAINPAGE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WR_ONCE_DONE | SLAVE3_NACK | SLAVE2_NACK | SLAVE1_NACK | SLAVE0_NACK | 0 | 0 | SENS_HUB_ENDOP |

**Table 105. STATUS_MASTER_MAINPAGE register description**

| | |
|---|---|
| WR_ONCE_DONE | When the bit WRITE_ONCE in MASTER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on slave 0 has been performed and completed. Default value: 0 |
| SLAVE3_NACK | This bit is set to 1 if not acknowledge occurs on slave 3 communication. Default value: 0 |
| SLAVE2_NACK | This bit is set to 1 if not acknowledge occurs on slave 2 communication. Default value: 0 |
| SLAVE1_NACK | This bit is set to 1 if not acknowledge occurs on slave 1 communication. Default value: 0 |
| SLAVE0_NACK | This bit is set to 1 if not acknowledge occurs on slave 0 communication. Default value: 0 |
| SENS_HUB_ENDOP | Sensor hub communication status. Default value: 0<br>(0: sensor hub communication not concluded;<br>1: sensor hub communication concluded) |

## 9.38 FIFO_STATUS1 (3Ah)

FIFO status register 1 (R)

**Table 106. FIFO_STATUS1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DIFF_FIFO_7 | DIFF_FIFO_6 | DIFF_FIFO_5 | DIFF_FIFO_4 | DIFF_FIFO_3 | DIFF_FIFO_2 | DIFF_FIFO_1 | DIFF_FIFO_0 |

**Table 107. FIFO_STATUS1 register description**

| | |
|---|---|
| DIFF_FIFO_[7:0] | Number of unread sensor data (TAG + 6 bytes) stored in FIFO<br>In conjunction with DIFF_FIFO[9:8] in FIFO_STATUS2 (3Bh). |

## 9.39 FIFO_STATUS2 (3Bh)

FIFO status register 2 (R)

**Table 108. FIFO_STATUS2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FIFO_ WTM_IA | FIFO_ OVR_IA | FIFO_ FULL_IA | COUNTER_ BDR_IA | FIFO_OVR_ LATCHED | 0 | DIFF_FIFO_9 | DIFF_FIFO_8 |

**Table 109. FIFO_STATUS2 register description**

| | |
|---|---|
| FIFO_WTM_IA | FIFO watermark status. Default value: 0<br>(0: FIFO filling is lower than WTM;<br>1: FIFO filling is equal to or greater than WTM)<br>Watermark is set through bits WTM[8:0] in FIFO_CTRL2 (08h) and FIFO_CTRL1 (07h). |
| FIFO_OVR_IA | FIFO overrun status. Default value: 0<br>(0: FIFO is not completely filled; 1: FIFO is completely filled) |
| FIFO_FULL_IA | Smart FIFO full status. Default value: 0<br>(0: FIFO is not full; 1: FIFO will be full at the next ODR) |
| COUNTER_BDR_IA | Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0<br>This bit is reset when these registers are read. |
| FIFO_OVR_LATCHED | Latched FIFO overrun status. Default value: 0<br>This bit is reset when this register is read. |
| DIFF_FIFO_[9:8] | Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00<br>In conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (3Ah) |

## 9.40 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 25 µs.

**Table 110. TIMESTAMP3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 |

**Table 111. TIMESTAMP2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |

**Table 112. TIMESTAMP1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 113. TIMESTAMP0 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| D[31:0] | Timestamp output registers: 1LSB = 25 µs |

The formula below can be used to calculate a better estimation of the actual timestamp resolution:
TS_Res = 1 / (40000 + (0.0015 * INTERNAL_FREQ_FINE * 40000))
where INTERNAL_FREQ_FINE is the content of INTERNAL_FREQ_FINE (63h).

## 9.41 INT_CFG0 (56h)

Activity/inactivity functions, configuration of filtering, and interrupt latch mode configuration (R/W)

**Table 114. INT_CFG0 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | INT_CLR_ON_READ | SLEEP_STATUS_ON_INT | SLOPE_FDS | 0(1) | 0(1) | 0(1) | LIR |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 115. INT_CFG0 register description**

| | |
|---|---|
| INT_CLR_ON_READ | This bit allows immediately clearing the latched interrupts of an event detection upon the read of the corresponding status register. It must be set to 1 together with LIR. Default value: 0<br>(0: latched interrupt signal cleared at the end of the ODR period;<br>1: latched interrupt signal immediately cleared) |
| SLEEP_STATUS_ON_INT | Activity/inactivity interrupt mode configuration.<br>If INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bits are enabled, drives the sleep status or sleep change on INT pins. Default value: 0<br>(0: sleep change notification on INT pins; 1: sleep status reported on INT pins) |
| SLOPE_FDS | HPF or slope filter selection on wake-up and activity/inactivity functions. Default value: 0<br>(0: SLOPE filter applied; 1: HPF applied) |
| LIR | Latched interrupt. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched) |

## 9.42 INT_CFG1 (58h)

Enable interrupt function register (R/W)

**Table 116. INT_CFG1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INTERRUPTS_ENABLE | INACT_EN1 | INACT_EN0 | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 117. INT_CFG1 register description**

| | |
|---|---|
| INTERRUPTS_ENABLE | Enables hardcoded functions |
| INACT_EN[1:0] | Enables activity/inactivity (sleep) function. Default value: 00<br>(00: stationary/motion-only interrupts generated, XL and gyro do not change;<br>01: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro does not change;<br>10: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to sleep mode;<br>11: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to power-down mode) |

## 9.43 THS_6D (59h)

Portrait/landscape position register (R/W)

**Table 118. THS_6D register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D4D_EN | SIXD_THS1 | SIXD_THS0 | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 119. THS_6D register description**

| | |
|---|---|
| D4D_EN | Enables detection of 4D orientation. Z-axis position detection is disabled. Default value: 0<br>(0: disabled; 1: enabled) |
| SIXD_THS[1:0] | Threshold for 4D/6D function<br>(00: 80 degrees (default);<br>01: 70 degrees;<br>10: 60 degrees;<br>11: 50 degrees) |

## 9.44 WAKE_UP_THS (5Bh)

Wake-up configuration register (R/W)

**Table 120. WAKE_UP_THS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | USR_OFF_ON_WU | WK_THS5 | WK_THS4 | WK_THS3 | WK_THS2 | WK_THS1 | WK_THS0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 121. WAKE_UP_THS register description**

| | |
|---|---|
| USR_OFF_ON_WU | Sends the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wake-up and the activity/inactivity functions. Default value: 0 |
| WK_THS[5:0] | Threshold for wake-up: 1 LSB weight depends on WAKE_THS_W in WAKE_UP_DUR (5Ch). Default value: 000000 |

## 9.45 WAKE_UP_DUR (5Ch)

Free-fall, wake-up and sleep mode functions duration setting register (R/W)

**Table 122. WAKE_UP_DUR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FF_DUR5 | WAKE_DUR1 | WAKE_DUR0 | WAKE_ THS_W | SLEEP_ DUR3 | SLEEP_ DUR2 | SLEEP_ DUR1 | SLEEP_ DUR0 |

**Table 123. WAKE_UP_DUR register description**

| | |
|---|---|
| FF_DUR5 | Free-fall duration event. Default: 0<br>For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in FREE_FALL (5Dh) configuration.<br>1 LSB = 1 ODR_time |
| WAKE_DUR[1:0] | Wake-up duration event. Default: 00<br>1LSB = 1 ODR_time |
| WAKE_THS_W | Weight of 1 LSB of wake-up threshold. Default: 0<br>(0: 1 LSB =FS_XL / ($2^6$);<br>1: 1 LSB = FS_XL / ($2^8$)) |
| SLEEP_DUR[3:0] | Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR)<br>1 LSB = 512 ODR |

## 9.46 FREE_FALL (5Dh)

Free-fall function duration setting register (R/W)

**Table 124. FREE_FALL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FF_DUR4 | FF_DUR3 | FF_DUR2 | FF_DUR1 | FF_DUR0 | FF_THS2 | FF_THS1 | FF_THS0 |

**Table 125. FREE_FALL register description**

| | |
|---|---|
| FF_DUR[4:0] | Free-fall duration event. Default: 0<br>For the complete configuration of the free fall duration, refer to FF_DUR5 in WAKE_UP_DUR (5Ch) configuration |
| FF_THS[2:0] | Free-fall threshold setting<br>(000: 156 mg (default);<br>001: 219 mg;<br>010: 250 mg;<br>011: 312 mg;<br>100: 344 mg;<br>101: 406 mg;<br>110: 469 mg;<br>111: 500 mg) |

## 9.47 MD1_CFG (5Eh)

Functions routing to INT1 pin register (R/W)

**Table 126. MD1_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT1_SLEEP_CHANGE | 0(1) | INT1_WU | INT1_FF | 0(1) | INT1_6D | INT1_EMB_FUNC | INT1_SHUB |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 127. MD1_CFG register description**

| | |
|---|---|
| INT1_SLEEP_CHANGE(1) | Routing activity/inactivity recognition event to INT1. Default: 0<br>(0: routing activity/inactivity event to INT1 disabled;<br>1: routing activity/inactivity event to INT1 enabled) |
| INT1_WU | Routing wake-up event to INT1. Default value: 0<br>(0: routing wake-up event to INT1 disabled;<br>1: routing wake-up event to INT1 enabled) |
| INT1_FF | Routing free-fall event to INT1. Default value: 0<br>(0: routing free-fall event to INT1 disabled;<br>1: routing free-fall event to INT1 enabled) |
| INT1_6D | Routing 6D event to INT1. Default value: 0<br>(0: routing 6D event to INT1 disabled;<br>1: routing 6D event to INT1 enabled) |
| INT1_EMB_FUNC | Routing embedded functions event to INT1. Default value: 0<br>(0: routing embedded functions event to INT1 disabled;<br>1: routing embedded functions event to INT1 enabled) |
| INT1_SHUB | Routing sensor hub communication concluded event to INT1. Default value: 0<br>(0: routing sensor hub communication concluded event to INT1 disabled;<br>1: routing sensor hub communication concluded event to INT1 enabled) |

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INT_CFG0 (56h) register.*

## 9.48 MD2_CFG (5Fh)

Functions routing to INT2 pin register (R/W)

**Table 128. MD2_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_SLEEP_CHANGE | 0(1) | INT2_WU | INT2_FF | 0(1) | INT2_6D | INT2_EMB_FUNC | INT2_TIMESTAMP |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 129. MD2_CFG register description**

| | |
|---|---|
| INT2_SLEEP_CHANGE(1) | Routing activity/inactivity recognition event to INT2. Default: 0<br>(0: routing activity/inactivity event to INT2 disabled;<br>1: routing activity/inactivity event to INT2 enabled) |
| INT2_WU | Routing wake-up event to INT2. Default value: 0<br>(0: routing wake-up event to INT2 disabled;<br>1: routing wake-up event to INT2 enabled) |
| INT2_FF | Routing free-fall event to INT2. Default value: 0<br>(0: routing free-fall event to INT2 disabled;<br>1: routing free-fall event to INT2 enabled) |
| INT2_6D | Routing 6D event to INT2. Default value: 0<br>(0: routing 6D event to INT2 disabled;<br>1: routing 6D event to INT2 enabled) |
| INT2_EMB_FUNC | Routing embedded functions event to INT2. Default value: 0<br>(0: routing embedded functions event to INT2 disabled;<br>1: routing embedded functions event to INT2 enabled) |
| INT2_TIMESTAMP | Enables routing the alert for timestamp overflow within 6.4 ms to the INT2 pin. |

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INT_CFG0 (56h) register.*

## 9.49 I3C_BUS_AVB (62h)

I3C_BUS_AVB register (R/W)

**Table 130. I3C_BUS_AVB register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | I3C_Bus_ Avb_Sel1 | I3C_Bus_ Avb_Sel0 | 0(1) | 0(1) | PD_DIS_ INT1 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 131. I3C_BUS_AVB register description**

| | |
|---|---|
| I3C_Bus_Avb_Sel[1:0] | These bits are used to select the bus available time when I3C IBI is used.<br>Default value: 00<br>(00: bus available time equal to 50 µs (default);<br>01: bus available time equal to 2 µs;<br>10: bus available time equal to 1 ms;<br>11: bus available time equal to 25 ms) |
| PD_DIS_INT1 | This bit allows disabling the INT1 pull-down.<br>(0: pull-down on INT1 enabled (pull-down is effectively connected only when no interrupts are routed to the INT1 pin or when the I3C dynamic address is assigned);<br>1: pull-down on INT1 disabled (pull-down not connected)) |

*Note: The IBI (in-band interrupt) is continuously generated (each time a bus available condition is satisfied) until an interrupt is served. The master should execute the interrupt service routine (ISR) at a time lower than the configured bus available time, otherwise the master should disable the interrupt (I3C DISEC in order to disable the interrupt request) at a time lower than the bus available time.*

*If the master needs more time to analyze and start the correct ISR, then the master can change the bus available time from 50 µs (default) to a higher time.*

## 9.50 INTERNAL_FREQ_FINE (63h)

Internal frequency register (R)

**Table 132. INTERNAL_FREQ_FINE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FREQ_FINE7 | FREQ_FINE6 | FREQ_FINE5 | FREQ_FINE4 | FREQ_FINE3 | FREQ_FINE2 | FREQ_FINE1 | FREQ_FINE0 |

**Table 133. INTERNAL_FREQ_FINE register description**

| | |
|---|---|
| FREQ_FINE[7:0] | Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.15%. 8-bit format, two's complement. |

The formula below can be used to calculate a better estimation of the actual ODR:
ODR_Actual = (6667 + ((0.0015 * INTERNAL_FREQ_FINE) * 6667)) / ODR_Coeff

| Selected_ODR | ODR_Coeff |
|---|---|
| 12.5 | 512 |
| 26 | 256 |
| 52 | 128 |
| 104 | 64 |
| 208 | 32 |
| 416 | 16 |
| 833 | 8 |
| 1667 | 4 |
| 3333 | 2 |
| 6667 | 1 |

The Selected_ODR parameter has to be derived from the ODR_XL selection (Table 43. CTRL1_XL register description) in order to estimate the accelerometer ODR and from the ODR_G selection (Table 46. CTRL2_G register description) in order to estimate the gyroscope ODR.

## 9.51 X_OFS_USR (73h)

Accelerometer X-axis user offset correction (R/W). The offset value set in the X_OFS_USR offset register is internally subtracted from the acceleration value measured on the X-axis.

**Table 134. X_OFS_USR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X_OFS_USR_7 | X_OFS_USR_6 | X_OFS_USR_5 | X_OFS_USR_4 | X_OFS_USR_3 | X_OFS_USR_2 | X_OFS_USR_1 | X_OFS_USR_0 |

**Table 135. X_OFS_USR register description**

| | |
|---|---|
| X_OFS_USR_[7:0] | Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127 127]. |

## 9.52 Y_OFS_USR (74h)

Accelerometer Y-axis user offset correction (R/W). The offset value set in the Y_OFS_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

**Table 136. Y_OFS_USR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Y_OFS_USR_7 | Y_OFS_USR_6 | Y_OFS_USR_5 | Y_OFS_USR_4 | Y_OFS_USR_3 | Y_OFS_USR_2 | Y_OFS_USR_1 | Y_OFS_USR_0 |

| | |
|---|---|
| Y_OFS_USR_[7:0] | Accelerometer Y-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127]. |

## 9.53 Z_OFS_USR (75h)

Accelerometer Z-axis user offset correction (R/W). The offset value set in the Z_OFS_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

**Table 137. Z_OFS_USR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Z_OFS_USR_7 | Z_OFS_USR_6 | Z_OFS_USR_5 | Z_OFS_USR_4 | Z_OFS_USR_3 | Z_OFS_USR_2 | Z_OFS_USR_1 | Z_OFS_USR_0 |

**Table 138. Z_OFS_USR register description**

| | |
|---|---|
| Z_OFS_USR_[7:0] | Accelerometer Z-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127]. |

## 9.54 FIFO_DATA_OUT_TAG (78h)

FIFO tag register (R)

**Table 139. FIFO_DATA_OUT_TAG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TAG_ SENSOR_4 | TAG_ SENSOR_3 | TAG_ SENSOR_2 | TAG_ SENSOR_1 | TAG_ SENSOR_0 | TAG_CNT_1 | TAG_CNT_0 | TAG_ PARITY |

**Table 140. FIFO_DATA_OUT_TAG register description**

| | |
|---|---|
| TAG_SENSOR_[4:0] | Identifies the sensor in:<br>FIFO_DATA_OUT_X_H (7Ah) and FIFO_DATA_OUT_X_L (79h), FIFO_DATA_OUT_Y_H (7Ch) and FIFO_DATA_OUT_Y_L (7Bh), and FIFO_DATA_OUT_Z_H (7Eh) and FIFO_DATA_OUT_Z_L (7Dh) |
| TAG_CNT_[1:0] | 2-bit counter which identifies sensor time slot |
| TAG_PARITY | Parity check of TAG content |

**Table 141. FIFO tag**

| TAG_SENSOR_[4:0] | Sensor name |
|---|---|
| 0x01 | Gyroscope |
| 0x02 | Accelerometer |
| 0x03 | Temperature |
| 0x04 | Timestamp |
| 0x05 | CFG_Change |
| 0x0E | Sensor hub slave 0 |
| 0x0F | Sensor hub slave 1 |
| 0x10 | Sensor hub slave 2 |
| 0x11 | Sensor hub slave 3 |
| 0x19 | Sensor hub nack |

## 9.55 FIFO_DATA_OUT_X_H (7Ah) and FIFO_DATA_OUT_X_L (79h)

FIFO data output X (R)

**Table 142. FIFO_DATA_OUT_X_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 143. FIFO_DATA_OUT_X_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 144. FIFO_DATA_OUT_X_H, FIFO_DATA_OUT_X_L register description**

| | |
|---|---|
| D[15:0] | FIFO X-axis output |

## 9.56 FIFO_DATA_OUT_Y_H (7Ch) and FIFO_DATA_OUT_Y_L (7Bh)

FIFO data output Y (R)

**Table 145. FIFO_DATA_OUT_Y_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 146. FIFO_DATA_OUT_Y_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 147. FIFO_DATA_OUT_Y_H, FIFO_DATA_OUT_Y_L register description**

| | |
|---|---|
| D[15:0] | FIFO Y-axis output |

## 9.57 FIFO_DATA_OUT_Z_H (7Eh) and FIFO_DATA_OUT_Z_L (7Dh)

FIFO data output Z (R)

**Table 148. FIFO_DATA_OUT_Z_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 149. FIFO_DATA_OUT_Z_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 150. FIFO_DATA_OUT_Z_H, FIFO_DATA_OUT_Z_L register description**

| | |
|---|---|
| D[15:0] | FIFO Z-axis output |

# 10 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when FUNC_CFG_EN is set to 1 in FUNC_CFG_ACCESS (01h).

**Table 151. Register address map - embedded functions**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| PAGE_SEL | R/W | 02 | 00000010 | 00000001 | |
| RESERVED | - | 03-04 | | | Reserved |
| EMB_FUNC_EN_B | R/W | 05 | 00000101 | 00000000 | |
| PAGE_ADDRESS | R/W | 08 | 00001000 | 00000000 | |
| PAGE_VALUE | R/W | 09 | 00001001 | 00000000 | |
| EMB_FUNC_INT1 | R/W | 0A | 00001010 | 00000000 | |
| FSM_INT1_A | R/W | 0B | 00001011 | 00000000 | |
| FSM_INT1_B | R/W | 0C | 00001100 | 00000000 | |
| MLC_INT1 | R/W | 0D | 00001101 | 00000000 | |
| EMB_FUNC_INT2 | R/W | 0E | 00001110 | 00000000 | |
| FSM_INT2_A | R | 0F | 00001111 | 01101011 | |
| FSM_INT2_B | R/W | 10 | 00010000 | 00000000 | |
| MLC_INT2 | R/W | 11 | 00010001 | 00000000 | |
| EMB_FUNC_STATUS | R | 12 | 00010010 | output | |
| FSM_STATUS_A | R | 13 | 00010011 | output | |
| FSM_STATUS_B | R | 14 | 00010100 | output | |
| MLC_STATUS | R | 15 | 00010101 | output | |
| PAGE_RW | R/W | 17 | 00010111 | 00000000 | |
| RESERVED | - | 18-45 | | | Reserved |
| FSM_ENABLE_A | R/W | 46 | 01000110 | 00000000 | |
| FSM_ENABLE_B | R/W | 47 | 01000111 | 00000000 | |
| FSM_LONG_COUNTER_L | R/W | 48 | 01001000 | 00000000 | |
| FSM_LONG_COUNTER_H | R/W | 49 | 01001001 | 00000000 | |
| FSM_LONG_COUNTER_CLEAR | R/W | 4A | 01001010 | 00000000 | |
| FSM_OUTS1 | R | 4C | 01001100 | output | |
| FSM_OUTS2 | R | 4D | 01001101 | output | |
| FSM_OUTS3 | R | 4E | 01001110 | output | |
| FSM_OUTS4 | R | 4F | 01001111 | output | |
| FSM_OUTS5 | R | 50 | 01010000 | output | |
| FSM_OUTS6 | R | 51 | 01010001 | output | |
| FSM_OUTS7 | R | 52 | 01010010 | output | |
| FSM_OUTS8 | R | 53 | 01010011 | output | |
| FSM_OUTS9 | R | 54 | 01010100 | output | |
| FSM_OUTS10 | R | 55 | 01010101 | output | |

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| FSM_OUTS11 | R | 56 | 01010110 | output | |
| FSM_OUTS12 | R | 57 | 01010111 | output | |
| FSM_OUTS13 | R | 58 | 01011000 | output | |
| FSM_OUTS14 | R | 59 | 01011001 | output | |
| FSM_OUTS15 | R | 5A | 01011010 | output | |
| FSM_OUTS16 | R | 5B | 01011011 | output | |
| RESERVED | - | 5C-5E | | | Reserved |
| EMB_FUNC_ODR_CFG_B | R/W | 5F | 01011111 | 01001011 | |
| EMB_FUNC_ODR_CFG_C | R/W | 60 | 01100000 | 00010101 | |
| RESERVED | - | 61-66 | | | Reserved |
| EMB_FUNC_INIT_B | R/W | 67 | 01100111 | 00000000 | |
| MLC0_SRC | R | 70 | 01110000 | output | |
| MLC1_SRC | R | 71 | 01110001 | output | |
| MLC2_SRC | R | 72 | 01110010 | output | |
| MLC3_SRC | R | 73 | 01110011 | output | |
| MLC4_SRC | R | 74 | 01110100 | output | |
| MLC5_SRC | R | 75 | 01110101 | output | |
| MLC6_SRC | R | 76 | 01110110 | output | |
| MLC7_SRC | R | 77 | 01110111 | output | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 11 Embedded functions register description

## 11.1 PAGE_SEL (02h)

Enable advanced features dedicated page (R/W)

**Table 152. PAGE_SEL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PAGE_SEL3 | PAGE_SEL2 | PAGE_SEL1 | PAGE_SEL0 | 0(1) | 0(1) | EMB_FUNC_CLK_DIS | 1(2) |

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

**Table 153. PAGE_SEL register description**

| | |
|---|---|
| PAGE_SEL[3:0] | Selects the advanced features dedicated page. Default value: 0000 |
| EMB_FUNC_CLK_DIS | Disables the embedded functions clock. Default value: 0<br>(0: clock enabled; 1: clock disabled) |

## 11.2 EMB_FUNC_EN_B (05h)

Enable embedded functions register (R/W)

**Table 154. EMB_FUNC_EN_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | MLC_EN | 0(1) | 0(1) | 0(1) | FSM_EN |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 155. EMB_FUNC_EN_B register description**

| | |
|---|---|
| MLC_EN | Enables machine learning core feature. Default value: 0<br>(0: machine learning core feature disabled;<br>1: machine learning core feature enabled) |
| FSM_EN | Enables finite state machine (FSM) feature. Default value: 0<br>(0: FSM feature disabled; 1: FSM feature enabled) |

## 11.3 PAGE_ADDRESS (08h)

Page address register (R/W)

**Table 156. PAGE_ADDRESS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PAGE_ADDR7 | PAGE_ADDR6 | PAGE_ADDR5 | PAGE_ADDR4 | PAGE_ADDR3 | PAGE_ADDR2 | PAGE_ADDR1 | PAGE_ADDR0 |

**Table 157. PAGE_ADDRESS register description**

| | |
|---|---|
| PAGE_ADDR[7:0] | After setting the bit PAGE_WRITE / PAGE_READ in register PAGE_RW (17h), this register is used to set the address of the register to be written/read in the advanced features page selected through the bits PAGE_SEL[3:0] in register PAGE_SEL (02h). |

## 11.4 PAGE_VALUE (09h)

Page value register (R/W)

**Table 158. PAGE_VALUE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PAGE_ VALUE7 | PAGE_ VALUE6 | PAGE_ VALUE5 | PAGE_ VALUE4 | PAGE_ VALUE3 | PAGE_ VALUE2 | PAGE_ VALUE1 | PAGE_ VALUE0 |

**Table 159. PAGE_VALUE register description**

| | |
|---|---|
| PAGE_VALUE[7:0] | These bits are used to write (if the bit PAGE_WRITE = 1 in register PAGE_RW (17h)) or read (if the bit PAGE_READ = 1 in register PAGE_RW (17h)) the data at the address PAGE_ADDR[7:0] of the selected advanced features page. |

## 11.5 EMB_FUNC_INT1 (0Ah)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 160. EMB_FUNC_INT1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT1_ FSM_LC | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 161. EMB_FUNC_INT1 register description**

| | |
|---|---|
| INT1_FSM_LC(1) | Routing FSM long counter timeout interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |

1. *This bit is activated if the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

## 11.6 FSM_INT1_A (0Bh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 162. FSM_INT1_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT1_FSM8 | INT1_FSM7 | INT1_FSM6 | INT1_FSM5 | INT1_FSM4 | INT1_FSM3 | INT1_FSM2 | INT1_FSM1 |

**Table 163. FSM_INT1_A register description**

| | |
|---|---|
| INT1_FSM8(1) | Routing FSM8 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM7(1) | Routing FSM7 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM6(1) | Routing FSM6 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM5(1) | Routing FSM5 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM4(1) | Routing FSM4 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM3(1) | Routing FSM3 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing INT1 enabled) |
| INT1_FSM2(1) | Routing FSM2 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM1(1) | Routing FSM1 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |

1. *This bit is activated if the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

## 11.7 FSM_INT1_B (0Ch)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 164. FSM_INT1_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT1_FSM16 | INT1_FSM15 | INT1_FSM14 | INT1_FSM13 | INT1_FSM12 | INT1_FSM11 | INT1_FSM10 | INT1_FSM9 |

**Table 165. FSM_INT1_B register description**

| | |
|---|---|
| INT1_FSM16(1) | Routing FSM16 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM15(1) | Routing FSM15 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM14(1) | Routing FSM14 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM13(1) | Routing FSM13 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM12(1) | Routing FSM12 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM11(1) | Routing FSM11 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM10(1) | Routing FSM10 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM9(1) | Routing FSM9 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |

1. *This bit is activated if the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

## 11.8 MLC_INT1 (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 166. MLC_INT1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT1_MLC8 | INT1_MLC7 | INT1_MLC6 | INT1_MLC5 | INT1_MLC4 | INT1_MLC3 | INT1_MLC2 | INT1_MLC1 |

**Table 167. MLC_INT1 register description**

| | |
|---|---|
| INT1_MLC8 | Routing MLC8 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_MLC7 | Routing MLC7 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_MLC6 | Routing MLC6 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_MLC5 | Routing MLC5 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_MLC4 | Routing MLC4 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_MLC3 | Routing MLC3 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_MLC2 | Routing MLC2 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_MLC1 | Routing MLC1 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |

## 11.9 EMB_FUNC_INT2 (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 168. EMB_FUNC_INT2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_ FSM_LC | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 169. EMB_FUNC_INT2 register description**

| | |
|---|---|
| INT2_FSM_LC(1) | Routing FSM long counter timeout interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |

1. *This bit is activated if the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

## 11.10 FSM_INT2_A (0Fh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 170. FSM_INT2_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_FSM8 | INT2_FSM7 | INT2_FSM6 | INT2_FSM5 | INT2_FSM4 | INT2_FSM3 | INT2_FSM2 | INT2_FSM1 |

**Table 171. FSM_INT2_A register description**

| | |
|---|---|
| INT2_FSM8(1) | Routing FSM8 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM7(1) | Routing FSM7 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM6(1) | Routing FSM6 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM5(1) | Routing FSM5 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM4(1) | Routing FSM4 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM3(1) | Routing FSM3 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled)<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT2_FSM2(1) | Routing FSM2 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM1(1) | Routing FSM1 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |

1. *This bit is activated if the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

## 11.11 FSM_INT2_B (10h)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 172. FSM_INT2_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_FSM16 | INT2_FSM15 | INT2_FSM14 | INT2_FSM13 | INT2_FSM12 | INT2_FSM11 | INT2_FSM10 | INT2_FSM9 |

**Table 173. FSM_INT2_B register description**

| | |
|---|---|
| INT2_FSM16(1) | Routing FSM16 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM15(1) | Routing FSM15 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM14(1) | Routing FSM14 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM13(1) | Routing FSM13 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM12(1) | Routing FSM12 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM11(1) | Routing FSM11 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM10(1) | Routing FSM10 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM9(1) | Routing FSM9 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |

1. *This bit is activated if the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

## 11.12 MLC_INT2 (11h)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 174. MLC_INT2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_MLC8 | INT2_MLC7 | INT2_MLC6 | INT2_MLC5 | INT2_MLC4 | INT2_MLC3 | INT2_MLC2 | INT2_MLC1 |

**Table 175. MLC_INT2 register description**

| | |
|---|---|
| INT2_MLC8 | Routing MLC8 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_MLC7 | Routing MLC7 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_MLC6 | Routing MLC6 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_MLC5 | Routing MLC5 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_MLC4 | Routing MLC4 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_MLC3 | Routing MLC3 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_MLC2 | Routing MLC2 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_MLC1 | Routing MLC1 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |

## 11.13 EMB_FUNC_STATUS (12h)

Embedded function status register (R)

**Table 176. EMB_FUNC_STATUS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM_LC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 177. EMB_FUNC_STATUS register description**

| | |
|---|---|
| IS_FSM_LC | Interrupt status bit for FSM long counter timeout interrupt event.<br>(1: interrupt detected; 0: no interrupt) |

## 11.14 FSM_STATUS_A (13h)

Finite state machine status register (R)

**Table 178. FSM_STATUS_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM8 | IS_FSM7 | IS_FSM6 | IS_FSM5 | IS_FSM4 | IS_FSM3 | IS_FSM2 | IS_FSM1 |

**Table 179. FSM_STATUS_A register description**

| | |
|---|---|
| IS_FSM8 | Interrupt status bit for FSM8 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM7 | Interrupt status bit for FSM7 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM6 | Interrupt status bit for FSM6 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM5 | Interrupt status bit for FSM5 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM4 | Interrupt status bit for FSM4 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM3 | Interrupt status bit for FSM3 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM2 | Interrupt status bit for FSM2 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM1 | Interrupt status bit for FSM1 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |

## 11.15 FSM_STATUS_B (14h)

Finite state machine status register (R)

**Table 180. FSM_STATUS_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM16 | IS_FSM15 | IS_FSM14 | IS_FSM13 | IS_FSM12 | IS_FSM11 | IS_FSM10 | IS_FSM9 |

**Table 181. FSM_STATUS_B register description**

| | |
|---|---|
| IS_FSM16 | Interrupt status bit for FSM16 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM15 | Interrupt status bit for FSM15 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM14 | Interrupt status bit for FSM14 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM13 | Interrupt status bit for FSM13 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM12 | Interrupt status bit for FSM12 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM11 | Interrupt status bit for FSM11 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM10 | Interrupt status bit for FSM10 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_FSM9 | Interrupt status bit for FSM9 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |

## 11.16 MLC_STATUS (15h)

Machine learning core status register (R)

**Table 182. MLC_STATUS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_MLC8 | IS_MLC7 | IS_MLC6 | IS_MLC5 | IS_MLC4 | IS_MLC3 | IS_MLC2 | IS_MLC1 |

**Table 183. MLC_STATUS register description**

| | |
|---|---|
| IS_MLC8 | Interrupt status bit for MLC8 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC7 | Interrupt status bit for MLC7 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC6 | Interrupt status bit for MLC6 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC5 | Interrupt status bit for MLC5 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC4 | Interrupt status bit for MLC4 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC3 | Interrupt status bit for MLC3 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC2 | Interrupt status bit for MLC2 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_MLC1 | Interrupt status bit for MLC1 interrupt event.<br>(1: interrupt detected; 0: no interrupt) |

## 11.17 PAGE_RW (17h)

Enable read and write mode of advanced features dedicated page (R/W)

**Table 184. PAGE_RW register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EMB_ FUNC_LIR | PAGE_ WRITE | PAGE_ READ | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 185. PAGE_RW register description**

| | |
|---|---|
| EMB_FUNC_LIR | Latched interrupt mode for embedded functions. Default value: 0<br>(0: embedded functions interrupt request not latched;<br>1: embedded functions interrupt request latched) |
| PAGE_WRITE | Enables writes to the selected advanced features dedicated page.(1) Default value: 0<br>(1: enable; 0: disable) |
| PAGE_READ | Enables reads from the selected advanced features dedicated page.(1) Default value: 0<br>(1: enable; 0: disable) |

1. *Page selected by PAGE_SEL[3:0] in PAGE_SEL (02h) register.*

## 11.18 FSM_ENABLE_A (46h)

Enable FSM register (R/W)

**Table 186. FSM_ENABLE_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM8_EN | FSM7_EN | FSM6_EN | FSM5_EN | FSM4_EN | FSM3_EN | FSM2_EN | FSM1_EN |

**Table 187. FSM_ENABLE_A register description**

| | |
|---|---|
| FSM8_EN | Enables FSM8. Default value: 0 (0: FSM8 disabled; 1: FSM8 enabled) |
| FSM7_EN | Enables FSM7. Default value: 0 (0: FSM7 disabled; 1: FSM7 enabled) |
| FSM6_EN | Enables FSM6. Default value: 0 (0: FSM6 disabled; 1: FSM6 enabled) |
| FSM5_EN | Enables FSM5. Default value: 0 (0: FSM5 disabled; 1: FSM5 enabled) |
| FSM4_EN | Enables FSM4. Default value: 0 (0: FSM4 disabled; 1: FSM4 enabled) |
| FSM3_EN | Enables FSM3. Default value: 0 (0: FSM3 disabled; 1: FSM3 enabled) |
| FSM2_EN | Enables FSM2. Default value: 0 (0: FSM2 disabled; 1: FSM2 enabled) |
| FSM1_EN | Enables FSM1. Default value: 0 (0: FSM1 disabled; 1: FSM1 enabled) |

## 11.19 FSM_ENABLE_B (47h)

Enable FSM register (R/W)

**Table 188. FSM_ENABLE_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM16_EN | FSM15_EN | FSM14_EN | FSM13_EN | FSM12_EN | FSM11_EN | FSM10_EN | FSM9_EN |

**Table 189. FSM_ENABLE_B register description**

| | |
|---|---|
| FSM16_EN | Enables FSM16. Default value: 0 (0: FSM16 disabled; 1: FSM16 enabled) |
| FSM15_EN | Enables FSM15. Default value: 0 (0: FSM15 disabled; 1: FSM15 enabled) |
| FSM14_EN | Enables FSM14. Default value: 0 (0: FSM14 disabled; 1: FSM14 enabled) |
| FSM13_EN | Enables FSM13. Default value: 0 (0: FSM13 disabled; 1: FSM13 enabled) |
| FSM12_EN | Enables FSM12. Default value: 0 (0: FSM12 disabled; 1: FSM12 enabled) |
| FSM11_EN | Enables FSM11. Default value: 0 (0: FSM11 disabled; 1: FSM11 enabled) |
| FSM10_EN | Enables FSM10. Default value: 0 (0: FSM10 disabled; 1: FSM10 enabled) |
| FSM9_EN | Enables FSM9. Default value: 0 (0: FSM9 disabled; 1: FSM9 enabled) |

## 11.20 FSM_LONG_COUNTER_L (48h) and FSM_LONG_COUNTER_H (49h)

FSM long counter status register (R/W)

Long counter value is an unsigned integer value (16-bit format); this value can be reset using the LC_CLEAR bit in FSM_LONG_COUNTER_CLEAR (4Ah) register.

**Table 190. FSM_LONG_COUNTER_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_LC_7 | FSM_LC_6 | FSM_LC_5 | FSM_LC_4 | FSM_LC_3 | FSM_LC_2 | FSM_LC_1 | FSM_LC_0 |

**Table 191. FSM_LONG_COUNTER_L register description**

| | |
|---|---|
| FSM_LC_[7:0] | Long counter current value (LSbyte). Default value: 00000000 |

**Table 192. FSM_LONG_COUNTER_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_LC_15 | FSM_LC_14 | FSM_LC_13 | FSM_LC_12 | FSM_LC_11 | FSM_LC_10 | FSM_LC_9 | FSM_LC_8 |

**Table 193. FSM_LONG_COUNTER_H register description**

| | |
|---|---|
| FSM_LC_[15:8] | Long counter current value (MSbyte). Default value: 00000000 |

## 11.21 FSM_LONG_COUNTER_CLEAR (4Ah)

FSM long counter reset register (R/W)

**Table 194. FSM_LONG_COUNTER_CLEAR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | FSM_LC_ CLEARED | FSM_LC_ CLEAR |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 195. FSM_LONG_COUNTER_CLEAR register description**

| | |
|---|---|
| FSM_LC_CLEARED | This read-only bit is automatically set to 1 when the long counter reset is done. Default value: 0 |
| FSM_LC_CLEAR | Clear FSM long counter value. Default value: 0 |

## 11.22 FSM_OUTS1 (4Ch)

FSM1 output register (R)

**Table 196. FSM_OUTS1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 197. FSM_OUTS1 register description**

| | |
|---|---|
| P_X | FSM1 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM1 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM1 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM1 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM1 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM1 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM1 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM1 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.23 FSM_OUTS2 (4Dh)

FSM2 output register (R)

**Table 198. FSM_OUTS2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 199. FSM_OUTS2 register description**

| | |
|---|---|
| P_X | FSM2 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM2 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM2 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM2 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM2 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM2 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM2 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM2 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.24 FSM_OUTS3 (4Eh)

FSM3 output register (R)

**Table 200. FSM_OUTS3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 201. FSM_OUTS3 register description**

| | |
|---|---|
| P_X | FSM3 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM3 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM3 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM3 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM3 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM3 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM3 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM3 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.25 FSM_OUTS4 (4Fh)

FSM4 output register (R)

**Table 202. FSM_OUTS4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 203. FSM_OUTS4 register description**

| | |
|---|---|
| P_X | FSM4 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM4 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM4 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM4 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM4 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM4 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM4 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM4 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.26 FSM_OUTS5 (50h)

FSM5 output register (R)

**Table 204. FSM_OUTS5 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 205. FSM_OUTS5 register description**

| | |
|---|---|
| P_X | FSM5 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM5 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM5 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM5 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM5 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM5 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM5 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM5 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.27 FSM_OUTS6 (51h)

FSM6 output register (R)

**Table 206. FSM_OUTS6 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 207. FSM_OUTS6 register description**

| | |
|---|---|
| P_X | FSM6 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM6 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM6 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM6 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM6 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM6 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM6 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM6 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.28 FSM_OUTS7 (52h)

FSM7 output register (R)

**Table 208. FSM_OUTS7 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 209. FSM_OUTS7 register description**

| | |
|---|---|
| P_X | FSM7 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM7 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM7 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM7 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM7 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM7 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM7 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM7 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.29 FSM_OUTS8 (53h)

FSM8 output register (R)

**Table 210. FSM_OUTS8 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 211. FSM_OUTS8 register description**

| | |
|---|---|
| P_X | FSM8 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM8 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM8 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM8 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM8 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM8 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM8 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM8 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.30 FSM_OUTS9 (54h)

FSM9 output register (R)

**Table 212. FSM_OUTS9 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 213. FSM_OUTS9 register description**

| | |
|---|---|
| P_X | FSM9 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM9 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM9 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM9 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM9 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM9 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM9 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM9 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.31 FSM_OUTS10 (55h)

FSM10 output register (R)

**Table 214. FSM_OUTS10 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 215. FSM_OUTS10 register description**

| | |
|---|---|
| P_X | FSM10 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM10 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM10 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM10 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM10 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM10 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM10 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM10 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.32 FSM_OUTS11 (56h)

FSM11 output register (R)

**Table 216. FSM_OUTS11 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 217. FSM_OUTS11 register description**

| | |
|---|---|
| P_X | FSM11 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM11 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM11 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM11 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM11 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM11 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM11 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM11 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.33 FSM_OUTS12 (57h)

FSM12 output register (R)

**Table 218. FSM_OUTS12 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 219. FSM_OUTS12 register description**

| | |
|---|---|
| P_X | FSM12 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM12 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM12 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM12 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM12 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM12 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM12 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM12 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.34 FSM_OUTS13 (58h)

FSM13 output register (R)

**Table 220. FSM_OUTS13 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 221. FSM_OUTS13 register description**

| | |
|---|---|
| P_X | FSM13 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM13 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM13 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM13 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM13 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM13 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM13 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM13 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.35 FSM_OUTS14 (59h)

FSM14 output register (R)

Table 222. **FSM_OUTS14 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

Table 223. **FSM_OUTS14 register description**

| | |
|---|---|
| P_X | FSM14 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM14 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM14 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM14 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM14 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM14 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM14 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM14 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.36 FSM_OUTS15 (5Ah)

FSM15 output register (R)

**Table 224. FSM_OUTS15 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 225. FSM_OUTS15 register description**

| | |
|---|---|
| P_X | FSM15 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM15 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM15 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM15 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM15 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM15 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM15 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM15 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.37 FSM_OUTS16 (5Bh)

FSM16 output register (R)

**Table 226. FSM_OUTS16 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 227. FSM_OUTS16 register description**

| | |
|---|---|
| P_X | FSM16 output: positive event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| N_X | FSM16 output: negative event detected on the X-axis.<br>(0: event not detected; 1: event detected) |
| P_Y | FSM16 output: positive event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| N_Y | FSM16 output: negative event detected on the Y-axis.<br>(0: event not detected; 1: event detected) |
| P_Z | FSM16 output: positive event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| N_Z | FSM16 output: negative event detected on the Z-axis.<br>(0: event not detected; 1: event detected) |
| P_V | FSM16 output: positive event detected on the vector.<br>(0: event not detected; 1: event detected) |
| N_V | FSM16 output: negative event detected on the vector.<br>(0: event not detected; 1: event detected) |

## 11.38 EMB_FUNC_ODR_CFG_B (5Fh)

Finite state machine output data rate configuration register (R/W)

**Table 228. EMB_FUNC_ODR_CFG_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 1(2) | 0(1) | FSM_ODR1 | FSM_ODR0 | 0(1) | 1(2) | 1(2) |

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device*

**Table 229. EMB_FUNC_ODR_CFG_B register description**

| | |
|---|---|
| FSM_ODR[1:0] | Finite state machine ODR configuration:<br>(00: 12.5 Hz;<br>01: 26 Hz (default);<br>10: 52 Hz;<br>11: 104 Hz) |

## 11.39 EMB_FUNC_ODR_CFG_C (60h)

Machine learning core output data rate configuration register (R/W)

**Table 230. EMB_FUNC_ODR_CFG_C register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | MLC_ODR1 | MLC_ODR0 | 0(1) | 1(2) | 0(1) | 1(2) |

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

**Table 231. EMB_FUNC_ODR_CFG_C register description**

| | |
|---|---|
| MLC_ODR[1:0] | Machine learning core ODR configuration:<br>(00: 12.5 Hz;<br>01: 26 Hz (default);<br>10: 52 Hz;<br>11: 104 Hz) |

## 11.40 EMB_FUNC_INIT_B (67h)

Embedded functions initialization register (R/W)

**Table 232. EMB_FUNC_INIT_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | MLC_INIT | 0(1) | 0(1) | 0(1) | FSM_INIT |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 233. EMB_FUNC_INIT_B register description**

| | |
|---|---|
| MLC_INIT | Machine learning core initialization request. Default value: 0 |
| FSM_INIT | Finite state machine initialization request. Default value: 0 |

## 11.41 MLC0_SRC (70h)

Machine learning core source register (R)

**Table 234. MLC0_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC0_SRC_7 | MLC0_SRC_6 | MLC0_SRC_5 | MLC0_SRC_4 | MLC0_SRC_3 | MLC0_SRC_2 | MLC0_SRC_1 | MLC0_SRC_0 |

**Table 235. MLC0_SRC register description**

| | |
|---|---|
| MLC0_SRC_[7:0] | Output value of MLC0 decision tree |

## 11.42 MLC1_SRC (71h)

Machine learning core source register (R)

Table 236. **MLC1_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC1_SRC_7 | MLC1_SRC_6 | MLC1_SRC_5 | MLC1_SRC_4 | MLC1_SRC_3 | MLC1_SRC_2 | MLC1_SRC_1 | MLC1_SRC_0 |

Table 237. **MLC1_SRC register description**

| | |
|---|---|
| MLC1_SRC_[7:0] | Output value of MLC1 decision tree |

## 11.43 MLC2_SRC (72h)

Machine learning core source register (R)

Table 238. **MLC2_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC2_SRC_7 | MLC2_SRC_6 | MLC2_SRC_5 | MLC2_SRC_4 | MLC2_SRC_3 | MLC2_SRC_2 | MLC2_SRC_1 | MLC2_SRC_0 |

Table 239. **MLC2_SRC register description**

| | |
|---|---|
| MLC2_SRC_[7:0] | Output value of MLC2 decision tree |

## 11.44 MLC3_SRC (73h)

Machine learning core source register (R)

Table 240. **MLC3_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC3_SRC_7 | MLC3_SRC_6 | MLC3_SRC_5 | MLC3_SRC_4 | MLC3_SRC_3 | MLC3_SRC_2 | MLC3_SRC_1 | MLC3_SRC_0 |

Table 241. **MLC3_SRC register description**

| | |
|---|---|
| MLC3_SRC_[7:0] | Output value of MLC3 decision tree |

## 11.45 MLC4_SRC (74h)

Machine learning core source register (R)

Table 242. **MLC4_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC4_SRC_7 | MLC4_SRC_6 | MLC4_SRC_5 | MLC4_SRC_4 | MLC4_SRC_3 | MLC4_SRC_2 | MLC4_SRC_1 | MLC4_SRC_0 |

Table 243. **MLC4_SRC register description**

| | |
|---|---|
| MLC4_SRC_[7:0] | Output value of MLC4 decision tree |

## 11.46 MLC5_SRC (75h)

Machine learning core source register (R)

**Table 244. MLC5_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC5_SRC_7 | MLC5_SRC_6 | MLC5_SRC_5 | MLC5_SRC_4 | MLC5_SRC_3 | MLC5_SRC_2 | MLC5_SRC_1 | MLC5_SRC_0 |

**Table 245. MLC5_SRC register description**

| | |
|---|---|
| MLC5_SRC_[7:0] | Output value of MLC5 decision tree |

## 11.47 MLC6_SRC (76h)

Machine learning core source register (R)

**Table 246. MLC6_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC6_SRC_7 | MLC6_SRC_6 | MLC6_SRC_5 | MLC6_SRC_4 | MLC6_SRC_3 | MLC6_SRC_2 | MLC6_SRC_1 | MLC6_SRC_0 |

**Table 247. MLC6_SRC register description**

| | |
|---|---|
| MLC6_SRC_[7:0] | Output value of MLC6 decision tree |

## 11.48 MLC7_SRC (77h)

Machine learning core source register (R)

**Table 248. MLC7_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC7_SRC_7 | MLC7_SRC_6 | MLC7_SRC_5 | MLC7_SRC_4 | MLC7_SRC_3 | MLC7_SRC_2 | MLC7_SRC_1 | MLC7_SRC_0 |

**Table 249. MLC7_SRC register description**

| | |
|---|---|
| MLC7_SRC_[7:0] | Output value of MLC7 decision tree |

# 12 Embedded advanced features

The following table provides a list of the registers for the embedded advanced features page 0. These registers are accessible when PAGE_SEL[3:0] are set to 0000 in PAGE_SEL (02h).

**Table 250. Register address map - embedded advanced features page 0**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| MAG_SENSITIVITY_L | R/W | BA | 10111010 | 00100100 | |
| MAG_SENSITIVITY_H | R/W | BB | 10111011 | 00010110 | |
| MAG_OFFX_L | R/W | C0 | 11000000 | 00000000 | |
| MAG_OFFX_H | R/W | C1 | 11000001 | 00000000 | |
| MAG_OFFY_L | R/W | C2 | 11000010 | 00000000 | |
| MAG_OFFY_H | R/W | C3 | 11000011 | 00000000 | |
| MAG_OFFZ_L | R/W | C4 | 11000100 | 00000000 | |
| MAG_OFFZ_H | R/W | C5 | 11000101 | 00000000 | |
| MAG_SI_XX_L | R/W | C6 | 11000110 | 00000000 | |
| MAG_SI_XX_H | R/W | C7 | 11000111 | 00111100 | |
| MAG_SI_XY_L | R/W | C8 | 11001000 | 00000000 | |
| MAG_SI_XY_H | R/W | C9 | 11001001 | 00000000 | |
| MAG_SI_XZ_L | R/W | CA | 11001010 | 00000000 | |
| MAG_SI_XZ_H | R/W | CB | 11001011 | 00000000 | |
| MAG_SI_YY_L | R/W | CC | 11001100 | 00000000 | |
| MAG_SI_YY_H | R/W | CD | 11001101 | 00111100 | |
| MAG_SI_YZ_L | R/W | CE | 11001110 | 00000000 | |
| MAG_SI_YZ_H | R/W | CF | 11001111 | 00000000 | |
| MAG_SI_ZZ_L | R/W | D0 | 11010000 | 00000000 | |
| MAG_SI_ZZ_H | R/W | D1 | 11010001 | 00111100 | |
| MAG_CFG_A | R/W | D4 | 11010100 | 00000101 | |
| MAG_CFG_B | R/W | D5 | 11010101 | 00000010 | |

The following table provides a list of the registers for the embedded advanced features page 1. These registers are accessible when PAGE_SEL[3:0] are set to 0001 in PAGE_SEL (02h).

**Table 251. Register address map - embedded advanced features page 1**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| FSM_LC_TIMEOUT_L | R/W | 7A | 01111010 | 00000000 | |
| FSM_LC_TIMEOUT_H | R/W | 7B | 01111011 | 00000000 | |
| FSM_PROGRAMS | R/W | 7C | 01111100 | 00000000 | |
| FSM_START_ADD_L | R/W | 7E | 01111110 | 00000000 | |
| FSM_START_ADD_H | R/W | 7F | 01111111 | 00000000 | |
| MLC_MAG_SENSITIVITY_L | R/W | E8 | 11101000 | 00000000 | |
| MLC_MAG_SENSITIVITY_H | R/W | E9 | 11101001 | 00111100 | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

**Write procedure example:**

Example: write value 01h in register at address 7Ch (FSM_PROGRAMS) in page 1

1. Write bit FUNC_CFG_EN = 1 in FUNC_CFG_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE_WRITE = 1 in PAGE_RW (17h) // Select write operation mode
3. Write 0001 in the PAGE_SEL[3:0] field of PAGE_SEL (02h) // Select page 1
4. Write 7Ch in PAGE_ADDRESS (08h) // Set address
5. Write 01h in PAGE_VALUE (09h) // Set value to be written
6. Write bit PAGE_WRITE = 0 in PAGE_RW (17h) // Write operation disabled
7. Write bit FUNC_CFG_EN = 0 in FUNC_CFG_ACCESS (01h) // Disable access to embedded functions registers

**Read procedure example:**

Example: read value of register at address 7Ch (FSM_PROGRAMS) in page 1

1. Write bit FUNC_CFG_EN = 1 in FUNC_CFG_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE_READ = 1 in PAGE_RW (17h) // Select read operation mode
3. Write 0001 in the PAGE_SEL[3:0] field of PAGE_SEL (02h) // Select page 1
4. Write 7Ch in PAGE_ADDRESS (08h) // Set address
5. Read value of PAGE_VALUE (09h) // Get register value
6. Write bit PAGE_READ = 0 in PAGE_RW (17h) // Read operation disabled
7. Write bit FUNC_CFG_EN = 0 in FUNC_CFG_ACCESS (01h) // Disable access to embedded functions registers

*Note: Steps 1 and 2 of both procedures are intended to be performed at the beginning of the procedure. Steps 6 and 7 of both procedures are intended to be performed at the end of the procedure. If the procedure involves multiple operations, only steps 3, 4 and 5 must be repeated for each operation. If, in particular, the multiple operations involve consecutive registers, only step 5 can be performed.*

# 13 Embedded advanced features register description

## 13.1 Page 0 - Embedded advanced features registers

### 13.1.1 MAG_SENSITIVITY_L (BAh) and MAG_SENSITIVITY_H (BBh)

External magnetometer sensitivity value register for the finite state machine (R/W)

This register corresponds to the LSB-to-gauss conversion value of the external magnetometer sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Default value of MAG_SENS[15:0] is 0x1624, corresponding to 0.0015 gauss/LSB.

**Table 252. MAG_SENSITIVITY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_ SENS_7 | MAG_ SENS_6 | MAG_ SENS_5 | MAG_ SENS_4 | MAG_ SENS_3 | MAG_ SENS_2 | MAG_ SENS_1 | MAG_ SENS_0 |

**Table 253. MAG_SENSITIVITY_L register description**

| | |
|---|---|
| MAG_SENS_[7:0] | External magnetometer sensitivity (LSbyte). Default value: 00100100 |

**Table 254. MAG_SENSITIVITY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_ SENS_15 | MAG_ SENS_14 | MAG_ SENS_13 | MAG_ SENS_12 | MAG_ SENS_11 | MAG_ SENS_10 | MAG_ SENS_9 | MAG_ SENS_8 |

**Table 255. MAG_SENSITIVITY_H register description**

| | |
|---|---|
| MAG_SENS_[15:8] | External magnetometer sensitivity (MSbyte). Default value: 00010110 |

### 13.1.2 MAG_OFFX_L (C0h) and MAG_OFFX_H (C1h)

Offset for X-axis hard-iron compensation register (R/W)
The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 256. MAG_OFFX_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_ OFFX_7 | MAG_ OFFX_6 | MAG_ OFFX_5 | MAG_ OFFX_4 | MAG_ OFFX_3 | MAG_ OFFX_2 | MAG_ OFFX_1 | MAG_ OFFX_0 |

**Table 257. MAG_OFFX_L register description**

| | |
|---|---|
| MAG_OFFX_[7:0] | Offset for X-axis hard-iron compensation (LSbyte). Default value: 00000000 |

**Table 258. MAG_OFFX_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_ OFFX_15 | MAG_ OFFX_14 | MAG_ OFFX_13 | MAG_ OFFX_12 | MAG_ OFFX_11 | MAG_ OFFX_10 | MAG_ OFFX_9 | MAG_ OFFX_8 |

**Table 259. MAG_OFFX_H register description**

| | |
|---|---|
| MAG_OFFX_[15:8] | Offset for X-axis hard-iron compensation (MSbyte). Default value: 00000000 |

### 13.1.3 MAG_OFFY_L (C2h) and MAG_OFFY_H (C3h)

Offset for Y-axis hard-iron compensation register (R/W)
The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 260. MAG_OFFY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_ OFFY_7 | MAG_ OFFY_6 | MAG_ OFFY_5 | MAG_ OFFY_4 | MAG_ OFFY_3 | MAG_ OFFY_2 | MAG_ OFFY_1 | MAG_ OFFY_0 |

**Table 261. MAG_OFFY_L register description**

| | |
|---|---|
| MAG_OFFY_[7:0] | Offset for Y-axis hard-iron compensation (LSbyte). Default value: 00000000 |

**Table 262. MAG_OFFY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_ OFFY_15 | MAG_ OFFY_14 | MAG_ OFFY_13 | MAG_ OFFY_12 | MAG_ OFFY_11 | MAG_ OFFY_10 | MAG_ OFFY_9 | MAG_ OFFY_8 |

**Table 263. MAG_OFFY_H register description**

| | |
|---|---|
| MAG_OFFY_[15:8] | Offset for Y-axis hard-iron compensation (MSbyte). Default value: 00000000 |

### 13.1.4 MAG_OFFZ_L (C4h) and MAG_OFFZ_H (C5h)

Offset for Z-axis hard-iron compensation register (R/W)
The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 264. MAG_OFFZ_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_ OFFZ_7 | MAG_ OFFZ_6 | MAG_ OFFZ_5 | MAG_ OFFZ_4 | MAG_ OFFZ_3 | MAG_ OFFZ_2 | MAG_ OFFZ_1 | MAG_ OFFZ_0 |

**Table 265. MAG_OFFZ_L register description**

| | |
|---|---|
| MAG_OFFZ_[7:0] | Offset for Z-axis hard-iron compensation (LSbyte). Default value: 00000000 |

**Table 266. MAG_OFFZ_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_ OFFZ_15 | MAG_ OFFZ_14 | MAG_ OFFZ_13 | MAG_ OFFZ_12 | MAG_ OFFZ_11 | MAG_ OFFZ_10 | MAG_ OFFZ_9 | MAG_ OFFZ_8 |

**Table 267. MAG_OFFZ_H register description**

| | |
|---|---|
| MAG_OFFZ_[15:8] | Offset for Z-axis hard-iron compensation (MSbyte). Default value: 00000000 |

### 13.1.5 MAG_SI_XX_L (C6h) and MAG_SI_XX_H (C7h)

Soft-iron (3x3 symmetric) matrix correction register (R/W)
The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 268. MAG_SI_XX_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_ XX_7 | MAG_SI_ XX_6 | MAG_SI_ XX_5 | MAG_SI_ XX_4 | MAG_SI_ XX_3 | MAG_SI_ XX_2 | MAG_SI_ XX_1 | MAG_SI_ XX_0 |

**Table 269. MAG_SI_XX_L register description**

| | |
|---|---|
| MAG_SI_XX_[7:0] | Soft-iron correction row1 col1 coefficient (LSbyte). Default value: 00000000 |

**Table 270. MAG_SI_XX_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_ XX_15 | MAG_SI_ XX_14 | MAG_SI_ XX_13 | MAG_SI_ XX_12 | MAG_SI_ XX_11 | MAG_SI_ XX_10 | MAG_SI_ XX_9 | MAG_SI_ XX_8 |

**Table 271. MAG_SI_XX_H register description**

| | |
|---|---|
| MAG_SI_XX_[15:8] | Soft-iron correction row1 col1 coefficient (MSbyte). Default value: 00111100 |

### 13.1.6 MAG_SI_XY_L (C8h) and MAG_SI_XY_H (C9h)

Soft-iron (3x3 symmetric) matrix correction register (R/W)
The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 272. MAG_SI_XY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_XY_7 | MAG_SI_XY_6 | MAG_SI_XY_5 | MAG_SI_XY_4 | MAG_SI_XY_3 | MAG_SI_XY_2 | MAG_SI_XY_1 | MAG_SI_XY_0 |

**Table 273. MAG_SI_XY_L register description**

| | |
|---|---|
| MAG_SI_XY_[7:0] | Soft-iron correction row1 col2 (and row2 col1) coefficient (LSbyte). Default value: 00000000 |

**Table 274. MAG_SI_XY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_XY_15 | MAG_SI_XY_14 | MAG_SI_XY_13 | MAG_SI_XY_12 | MAG_SI_XY_11 | MAG_SI_XY_10 | MAG_SI_XY_9 | MAG_SI_XY_8 |

**Table 275. MAG_SI_XY_H register description**

| | |
|---|---|
| MAG_SI_XY_[15:8] | Soft-iron correction row1 col2 (and row2 col1) coefficient (MSbyte). Default value: 00000000 |

### 13.1.7 MAG_SI_XZ_L (CAh) and MAG_SI_XZ_H (CBh)

Soft-iron (3x3 symmetric) matrix correction register (R/W)
The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 276. MAG_SI_XZ_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_XZ_7 | MAG_SI_XZ_6 | MAG_SI_XZ_5 | MAG_SI_XZ_4 | MAG_SI_XZ_3 | MAG_SI_XZ_2 | MAG_SI_XZ_1 | MAG_SI_XZ_0 |

**Table 277. MAG_SI_XZ_L register description**

| | |
|---|---|
| MAG_SI_XZ_[7:0] | Soft-iron correction row1 col3 (and row3 col1) coefficient (LSbyte). Default value: 00000000 |

**Table 278. MAG_SI_XZ_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_XZ_15 | MAG_SI_XZ_14 | MAG_SI_XZ_13 | MAG_SI_XZ_12 | MAG_SI_XZ_11 | MAG_SI_XZ_10 | MAG_SI_XZ_9 | MAG_SI_XZ_8 |

**Table 279. MAG_SI_XZ_H register description**

| | |
|---|---|
| MAG_SI_XZ_[15:8] | Soft-iron correction row1 col3 (and row3 col1) coefficient (MSbyte). Default value: 00000000 |

### 13.1.8 MAG_SI_YY_L (CCh) and MAG_SI_YY_H (CDh)

Soft-iron (3x3 symmetric) matrix correction register (R/W)
The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 280. MAG_SI_YY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_YY_7 | MAG_SI_YY_6 | MAG_SI_YY_5 | MAG_SI_YY_4 | MAG_SI_YY_3 | MAG_SI_YY_2 | MAG_SI_YY_1 | MAG_SI_YY_0 |

**Table 281. MAG_SI_YY_L register description**

| | |
|---|---|
| MAG_SI_YY_[7:0] | Soft-iron correction row2 col2 coefficient (LSbyte). Default value: 00000000 |

**Table 282. MAG_SI_YY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_YY_15 | MAG_SI_YY_14 | MAG_SI_YY_13 | MAG_SI_YY_12 | MAG_SI_YY_11 | MAG_SI_YY_10 | MAG_SI_YY_9 | MAG_SI_YY_8 |

**Table 283. MAG_SI_YY_H register description**

| | |
|---|---|
| MAG_SI_YY_[15:8] | Soft-iron correction row2 col2 coefficient (MSbyte). Default value: 00111100 |

### 13.1.9 MAG_SI_YZ_L (CEh) and MAG_SI_YZ_H (CFh)

Soft-iron (3x3 symmetric) matrix correction register (R/W)
The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 284. MAG_SI_YZ_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_YZ_7 | MAG_SI_YZ_6 | MAG_SI_YZ_5 | MAG_SI_YZ_4 | MAG_SI_YZ_3 | MAG_SI_YZ_2 | MAG_SI_YZ_1 | MAG_SI_YZ_0 |

**Table 285. MAG_SI_YZ_L register description**

| | |
|---|---|
| MAG_SI_YZ_[7:0] | Soft-iron correction row2 col3 (and row3 col2) coefficient (LSbyte). Default value: 00000000 |

**Table 286. MAG_SI_YZ_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_YZ_15 | MAG_SI_YZ_14 | MAG_SI_YZ_13 | MAG_SI_YZ_12 | MAG_SI_YZ_11 | MAG_SI_YZ_10 | MAG_SI_YZ_9 | MAG_SI_YZ_8 |

**Table 287. MAG_SI_YZ_H register description**

| | |
|---|---|
| MAG_SI_YZ_[15:8] | Soft-iron correction row2 col3 (and row3 col2) coefficient (MSbyte). Default value: 00000000 |

### 13.1.10 MAG_SI_ZZ_L (D0h) and MAG_SI_ZZ_H (D1h)

Soft-iron (3x3 symmetric) matrix correction register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 288. MAG_SI_ZZ_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_ZZ_7 | MAG_SI_ZZ_6 | MAG_SI_ZZ_5 | MAG_SI_ZZ_4 | MAG_SI_ZZ_3 | MAG_SI_ZZ_2 | MAG_SI_ZZ_1 | MAG_SI_ZZ_0 |

**Table 289. MAG_SI_ZZ_L register description**

| | |
|---|---|
| MAG_SI_ZZ_[7:0] | Soft-iron correction row3 col3 coefficient (LSbyte). Default value: 00000000 |

**Table 290. MAG_SI_ZZ_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MAG_SI_ZZ_15 | MAG_SI_ZZ_14 | MAG_SI_ZZ_13 | MAG_SI_ZZ_12 | MAG_SI_ZZ_11 | MAG_SI_ZZ_10 | MAG_SI_ZZ_9 | MAG_SI_ZZ_8 |

**Table 291. MAG_SI_ZZ_H register description**

| | |
|---|---|
| MAG_SI_ZZ_[15:8] | Soft-iron correction row3 col3 coefficient (MSbyte). Default value: 00111100 |

### 13.1.11 MAG_CFG_A (D4h)

External magnetometer coordinates (Z and Y axes) rotation register (R/W)

**Table 292. MAG_CFG_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | MAG_Y_ AXIS2 | MAG_Y_ AXIS1 | MAG_Y_ AXIS0 | 0(1) | MAG_Z_ AXIS2 | MAG_Z_ AXIS1 | MAG_Z_ AXIS0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 293. MAG_CFG_A register description**

| | |
|---|---|
| MAG_Y_AXIS[2:0] | Magnetometer Y-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: Y = Y; (default)<br>001: Y = -Y;<br>010: Y = X;<br>011: Y = -X;<br>100: Y = -Z;<br>101: Y = Z;<br>Others: Y = Y) |
| MAG_Z_AXIS[2:0] | Magnetometer Z-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: Z = Y;<br>001: Z = -Y;<br>010: Z = X;<br>011: Z = -X;<br>100: Z = -Z;<br>101: Z = Z; (default)<br>Others: Z = Y) |

### 13.1.12 MAG_CFG_B (D5h)

External magnetometer coordinates (X-axis) rotation register (R/W)

**Table 294. MAG_CFG_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | MAG_X_ AXIS2 | MAG_X_ AXIS1 | MAG_X_ AXIS0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 295. MAG_CFG_B register description**

| | |
|---|---|
| MAG_X_AXIS[2:0] | Magnetometer X-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: X = Y;<br>001: X = -Y;<br>010: X = X; (default)<br>011: X = -X;<br>100: X = -Z;<br>101: X = Z;<br>Others: X = Y) |

## 13.2 Page 1 - Embedded advanced features registers

### 13.2.1 FSM_LC_TIMEOUT_L (7Ah) and FSM_LC_TIMEOUT_H (7Bh)

FSM long counter timeout register (R/W)

The long counter timeout value is an unsigned integer value (16-bit format). When the long counter value reaches this value, the FSM generates an interrupt.

**Table 296. FSM_LC_TIMEOUT_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_LC_ TIMEOUT7 | FSM_LC_ TIMEOUT6 | FSM_LC_ TIMEOUT5 | FSM_LC_ TIMEOUT4 | FSM_LC_ TIMEOUT3 | FSM_LC_ TIMEOUT2 | FSM_LC_ TIMEOUT1 | FSM_LC_ TIMEOUT0 |

**Table 297. FSM_LC_TIMEOUT_L register description**

| | |
|---|---|
| FSM_LC_TIMEOUT[7:0] | FSM long counter timeout value (LSbyte). Default value: 00000000 |

**Table 298. FSM_LC_TIMEOUT_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_LC_ TIMEOUT15 | FSM_LC_ TIMEOUT14 | FSM_LC_ TIMEOUT13 | FSM_LC_ TIMEOUT12 | FSM_LC_ TIMEOUT11 | FSM_LC_ TIMEOUT10 | FSM_LC_ TIMEOUT9 | FSM_LC_ TIMEOUT8 |

**Table 299. FSM_LC_TIMEOUT_H register description**

| | |
|---|---|
| FSM_LC_TIMEOUT[15:8] | FSM long counter timeout value (MSbyte). Default value: 00000000 |

### 13.2.2 FSM_PROGRAMS (7Ch)

FSM number of programs register (R/W)

**Table 300. FSM_PROGRAMS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_N_ PROG7 | FSM_N_ PROG6 | FSM_N_ PROG5 | FSM_N_ PROG4 | FSM_N_ PROG3 | FSM_N_ PROG2 | FSM_N_ PROG1 | FSM_N_ PROG0 |

**Table 301. FSM_PROGRAMS register description**

| | |
|---|---|
| FSM_N_PROG[7:0] | Number of FSM programs; must be less than or equal to 16. Default value: 00000000 |

### 13.2.3 FSM_START_ADD_L (7Eh) and FSM_START_ADD_H (7Fh)

FSM start address register (R/W). First available address is 0x033C.

**Table 302. FSM_START_ADD_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_ START7 | FSM_ START6 | FSM_ START5 | FSM_ START4 | FSM_ START3 | FSM_ START2 | FSM_ START1 | FSM_ START0 |

**Table 303. FSM_START_ADD_L register description**

| | |
|---|---|
| FSM_START[7:0] | FSM start address value (LSbyte). Default value: 00000000 |

**Table 304. FSM_START_ADD_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_ START15 | FSM_ START14 | FSM_ START13 | FSM_ START12 | FSM_ START11 | FSM_ START10 | FSM_ START9 | FSM_ START8 |

**Table 305. FSM_START_ADD_H register description**

| | |
|---|---|
| FSM_START[15:8] | FSM start address value (MSbyte). Default value: 00000000 |

### 13.2.4 MLC_MAG_SENSITIVITY_L (E8h) and MLC_MAG_SENSITIVITY_H (E9h)

External magnetometer sensitivity value register for the machine learning core (R/W)

This register corresponds to the LSB-to-gauss conversion value of the external magnetometer sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits). Default value of MLC_MAG_S_[15:0] is 0x3C00, corresponding to 1 gauss/LSB.

**Table 306. MLC_MAG_SENSITIVITY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC_MAG_S_7 | MLC_MAG_S_6 | MLC_MAG_S_5 | MLC_MAG_S_4 | MLC_MAG_S_3 | MLC_MAG_S_2 | MLC_MAG_S_1 | MLC_MAG_S_0 |

**Table 307. MLC_MAG_SENSITIVITY_L register description**

| | |
|---|---|
| MLC_MAG_S_[7:0] | External magnetometer sensitivity (LSbyte). Default value: 00000000 |

**Table 308. MLC_MAG_SENSITIVITY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MLC_MAG_S_15 | MLC_MAG_S_14 | MLC_MAG_S_13 | MLC_MAG_S_12 | MLC_MAG_S_11 | MLC_MAG_S_10 | MLC_MAG_S_9 | MLC_MAG_S_8 |

**Table 309. MLC_MAG_SENSITIVITY_H register description**

| | |
|---|---|
| MLC_MAG_S_[15:8] | External magnetometer sensitivity (MSbyte). Default value: 00111100 |

# 14 Sensor hub register mapping

The table given below provides a list of the registers for the sensor hub functions available in the device and the corresponding addresses. The sensor hub registers are accessible when bit SHUB_REG_ACCESS is set to 1 in FUNC_CFG_ACCESS (01h).

**Table 310. Registers address map**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| SENSOR_HUB_1 | R | 02 | 00000010 | output | |
| SENSOR_HUB_2 | R | 03 | 00000011 | output | |
| SENSOR_HUB_3 | R | 04 | 00000100 | output | |
| SENSOR_HUB_4 | R | 05 | 00000101 | output | |
| SENSOR_HUB_5 | R | 06 | 00000110 | output | |
| SENSOR_HUB_6 | R | 07 | 00000111 | output | |
| SENSOR_HUB_7 | R | 08 | 00001000 | output | |
| SENSOR_HUB_8 | R | 09 | 00001001 | output | |
| SENSOR_HUB_9 | R | 0A | 00001010 | output | |
| SENSOR_HUB_10 | R | 0B | 00001011 | output | |
| SENSOR_HUB_11 | R | 0C | 00001100 | output | |
| SENSOR_HUB_12 | R | 0D | 00001101 | output | |
| SENSOR_HUB_13 | R | 0E | 00001110 | output | |
| SENSOR_HUB_14 | R | 0F | 00001111 | output | |
| SENSOR_HUB_15 | R | 10 | 00010000 | output | |
| SENSOR_HUB_16 | R | 11 | 00010001 | output | |
| SENSOR_HUB_17 | R | 12 | 00010010 | output | |
| SENSOR_HUB_18 | R | 13 | 00010011 | output | |
| MASTER_CONFIG | R/W | 14 | 00010100 | 00000000 | |
| SLV0_ADD | R/W | 15 | 00010101 | 00000000 | |
| SLV0_SUBADD | R/W | 16 | 00010110 | 00000000 | |
| SLV0_CONFIG | R/W | 17 | 00010111 | 00000000 | |
| SLV1_ADD | R/W | 18 | 00011000 | 00000000 | |
| SLV1_SUBADD | R/W | 19 | 00011001 | 00000000 | |
| SLV1_CONFIG | R/W | 1A | 00011010 | 00000000 | |
| SLV2_ADD | R/W | 1B | 00011011 | 00000000 | |
| SLV2_SUBADD | R/W | 1C | 00011100 | 00000000 | |
| SLV2_CONFIG | R/W | 1D | 00011101 | 00000000 | |
| SLV3_ADD | R/W | 1E | 00011110 | 00000000 | |
| SLV3_SUBADD | R/W | 1F | 00011111 | 00000000 | |
| SLV3_CONFIG | R/W | 20 | 00100000 | 00000000 | |
| DATAWRITE_SLV0 | R/W | 21 | 00100001 | 00000000 | |
| STATUS_MASTER | R | 22 | 00100010 | output | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 15 Sensor hub register description

## 15.1 SENSOR_HUB_1 (02h)

Sensor hub output register (R)

First byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 311. SENSOR_HUB_1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub1_7 | Sensor Hub1_6 | Sensor Hub1_5 | Sensor Hub1_4 | Sensor Hub1_3 | Sensor Hub1_2 | Sensor Hub1_1 | Sensor Hub1_0 |

**Table 312. SENSOR_HUB_1 register description**

| | |
|---|---|
| SensorHub1_[7:0] | First byte associated to external sensors |

## 15.2 SENSOR_HUB_2 (03h)

Sensor hub output register (R)

Second byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 313. SENSOR_HUB_2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub2_7 | Sensor Hub2_6 | Sensor Hub2_5 | Sensor Hub2_4 | Sensor Hub2_3 | Sensor Hub2_2 | Sensor Hub2_1 | Sensor Hub2_0 |

**Table 314. SENSOR_HUB_2 register description**

| | |
|---|---|
| SensorHub2_[7:0] | Second byte associated to external sensors |

## 15.3 SENSOR_HUB_3 (04h)

Sensor hub output register (R)

Third byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 315. SENSOR_HUB_3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub3_7 | Sensor Hub3_6 | Sensor Hub3_5 | Sensor Hub3_4 | Sensor Hub3_3 | Sensor Hub3_2 | Sensor Hub3_1 | Sensor Hub3_0 |

**Table 316. SENSOR_HUB_3 register description**

| | |
|---|---|
| SensorHub3_[7:0] | Third byte associated to external sensors |

## 15.4 SENSOR_HUB_4 (05h)

Sensor hub output register (R)

Fourth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 317. SENSOR_HUB_4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub4_7 | Sensor Hub4_6 | Sensor Hub4_5 | Sensor Hub4_4 | Sensor Hub4_3 | Sensor Hub4_2 | Sensor Hub4_1 | Sensor Hub4_0 |

**Table 318. SENSOR_HUB_4 register description**

| | |
|---|---|
| SensorHub4_[7:0] | Fourth byte associated to external sensors |

## 15.5 SENSOR_HUB_5 (06h)

Sensor hub output register (R)

Fifth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 319. SENSOR_HUB_5 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub5_7 | Sensor Hub5_6 | Sensor Hub5_5 | Sensor Hub5_4 | Sensor Hub5_3 | Sensor Hub5_2 | Sensor Hub5_1 | Sensor Hub5_0 |

**Table 320. SENSOR_HUB_5 register description**

| | |
|---|---|
| SensorHub5_[7:0] | Fifth byte associated to external sensors |

## 15.6 SENSOR_HUB_6 (07h)

Sensor hub output register (R)

Sixth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 321. SENSOR_HUB_6 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub6_7 | Sensor Hub6_6 | Sensor Hub6_5 | Sensor Hub6_4 | Sensor Hub6_3 | Sensor Hub6_2 | Sensor Hub6_1 | Sensor Hub6_0 |

**Table 322. SENSOR_HUB_6 register description**

| | |
|---|---|
| SensorHub6_[7:0] | Sixth byte associated to external sensors |

## 15.7 SENSOR_HUB_7 (08h)

Sensor hub output register (R)

Seventh byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 323. SENSOR_HUB_7 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub7_7 | Sensor Hub7_6 | Sensor Hub7_5 | Sensor Hub7_4 | Sensor Hub7_3 | Sensor Hub7_2 | Sensor Hub7_1 | Sensor Hub7_0 |

**Table 324. SENSOR_HUB_7 register description**

| | |
|---|---|
| SensorHub7_[7:0] | Seventh byte associated to external sensors |

## 15.8 SENSOR_HUB_8 (09h)

Sensor hub output register (R)

Eighth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 325. SENSOR_HUB_8 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub8_7 | Sensor Hub8_6 | Sensor Hub8_5 | Sensor Hub8_4 | Sensor Hub8_3 | Sensor Hub8_2 | Sensor Hub8_1 | Sensor Hub8_0 |

**Table 326. SENSOR_HUB_8 register description**

| | |
|---|---|
| SensorHub8_[7:0] | Eighth byte associated to external sensors |

## 15.9 SENSOR_HUB_9 (0Ah)

Sensor hub output register (R)

Ninth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 327. SENSOR_HUB_9 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub9_7 | Sensor Hub9_6 | Sensor Hub9_5 | Sensor Hub9_4 | Sensor Hub9_3 | Sensor Hub9_2 | Sensor Hub9_1 | Sensor Hub9_0 |

**Table 328. SENSOR_HUB_9 register description**

| | |
|---|---|
| SensorHub9_[7:0] | Ninth byte associated to external sensors |

## 15.10 SENSOR_HUB_10 (0Bh)

Sensor hub output register (R)

Tenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 329. SENSOR_HUB_10 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub10_7 | Sensor Hub10_6 | Sensor Hub10_5 | Sensor Hub10_4 | Sensor Hub10_3 | Sensor Hub10_2 | Sensor Hub10_1 | Sensor Hub10_0 |

**Table 330. SENSOR_HUB_10 register description**

| | |
|---|---|
| SensorHub10_[7:0] | Tenth byte associated to external sensors |

## 15.11 SENSOR_HUB_11 (0Ch)

Sensor hub output register (R)

Eleventh byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 331. SENSOR_HUB_11 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub11_7 | Sensor Hub11_6 | Sensor Hub11_5 | Sensor Hub11_4 | Sensor Hub11_3 | Sensor Hub11_2 | Sensor Hub11_1 | Sensor Hub11_0 |

**Table 332. SENSOR_HUB_11 register description**

| | |
|---|---|
| SensorHub11_[7:0] | Eleventh byte associated to external sensors |

## 15.12 SENSOR_HUB_12 (0Dh)

Sensor hub output register (R)

Twelfth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 333. SENSOR_HUB_12 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub12_7 | Sensor Hub12_6 | Sensor Hub12_5 | Sensor Hub12_4 | Sensor Hub12_3 | Sensor Hub12_2 | Sensor Hub12_1 | Sensor Hub12_0 |

**Table 334. SENSOR_HUB_12 register description**

| | |
|---|---|
| SensorHub12_[7:0] | Twelfth byte associated to external sensors |

## 15.13 SENSOR_HUB_13 (0Eh)

Sensor hub output register (R)

Thirteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 335. SENSOR_HUB_13 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub13_7 | Sensor Hub13_6 | Sensor Hub13_5 | Sensor Hub13_4 | Sensor Hub13_3 | Sensor Hub13_2 | Sensor Hub13_1 | Sensor Hub13_0 |

**Table 336. SENSOR_HUB_13 register description**

| | |
|---|---|
| SensorHub13_[7:0] | Thirteenth byte associated to external sensors |

## 15.14 SENSOR_HUB_14 (0Fh)

Sensor hub output register (R)

Fourteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 337. SENSOR_HUB_14 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub14_7 | Sensor Hub14_6 | Sensor Hub14_5 | Sensor Hub14_4 | Sensor Hub14_3 | Sensor Hub14_2 | Sensor Hub14_1 | Sensor Hub14_0 |

**Table 338. SENSOR_HUB_14 register description**

| | |
|---|---|
| SensorHub14_[7:0] | Fourteenth byte associated to external sensors |

## 15.15 SENSOR_HUB_15 (10h)

Sensor hub output register (R)

Fifteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 339. SENSOR_HUB_15 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub15_7 | Sensor Hub15_6 | Sensor Hub15_5 | Sensor Hub15_4 | Sensor Hub15_3 | Sensor Hub15_2 | Sensor Hub15_1 | Sensor Hub15_0 |

**Table 340. SENSOR_HUB_15 register description**

| | |
|---|---|
| SensorHub15_[7:0] | Fifteenth byte associated to external sensors |

## 15.16 SENSOR_HUB_16 (11h)

Sensor hub output register (R)

Sixteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 341. SENSOR_HUB_16 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub16_7 | Sensor Hub16_6 | Sensor Hub16_5 | Sensor Hub16_4 | Sensor Hub16_3 | Sensor Hub16_2 | Sensor Hub16_1 | Sensor Hub16_0 |

**Table 342. SENSOR_HUB_16 register description**

| | |
|---|---|
| SensorHub16_[7:0] | Sixteenth byte associated to external sensors |

## 15.17 SENSOR_HUB_17 (12h)

Sensor hub output register (R)

Seventeenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 343. SENSOR_HUB_17 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub17_7 | Sensor Hub17_6 | Sensor Hub17_5 | Sensor Hub17_4 | Sensor Hub17_3 | Sensor Hub17_2 | Sensor Hub17_1 | Sensor Hub17_0 |

**Table 344. SENSOR_HUB_17 register description**

| | |
|---|---|
| SensorHub17_[7:0] | Seventeenth byte associated to external sensors |

## 15.18 SENSOR_HUB_18 (13h)

Sensor hub output register (R)

Eighteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 345. SENSOR_HUB_18 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub18_7 | Sensor Hub18_6 | Sensor Hub18_5 | Sensor Hub18_4 | Sensor Hub18_3 | Sensor Hub18_2 | Sensor Hub18_1 | Sensor Hub18_0 |

**Table 346. SENSOR_HUB_18 register description**

| | |
|---|---|
| SensorHub18_[7:0] | Eighteenth byte associated to external sensors |

## 15.19 MASTER_CONFIG (14h)

Master configuration register (R/W)

**Table 347. MASTER_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| RST_MASTER_REGS | WRITE_ONCE | START_CONFIG | PASS_THROUGH_MODE | SHUB_PU_EN | MASTER_ON | AUX_SENS_ON1 | AUX_SENS_ON0 |

**Table 348. MASTER_CONFIG register description**

| | |
|---|---|
| RST_MASTER_REGS | Reset master logic and output registers. Must be set to 1 and then set it to 0. Default value: 0 |
| WRITE_ONCE | Slave 0 write operation is performed only at the first sensor hub cycle.<br>Default value: 0<br>(0: write operation for each sensor hub cycle;<br>1: write operation only for the first sensor hub cycle) |
| START_CONFIG | Sensor hub trigger signal selection. Default value: 0<br>(0: sensor hub trigger signal is the accelerometer/gyro data-ready;<br>1: sensor hub trigger signal external from INT2 pin) |
| PASS_THROUGH_MODE | I²C interface pass-through. Default value: 0<br>(0: pass-through disabled;<br>1: pass-through enabled, main I²C line is short-circuited with the auxiliary line) |
| SHUB_PU_EN | Enables master I²C pull-up. Default value: 0<br>(0: internal pull-up on auxiliary I²C line disabled;<br>1: internal pull-up on auxiliary I²C line enabled) |
| MASTER_ON | Enables sensor hub I²C master. Default: 0<br>(0: master I²C of sensor hub disabled; 1: master I²C of sensor hub enabled) |
| AUX_SENS_ON[1:0] | Number of external sensors to be read by the sensor hub.<br>(00: one sensor (default);<br>01: two sensors;<br>10: three sensors;<br>11: four sensors) |

## 15.20 SLV0_ADD (15h)

I²C slave address of the first external sensor (sensor 1) register (R/W)

**Table 349. SLV0_ADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| slave0_ add6 | slave0_ add5 | slave0_ add4 | slave0_ add3 | slave0_ add2 | slave0_ add1 | slave0_ add0 | rw_0 |

**Table 350. SLV0_ADD register description**

| | |
|---|---|
| slave0_add[6:0] | I²C slave address of sensor 1 that can be read by the sensor hub.<br>Default value: 0000000 |
| rw_0 | Read/write operation on Sensor 1. Default value: 0<br>(0: write operation; 1: read operation) |

## 15.21 SLV0_SUBADD (16h)

Address of register on the first external sensor (sensor 1) register (R/W)

**Table 351. SLV0_SUBADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| slave0_ reg7 | slave0_ reg6 | slave0_ reg5 | slave0_ reg4 | slave0_ reg3 | slave0_ reg2 | slave0_ reg1 | slave0_ reg0 |

**Table 352. SLV0_SUBADD register description**

| | |
|---|---|
| slave0_reg[7:0] | Address of register on sensor 1 that has to be read/written according to the rw_0 bit value in SLV0_ADD (15h). Default value: 00000000 |

## 15.22 SLV0_CONFIG (17h)

First external sensor (sensor 1) configuration and sensor hub settings register (R/W)

**Table 353. SLV0_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SHUB_ ODR_1 | SHUB_ ODR_0 | 0(1) | 0(1) | BATCH_EXT_ SENS_0_EN | Slave0_ numop2 | Slave0_ numop1 | Slave0_ numop0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 354. SLV0_CONFIG register description**

| | |
|---|---|
| SHUB_ODR_[1:0] | Rate at which the master communicates. Default value: 00<br>(00: 104 Hz (or at the maximum ODR between the accelerometer and gyroscope if it is less than 104 Hz);<br>01: 52 Hz (or at the maximum ODR between the accelerometer and gyroscope if it is less than 52 Hz);<br>10: 26 Hz (or at the maximum ODR between the accelerometer and gyroscope if it is less than 26 Hz);<br>11: 12.5 Hz (or at the maximum ODR between the accelerometer and gyroscope if it is less than 12.5 Hz) |
| BATCH_EXT_SENS_0_EN | Enables FIFO data batching of first slave. Default value: 0 |
| Slave0_numop[2:0] | Number of read operations on sensor 1. Default value: 000 |

## 15.23 SLV1_ADD (18h)

I²C slave address of the second external sensor (sensor 2) register (R/W)

**Table 355. SLV1_ADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave1_ add6 | Slave1_ add5 | Slave1_ add4 | Slave1_ add3 | Slave1_ add2 | Slave1_ add1 | Slave1_ add0 | r_1 |

**Table 356. SLV1_ADD register description**

| | |
|---|---|
| Slave1_add[6:0] | I²C slave address of sensor 2 that can be read by the sensor hub.<br>Default value: 0000000 |
| r_1 | Enables read operation on sensor 2. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

## 15.24 SLV1_SUBADD (19h)

Address of register on the second external sensor (sensor 2) register (R/W)

**Table 357. SLV1_SUBADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave1_ reg7 | Slave1_ reg6 | Slave1_ reg5 | Slave1_ reg4 | Slave1_ reg3 | Slave1_ reg2 | Slave1_ reg1 | Slave1_ reg0 |

**Table 358. SLV1_SUBADD register description**

| | |
|---|---|
| Slave1_reg[7:0] | Address of register on sensor 2 that has to be read/written according to the r_1 bit value in SLV1_ADD (18h). |

## 15.25 SLV1_CONFIG (1Ah)

Second external sensor (sensor 2) configuration register (R/W)

**Table 359. SLV1_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | BATCH_EXT_ SENS_1_EN | Slave1_ numop2 | Slave1_ numop1 | Slave1_ numop0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 360. SLV1_CONFIG register description**

| | |
|---|---|
| BATCH_EXT_SENS_1_EN | Enables FIFO data batching of second slave. Default value: 0 |
| Slave1_numop[2:0] | Number of read operations on sensor 2. Default value: 000 |

## 15.26 SLV2_ADD (1Bh)

I²C slave address of the third external sensor (sensor 3) register (R/W)

**Table 361. SLV2_ADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave2_ add6 | Slave2_ add5 | Slave2_ add4 | Slave2_ add3 | Slave2_ add2 | Slave2_ add1 | Slave2_ add0 | r_2 |

**Table 362. SLV2_ADD register description**

| | |
|---|---|
| Slave2_add[6:0] | I²C slave address of sensor 3 that can be read by the sensor hub. |
| r_2 | Enables read operation on sensor 3. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

## 15.27 SLV2_SUBADD (1Ch)

Address of register on the third external sensor (sensor 3) register (R/W)

**Table 363. SLV2_SUBADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave2_ reg7 | Slave2_ reg6 | Slave2_ reg5 | Slave2_ reg4 | Slave2_ reg3 | Slave2_ reg2 | Slave2_ reg1 | Slave2_ reg0 |

**Table 364. SLV2_SUBADD register description**

| | |
|---|---|
| Slave2_reg[7:0] | Address of register on sensor 3 that has to be read/written according to the r_2 bit value in SLV2_ADD (1Bh). |

## 15.28 SLV2_CONFIG (1Dh)

Third external sensor (sensor 3) configuration register (R/W)

**Table 365. SLV2_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | BATCH_EXT_ SENS_2_EN | Slave2_ numop2 | Slave2_ numop1 | Slave2_ numop0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 366. SLV2_CONFIG register description**

| | |
|---|---|
| BATCH_EXT_SENS_2_EN | Enables FIFO data batching of third slave. Default value: 0 |
| Slave2_numop[2:0] | Number of read operations on sensor 3. Default value: 000 |

## 15.29 SLV3_ADD (1Eh)

I²C slave address of the fourth external sensor (sensor 4) register (R/W)

**Table 367. SLV3_ADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave3_ add6 | Slave3_ add5 | Slave3_ add4 | Slave3_ add3 | Slave3_ add2 | Slave3_ add1 | Slave3_ add0 | r_3 |

**Table 368. SLV3_ADD register description**

| | |
|---|---|
| Slave3_add[6:0] | I²C slave address of sensor 4 that can be read by the sensor hub. |
| r_3 | Enables read operation on sensor 4. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

## 15.30 SLV3_SUBADD (1Fh)

Address of register on the fourth external sensor (sensor 4) register (R/W)

**Table 369. SLV3_SUBADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave3_ reg7 | Slave3_ reg6 | Slave3_ reg5 | Slave3_ reg4 | Slave3_ reg3 | Slave3_ reg2 | Slave3_ reg1 | Slave3_ reg0 |

**Table 370. SLV3_SUBADD register description**

| | |
|---|---|
| Slave3_reg[7:0] | Address of register on sensor 4 that has to be read according to the r_3 bit value in SLV3_ADD (1Eh). |

## 15.31 SLV3_CONFIG (20h)

Fourth external sensor (sensor 4) configuration register (R/W)

**Table 371. SLV3_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | BATCH_EXT_ SENS_3_EN | Slave3_ numop2 | Slave3_ numop1 | Slave3_ numop0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 372. SLV3_CONFIG register description**

| | |
|---|---|
| BATCH_EXT_SENS_3_EN | Enables FIFO data batching of fourth slave. Default value: 0 |
| Slave3_numop[2:0] | Number of read operations on sensor 4. Default value: 000 |

## 15.32 DATAWRITE_SLV0 (21h)

Data to be written into the slave device register (R/W)

**Table 373. DATAWRITE_SLV0 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave0_ dataw7 | Slave0_ dataw6 | Slave0_ dataw5 | Slave0_ dataw4 | Slave0_ dataw3 | Slave0_ dataw2 | Slave0_ dataw1 | Slave0_ dataw0 |

**Table 374. DATAWRITE_SLV0 register description**

| | |
|---|---|
| Slave0_dataw[7:0] | Data to be written into the slave 0 device according to the rw_0 bit in register SLV0_ADD (15h).<br>Default value: 00000000 |

## 15.33 STATUS_MASTER (22h)

Sensor hub source register (R)

**Table 375. STATUS_MASTER register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WR_ONCE _DONE | SLAVE3_ NACK | SLAVE2_ NACK | SLAVE1_ NACK | SLAVE0_ NACK | 0 | 0 | SENS_HUB _ENDOP |

**Table 376. STATUS_MASTER register description**

| | |
|---|---|
| WR_ONCE_DONE | When the bit WRITE_ONCE in MASTER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on slave 0 has been performed and completed. Default value: 0 |
| SLAVE3_NACK | This bit is set to 1 if not acknowledge occurs on slave 3 communication. Default value: 0 |
| SLAVE2_NACK | This bit is set to 1 if not acknowledge occurs on slave 2 communication. Default value: 0 |
| SLAVE1_NACK | This bit is set to 1 if not acknowledge occurs on slave 1 communication. Default value: 0 |
| SLAVE0_NACK | This bit is set to 1 if not acknowledge occurs on slave 0 communication. Default value: 0 |
| SENS_HUB_ENDOP | Sensor hub communication status. Default value: 0<br>(0: sensor hub communication not concluded;<br>1: sensor hub communication concluded) |

# 16 Soldering information

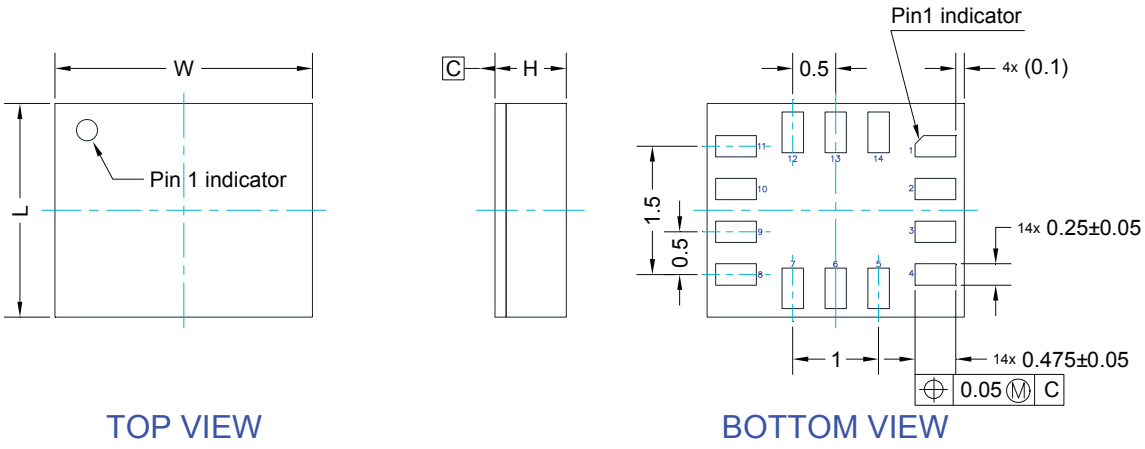
The LGA package is compliant with the ECOPACK and RoHS standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.
For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

# 17 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 17.1 LGA-14L package information

**Figure 23. LGA-14L 2.5 x 3.0 x 0.86 mm package outline and mechanical data**




Dimensions are in millimeter unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

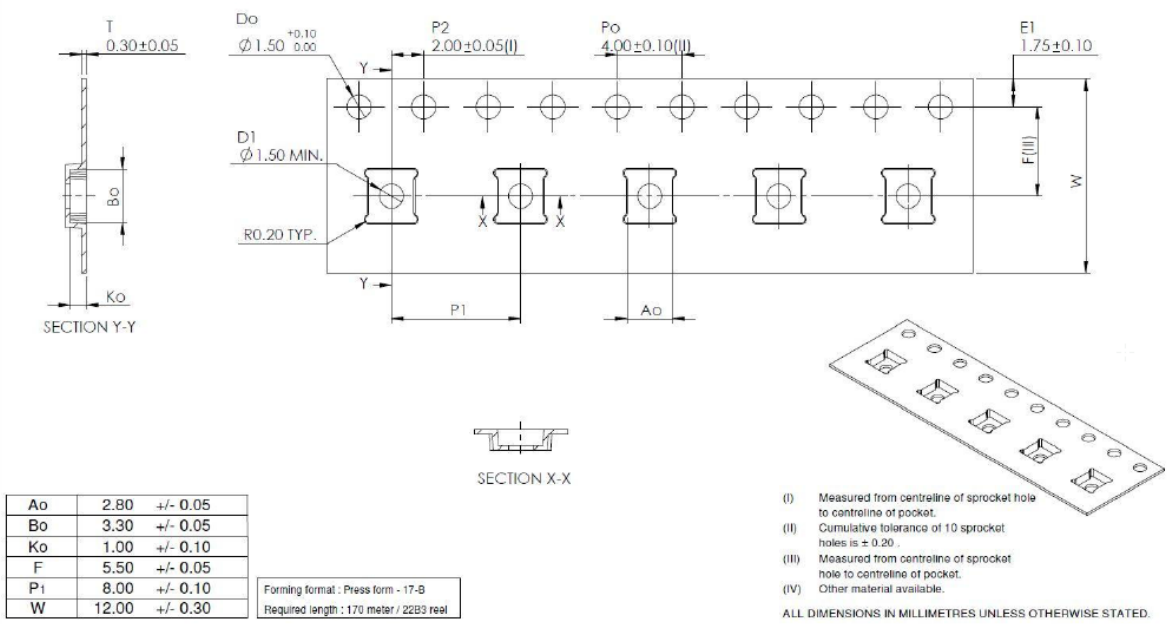
OUTER DIMENSIONS

| ITEM | DIMENSION [mm] | TOLERANCE [mm] |
|---|---|---|
| Length [L] | 2.50 | ±0.1 |
| Width [W] | 3.00 | ±0.1 |
| Height [H] | 0.86 | MAX |

DM00249496_5

## 17.2 LGA-14 packing information

Figure 24. **Carrier tape information for LGA-14 package**




| | | |
|---|---|---|
| Ao | 2.80 | +/- 0.05 |
| Bo | 3.30 | +/- 0.05 |
| Ko | 1.00 | +/- 0.10 |
| F | 5.50 | +/- 0.05 |
| P1 | 8.00 | +/- 0.10 |
| W | 12.00 | +/- 0.30 |

Forming format : Press form - 17-B
Required length : 170 meter / 22B3 reel

Figure 25. **LGA-14 package orientation in carrier tape**

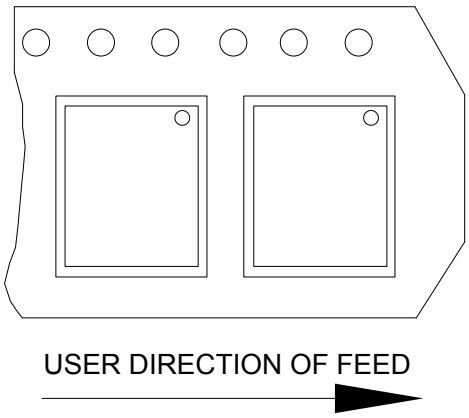


Figure 26. **Reel information for carrier tape of LGA-14 package**

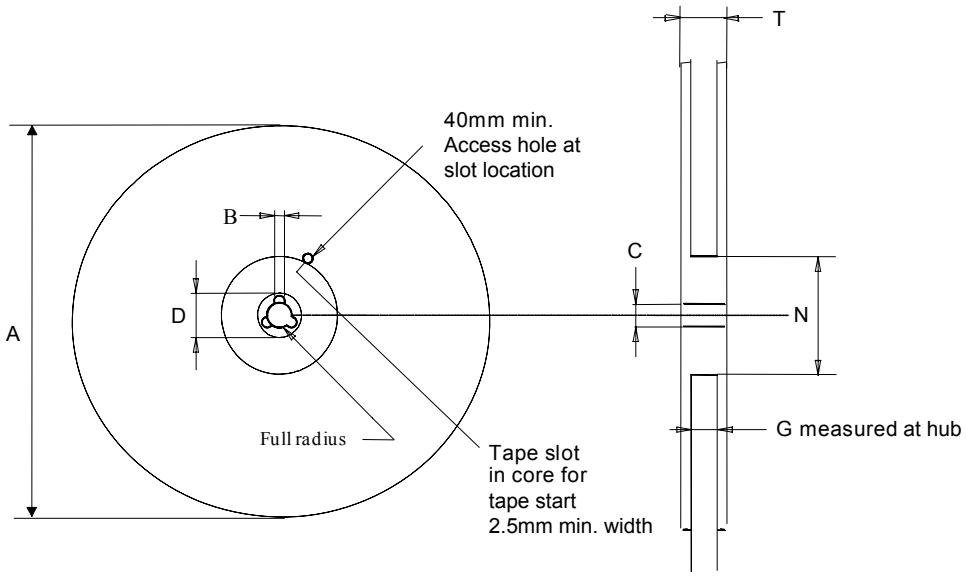



Table 377. **Reel dimensions for carrier tape of LGA-14 package**

| Reel dimensions (mm) | |
|---|---|
| A (max) | 330 |
| B (min) | 1.5 |
| C | 13 ±0.25 |
| D (min) | 20.2 |
| N (min) | 60 |
| G | 12.4 +2/-0 |
| T (max) | 18.4 |

# Revision history

Table 378. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 11-Jul-2023 | 1 | Initial release |
| 29-Nov-2023 | 2 | Updated Features |

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