TDA8035

High integrated and low power smart card interface

Rev. 3.1 — 30 June 2016 Product data sheet

1. General description

The TDA8035 is the cost efficient successor of the established integrated contact smart card reader IC TDA8024. It offers a high level of security for the card by performing current limitation, short-circuit detection, ESD protection as well as supply supervision. The current consumption during the standby mode of the contact reader is very low as it operates in the 3 V supply domain. The TDA8035 is therefore the ideal component for a power efficient contact reader.

2. Features and benefits

2.1 Protection of the contact smart card

- Thermal and short-circuit protection on all card contacts
- V_{CC} regulation:
  - 5 V, 3 V, 1.8 V ± 5 % on 2 × 220 nF multilayer ceramic capacitors with low ESR
  - Current spikes of 40 nA/s (V_{CC} = 5 V and 3 V) or 15 nA/s (V_{CC} = 1.8 V) up to 20 MHz, with controlled rise and fall times. Filtered overload detection is approximately 120 mA.
- Automatic activation and deactivation sequences initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, falling V_{REG} $V_{DD(INTF)}$,V_{DDP}
- Enhanced card-side ElectroStatic Discharge (ESD) protection of (> 8 kV)
- Supply supervisor for killing spikes during power on and off:
  - threshold internally fixed
  - externally by a resistor bridge

2.2 Easy integration into your contact reader

- SW compatible to TDA8024 and TDA8034
- 5 V, 3 V, 1.8 V smart card supply
- DC-to-DC converter for V_{CC} generation separately powered from 2.7 V to 5.5 V supply (V_{DDP} and GNDP)
- Very low power consumption in Deep Shutdown mode
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7 and C8)
- External clock input up to 26 MHz
- Card clock generation up to 20 MHz using pins CLKDIV1 and CLKDIV2 with synchronous frequency changes of f_{XTAL}, fXTAL/2, fXTAL/4 or fXTAL/8
- Non-inverted control of pin RST using pin RSTIN
- Built-in debouncing on card presence contact
- Multiplexed status signal using pin OFFN

- Chip Select digital input for parallel operation of several TDA8035 ICs.

2.2.1 Other

- HVQFN32 package
- Compliant with ISO 7816, NDS and EMV 4.3 (*) payment systems

(*) for C2 version

3. Applications

- Pay TV
- Electronic payment
- Identification
- IC card readers for banking

4. Quick reference data

Table 1. Quick reference data

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{xtal} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DDP}	power supply voltage		2.7	3.3	5.5	V
$V_{DD(INTF)}$	interface supply voltage		1.6	3.3	3.6	V
I_{DDP}	power supply current	deep shutdown mode; f_{XTAL} = stopped;	-	0.1	3	µA
		shutdown mode; f_{XTAL} = stopped;	-	300	500	µA
		active mode; V_{CC} = +5 V CLK = f_{XTAL}/2; no load	-	-	5	mA
		active mode; CLK = f_{XTAL}/2; V_{CC} = +5 V; I_{CC} = 65 mA	-	-	220	mA
		active mode; CLK = f_{XTAL}/2; V_{CC} = +3 V; I_{CC} = 65 mA	-	-	160	mA
		active mode; CLK = f_{XTAL}/2; V_{CC} = +1.8 V; I_{CC} = 35 mA	-	-	120	mA
$I_{DD(INTF)}$	interface supply current	deep shutdown mode; f_{XTAL} = stopped; present card	-	-	1	µA
		shutdown mode; f_{XTAL} = stopped; present card	-	-	1	µA
Internal supply voltage						
V_{DD}	supply voltage		1.62	1.8	1.98	V

Table 1. Quick reference data *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{xtal} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Card supply voltage: pin VCC						
V_{CC}	supply voltage	5 V card; DC ICC < 65 mA	4.75	5.0	5.25	V
		5 V card; AC current spikes of 40 nA/s	4.65	5.0	5.25	V
		3 V card; DC I_{CC} < 65 mA	2.85	-	3.15	V
		3 V card; AC current spikes of 40 nA/s	2.76	-	3.24	V
		1.8 V card; DC I_{CC} < 35 mA	1.71	-	1.89	V
		1.8 V card; AC current spikes of 15 nA/s	1.66	-	1.94	V
$V_{ripple(p-p)}$	peak-to-peak ripple voltage	from 20 kHz to 200 MHz	-	-	300	mV
I_{CC}	supply current	$V_{CC = 5\ V\ or\ 3\ V}$	-	-	65	mA
		$V_{CC = 1.8\ V}$	-	-	35	mA
General						
t_{deact}	deactivation time	total sequence	35	90	250	µs
P_{tot}	total power dissipation		-	-	0.45	W
T_{amb}	ambient temperature		−25	-	+85	°C

5. Ordering information

The TDA8035 is available in 2 versions, which have the same functionalities. The C2 version is compliant with the EMVC0 4.3 standard.

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8035HN/C1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-7
TDA8035HN/C1/S1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm; [1]	SOT617-7
TDA8035HN/C2/S1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm; [1]	SOT617-7

[1] copper wiring

6. Block diagram

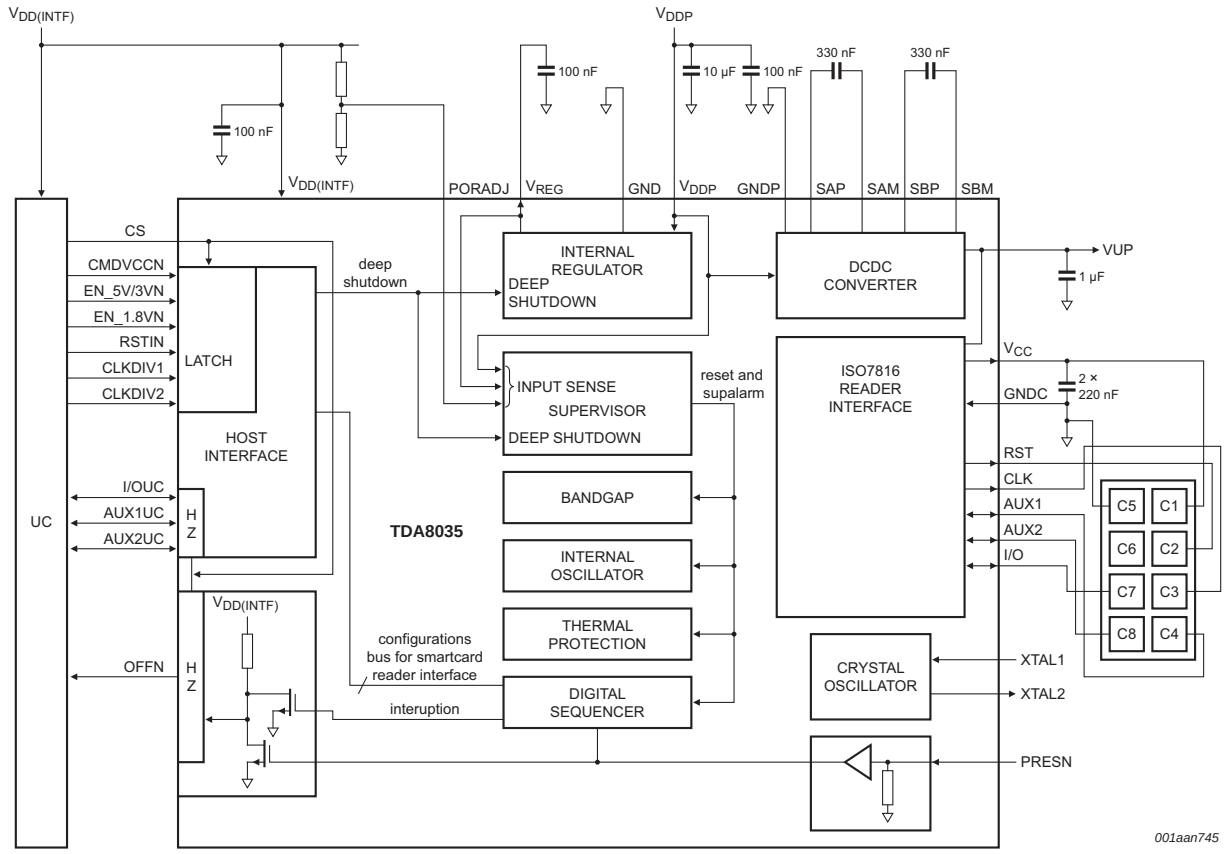


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

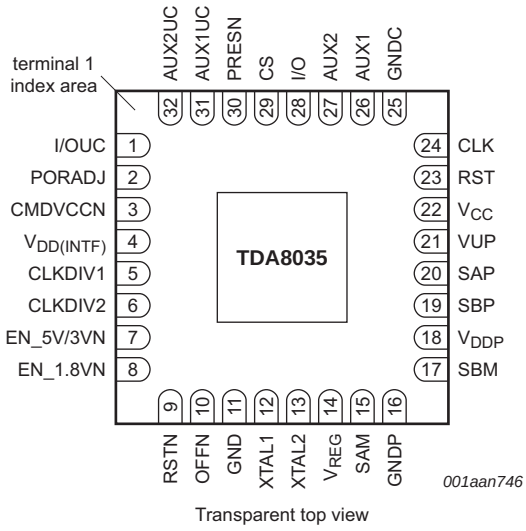


Fig 2. Pin configuration HVQFN32

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Supply	Type	Description
I/OUC	1	$V_{DD(INTF)}$	I/O	host data I/O line (internal 10 kΩ pull-up resistor to $V_{DD(INTF)}$)
PORADJ	2	$V_{DD(INTF)}$	I	Input for $V_{DD(INTF)}$ supervisor. PORADJ threshold can be changed with an external R bridge
CMDVCCN	3	$V_{DD(INTF)}$	I	start activation sequence input from the host (active LOW)
$V_{DD(INTF)}$	4	$V_{DD(INTF)}$	supply	interface supply voltage
CLKDIV1	5	$V_{DD(INTF)}$	I	control with CLKDIV2 for choosing CLK frequency (see Table 4)
CLKDIV2	6	$V_{DD(INTF)}$	I	control with CLKDIV1 for choosing CLK frequency (see Table 4)
EN_5V/3VN	7	$V_{DD(INTF)}$	I	control signal for selecting V_{CC} = 5 V (HIGH) or V_{CC} = 3 V (LOW) if EN_1.8 VN = High
EN_1.8 VN	8	$V_{DD(INTF)}$	I	control signal for selecting V_{CC} = 1.8 V (low)
RSTIN	9	$V_{DD(INTF)}$	I	card reset input from the host (active HIGH)
OFFN	10	$V_{DD(INTF)}$	O	NMOS interrupt to the host (active LOW) with 10 kΩ internal pull-up resistor to $V_{DD(INTF)}$ (See fault detection)
GND	11	-	supply	ground
XTAL1	12	$V_{DD(INTF)}$	I	crystal connection 1
XTAL2	13	$V_{DD(INTF)}$	O	crystal connection 2
V_{REG}	14	V_{DDP}	supply	Internal supply voltage
SAM	15	V_{DDP}	I/O	DC-to-DC converter capacitor; connected between SAM and SAP; C = 330 nF or 100 nF (see Figure 13) with ESR < 100 mΩ at Freq=100kHz
GNDP	16	-	supply	DC-to-DC converter power supply ground

Table 3. Pin description *…continued*

Symbol	Pin	Supply	Type	Description
SBM	17	V_{DDP}	I/O	DC-to-DC converter capacitor; connected between SBM and SBP; C = 330 nF or 100nF (see Figure 13) with ESR < 100 mΩ at Freq=100kHz
V_{DDP}	18	V_{DDP}	supply	Power supply voltage
SBP	19	V_{DDP}	I/O	DC-to-DC converter capacitor; connected between SBM and SBP; C = 330 nF or 100nF (see Figure 13) with ESR < 100 mΩ at Freq=100kHz
SAP	20	V_{DDP}	I/O	DC-to-DC converter capacitor; connected between SAM and SAP; C = 330 nF or 100nF (see Figure 13) with ESR < 100 mΩ at Freq=100kHz
VUP	21	V_{DDP}	I/O	DC-to-DC converter output decoupling capacitor connected between VUP and GNDP; C = 1 μF with ESR < 100 mΩ at Freq=100kHz
V_{CC}	22	V_{CC}	O	supply for the card (C1), decouple to GND with 2 × 220 nF capacitors with ESR < 100 mΩ
RST	23	V_{CC}	O	card reset (C2)
CLK	24	V_{CC}	O	clock to the card (C3)
GNDC	25	-	supply	card signal ground
AUX1	26	V_{CC}	I/O	auxiliary data line to and from the card (C4), internal 10 kΩ pull-up resistor to V_{CC}
AUX2	27	V_{CC}	I/O	auxiliary data line to and from the card (C8), internal 10 kΩ pull-up resistor to V_{CC}
I/O	28	V_{CC}	I/O	data line to and from the card (C7), internal 10 kΩ pull-up resistor to V_{CC}
CS	29	$V_{DD(INTF)}$	I	Chip Select input from the host (active High)
PRESN	30	$V_{DD(INTF)}$	I	Card presence contact input (active LOW); if PRESN is true, then the card is considered as present. A debouncing feature of 4.05 ms typical is built in.
AUX1UC	31	$V_{DD(INTF)}$	I/O	auxiliary data line to and from the host, internal 10 kΩ pull-up resistor to $V_{DD(INTF)}$
AUX2UC	32	$V_{DD(INTF)}$	I/O	auxiliary data line to and from the host, internal 10 kΩ pull-up resistor to $V_{DD(INTF)}$

8. Functional description

Remark: The ISO 7816 terminology convention has been adhered to throughout this document, and it is assumed that the reader is familiar with this convention.

8.1 Power supply

Power supply voltage V_{DDP} is from 2.7 V to 5.5 V

All interface signals with the system controller are referenced to $V_{DD(INTF)}$. All card contacts remain inactive during powering up or powering down.

Internal regulator V_{REG} is 1.8 V

After powering the device, OFFN remains low until CMDVCCN is set high and PRESN is low.

During power off, OFFN falls low when V_{DDP} is below the threshold voltage falling.

While the card is not activated, CMDVCCN is kept at high level. To save power consumption, the frequency of the internal oscillator ($f_{osc(int)}$) used for the activation sequences is put in low frequency mode.

This device includes a DC-to-DC converter to generate the 5 V, 3 V or 1.8 V card supply voltage (V_{CC}). The DC-to-DC converter is separately supplied by V_{DDP} and G_{NDP}. The DC-to-DC converter operates as a voltage tripler, doubler or follower according to the respective values of V_{CC} and V_{DDP}.

Special care has to me made in the selection of the capacitors of the DC/DC converter specially with respect to capacitor value versus voltage and ESR (see Table 7)

The operating mode is as follows (see Figure 3):

- V_{CC} = 5 V and V_{DDP} > 3.8 V; voltage doubler
- V_{CC} = 5 V and V_{DDP} < 3.6 V; voltage tripler
- V_{CC} = 3 V and V_{DDP} > 3.8 V; voltage follower
- V_{CC} = 3 V and V_{DDP} < 3.6 V; voltage doubler
- V_{CC} = 1.8 V and V_{DDP} > 3.8 V; voltage doubler
- V_{CC} = 1.8 V and V_{DDP} < 3.6 V; voltage tripler

8.2 Voltage supervisor

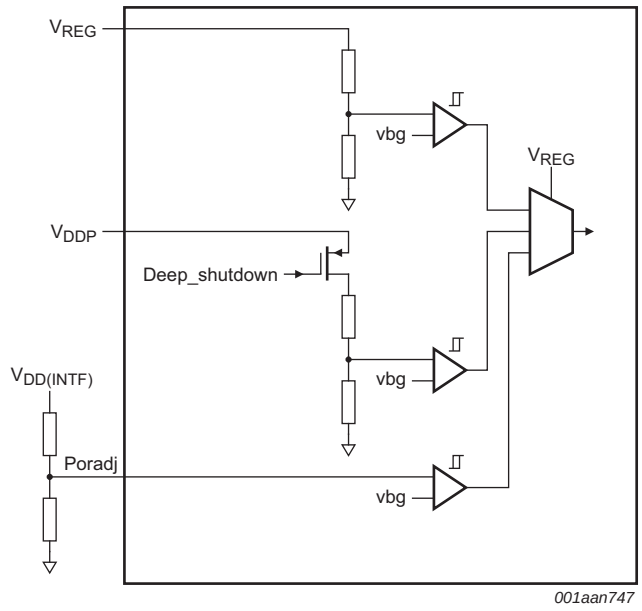


Fig 3. Block voltage supervisor

The voltage supervisor is used as a power-on reset, and also as supply drop detection during a card session. The threshold of the voltage supervisor is set internally in the IC for VDDP and VREG. The threshold can be adjusted externally for VDD(INTF) using the PORADJ pin. As long as VREG is less than $V_{th(VREG)} + V_{hys(VREG)}$, the IC remains inactive whatever the levels on the command lines are. The inactivity lasts for the duration of t_w after VREG has reached a level higher than $V_{th(VREG)} + V_{hys(VREG)}$. The outputs of the VDDP, VREG and VDD(INTF) supervisors are combined and sent to a digital controller in order to reset the TDA8035. The reset pulse of approximately 5.7 ms ($t_w = 2048 \times 1/(f_{osc(int)\_Low})$) is used internally for maintaining the IC in an inactive mode during the supply voltage power-on (see Figure 4 and Figure 5). A deactivation sequence is performed when:

- VREG falls below $V_{th(VREG)}$
- $V_{DD(INTF)}$ falls below $V_{th(PORADJ)}$
- VDDP falls below $V_{th(VDDP)}$

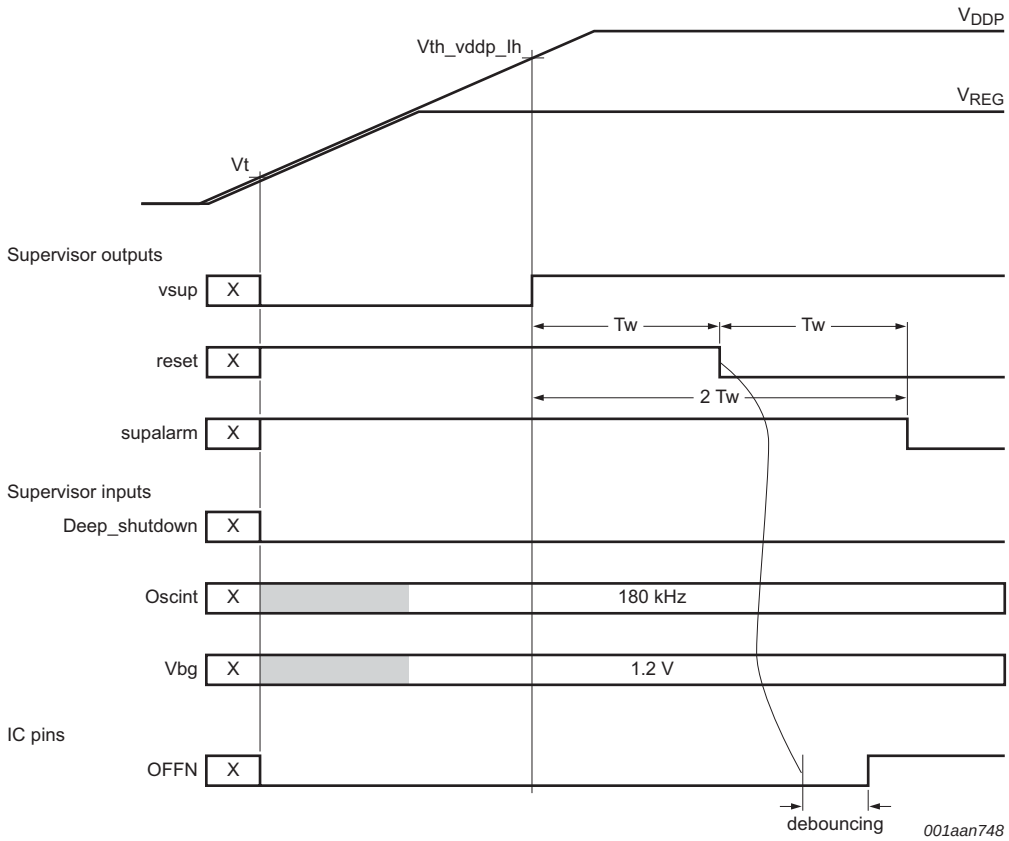


Fig 4. Voltage supervisor

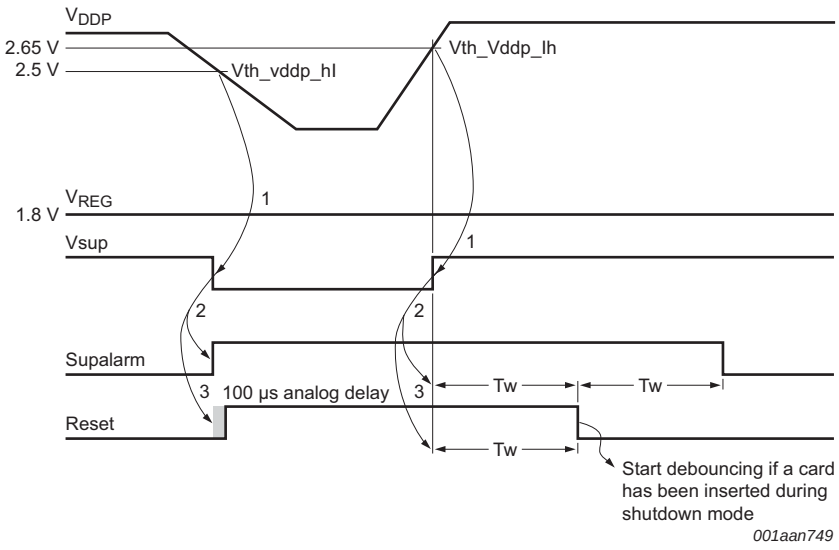


Fig 5. Voltage supervisor

8.3 Clock circuitry

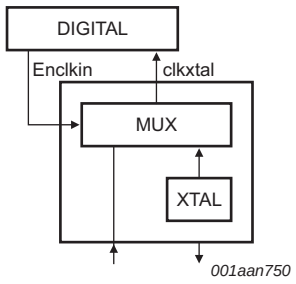


Fig 6. Switch external clock

To generate the card clock CLK, the TDA8035 can either use an external clock provided on XTAL1 pin or a crystal oscillator connected on both XTAL1 and XTAL2 pins. The TDA8035 automatically detects when an external clock is provided on XTAL1. Consequently, there is no need for an extra pin to configure the clock source (external clock or crystal).

The automatic clock source detection is performed on each activation command (CMDVCCN pin falling edge). During a time window defined by the internal oscillator, the presence of an external clock on XTAL1 pin is checked. If a clock is detected, the crystal oscillator is kept stopped, else, the crystal oscillator is started. It is mandatory when an external clock is used, that the clock is applied on XTAL1 before CMDVCCN falling edge signal.

The frequency is chosen as f_{XTAL}, $f_{XTAL/2}$, $f_{XTAL/4}$ or $f_{XTAL/8}$ via the pins CLKDIV1 and CLKDIV2. Both selection inputs are not changed simultaneously. A minimum of 10 ns is required between changes on CLKDIV1 and CLKDIV2.

The frequency change is synchronous, which means that during transition, no pulse is shorter than 45 % of the smallest period. This ensures that the first and last clock pulse around the change has the correct width. When changing the frequency dynamically, the change is effective for only 10 periods of XTAL1 after the command.

The duty cycle on pin CLK is between 45 % and 55 %:

- When an external clock is used on XTAL1 pin and f_{XTAL} is used, the duty cycle is between 48 % and 52 %. The subsequent rise and fall times ($t_{r(i)}$ and $t_{f(i)}$) conform to values listed in Table 7. It has to connect a 56 pF serial capacitor (see Figure 13).
- CLK frequency is f_{XTAL}, $f_{XTAL/2}$, $f_{XTAL/4}$ or $f_{XTAL/8}$:
  It is guaranteed between 45 % and 55 % of the period by the frequency dividers.

Table 4. Clock configuration

CLKDIV1	CLKDIV2	CLK
0	0	$f_{XTAL/8}$
0	1	$f_{XTAL/4}$
1	1	$f_{XTAL/2}$
1	0	f_{XTAL}

8.4 I/O circuitry

The three data lines I/O, AUX1 and AUX2 are identical.

To enter the idle state, both lines (I/O and I/OUC) are pulled HIGH via a 10 kΩ resistor (I/O to V_{CC} and I/OUC to $V_{DD(INTF)}$).

I/O is referenced to V_{CC}, and I/OUC to $V_{DD(INTF)}$ which allows operation with $V_{CC} \neq V_{DD(INTF)}$.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other line, which becomes the slave.

After a time delay $t_{d(edge)}$, the logic 0 present on the master side is transmitted to the slave side.

When the master side returns to logic 1, the slave side transmits the logic 1 during the time delay t_{pu} and both sides return to their idle states.

The active pull-up feature ensures fast Low to High transitions. It is able to deliver more than 1 mA to an output voltage of 0.9 V_{CC} on an 80 pF load. At the end of the active pull-up pulse, the output voltage depends on the internal pull-up resistor and on the load current.

The current to and from the cards I/O lines is internally limited to 15 mA.

The maximum frequency on these lines is 1.5 MHz.

8.5 CS control

The CS (Chip Select) input allows multiple devices to operate in parallel. When CS is high, the system interface signals operate as described. When CS is low, the signals CMDVCCN, RSTIN, CLKDIV1, CLKDIV2, EN_5V/3VN and EN_1.8VN are latched. I/OUC, AUX1UC and AUX2UC are set to high impedance pull-up mode and data is no longer passed to or from the smart card. The OFFN output is a 3-state output.

8.6 Shutdown mode and Deep Shutdown mode

After power-on reset, the circuit enters the Shutdown mode if CMDVCCN input pin is set to a logic high. A minimum number of circuits are active while waiting for the microcontroller to start a session.

1. All card contacts are inactive (approximately 200 Ω to GND).
2. I/OUC, AUX1UC and AUX2UC are high impedance (10 kW pull-up resistor connected to $V_{DD(INTF)}$).
3. Voltage generators are stopped.
4. Voltage supervisor is active.
5. The internal oscillator runs at its low frequency.

A Deep Shutdown mode can be entered by forcing CMDVCCN input pin to a logic-High state and EN_5V/3VN, EN_1.8VN input pins to a logic-Low state. Deep Shutdown mode can only be entered when the smart card reader is inactive. In Deep Shutdown mode, all circuits are disabled. The OFFN pin follows the status of PRESN pin. To exit Deep Shutdown mode, change the state of one or more of the three control pins. Figure 8 shows the control sequence for entering and exiting.

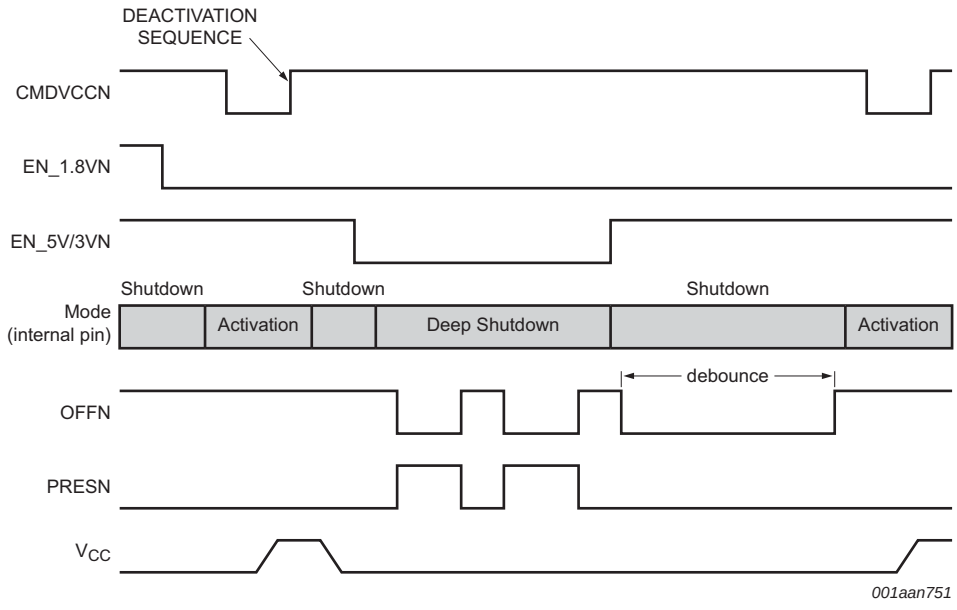


Fig 7. Shutdown mode and Deep Shutdown mode

8.7 Activation sequence

The following sequence then occurs with crystal oscillator (see Figure 8):

$T = 64 \times T_{oscint}$ (freq high)

1. CMDVCCN is pulled low (t0)
2. Crystal oscillator start-up time (t0).
3. The internal oscillator changes to its high frequency and DC-to-DC starts $t1 = t0 + 768 \times T_{osc\ (freq\ low)}$
4. V_{CC} rises from 0 to selected V_{CC} value (5 V, 3 V, 1.8 V) with a controlled slope ($t_2 = t_1 + 3T/2$)
5. I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 10T$), until now, they were pulled LOW
6. CLK is applied to the C3 contact ($t_4 = t_3 + \times$) with 200 ns < × < 10 × $1/f_{Xtal}$
7. RST is enabled ($t_5 = t_1 + 13T$).

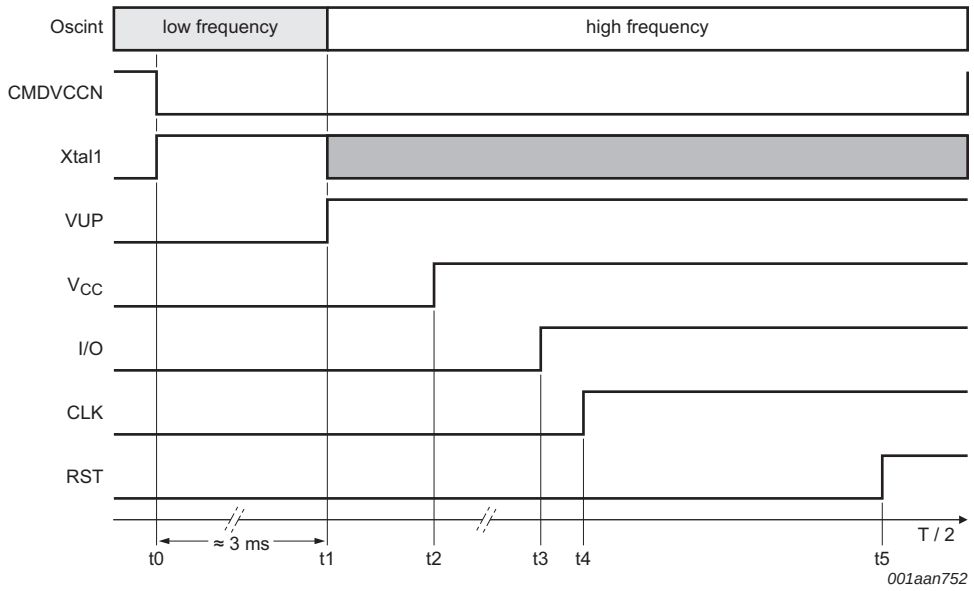


Fig 8. Activation sequence at t3

8.8 Deactivation sequence

When a session is completed, the microcontroller sets the CMDVCCN line to the HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in the inactive state (see Figure 9):

1. RST goes LOW ($t_{11} = t_{10} + 3T/64$)
2. CLK is stopped LOW ($t_{12} = t_{11} + T/2$)
3. I/O, AUX1 and AUX2 are pulled LOW ($t_{13} = t_{11} + T$)
4. V_{CC} falls to zero ($t_{14} = t_{11} + 3T/2$). The deactivation sequence is completed when V_{CC} reaches its inactive state
5. VUP falls to zero ($t_{15} = t_{11} + 7T/2$)
6. $V_{CC} < 0.4$ V ($t_{de} = t_{11} + 3T/2 + V_{CC}$ fall time)
7. All card contacts become low-impedance to GND. I/OUC, AUX1UC and AUX2UC remain pulled up to $V_{DD(INTF)}$ via a 10 kΩ resistor.
8. The internal oscillator reverts to its lower frequency.

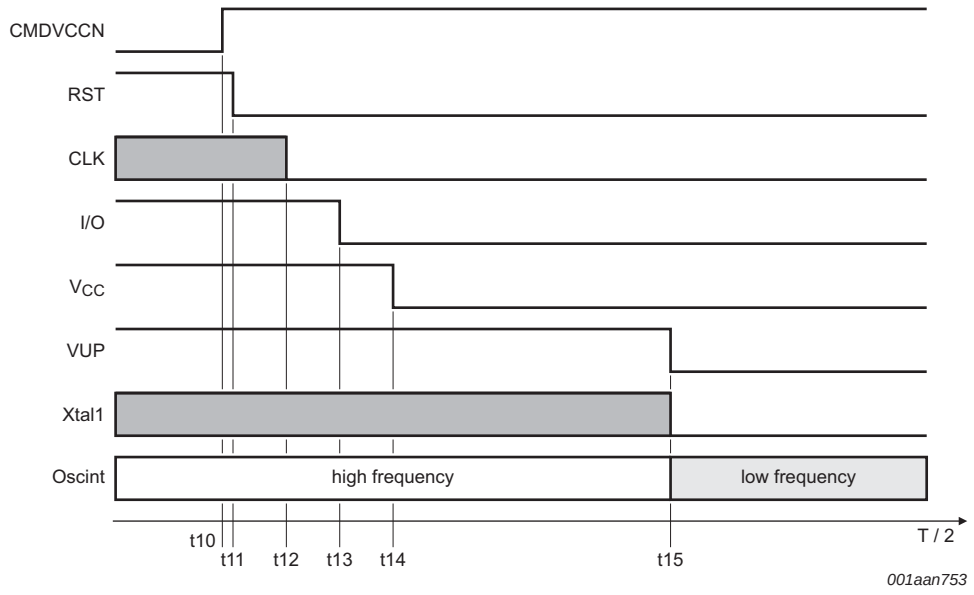


Fig 9. Deactivation sequence

8.9 V_{CC} regulator

V_{CC} buffer is able to deliver up to 65 mA continuously at V_{CC} = 5 V and V_{CC} = 3 V, and 35 mA at V_{CC} = 1.8 V.

V_{CC} buffer has an internal overload detection at approximately 125 mA.

This detection is internally filtered, allowing the card to draw spurious current pulses of up to 200 mA for some milliseconds, without causing a deactivation. The average current value must remain below the maximum.

8.10 Fault detection

The circuit monitors the following fault conditions:

- short-circuit or high current on V_{CC}
- Card removal during transaction
- V_{DDP} or $V_{DD(INTF)}$ or V_{reg} dropping
- overheating.

There are two different cases (see Figure 10 on page 16):

1. CMDVCCN High (outside a card session): OFFN is Low when the card is not in the reader, and High when the card is in the reader. The supply supervisor detects a supply voltage drop on V_{DDP} and generates an internal power-on reset pulse, but it does not act upon OFFN. The card is not powered-up, so no short-circuit or overheating is detected.
2. CMDVCCN Low (within a card session): OFFN falls Low in any of the previously mentioned cases. As soon as the fault is detected, an emergency deactivation is automatically performed. When the system controller sets CMDVCCN back to High, it senses OFFN again. After a complete deactivation sequence, the system controller sets CMDVCCN back to High and it senses OFFN again. This is to distinguish between a hardware problem or a card extraction. OFFN reverts to High when the card is still present.

A bounce can occur on the PRESN signal during card insertion or withdrawal. The bounce depends on the type of card presence switch within the connector (normally closed or normally open), and on the mechanical characteristics of the switch. To prevent this bounce, a debounce function of approximately 4.05 ms (tdeb = 1280 $\times$ 1/($f_{osc(int)\_Low}$) is integrated in the device.

When the card is inserted, OFFN goes High only at the end of the debounce time (see Figure 11 on page 16).

When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRESN. OFFN goes Low.

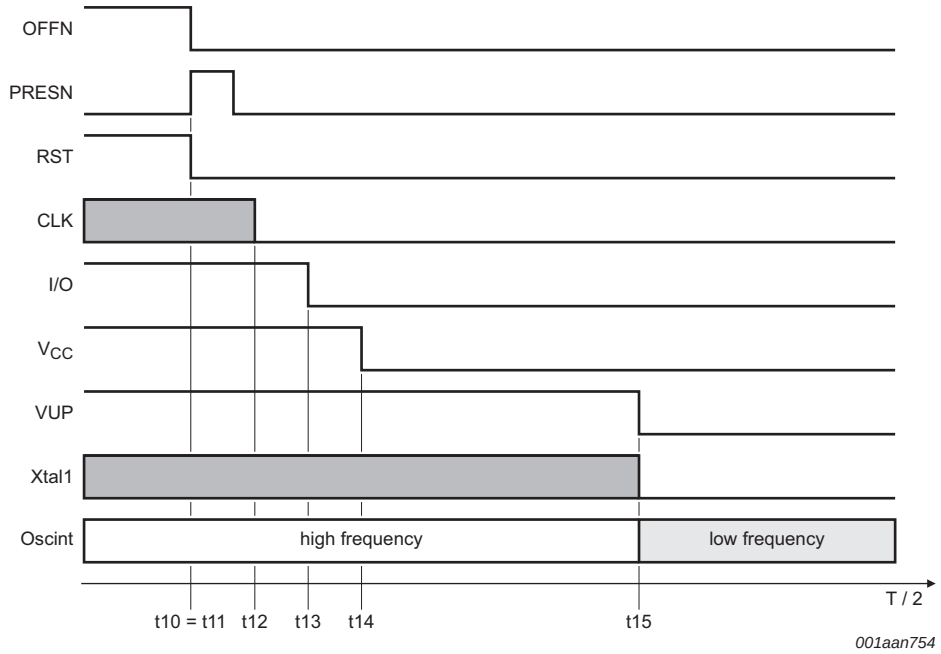


Fig 10. Emergency deactivation sequence (card extraction)

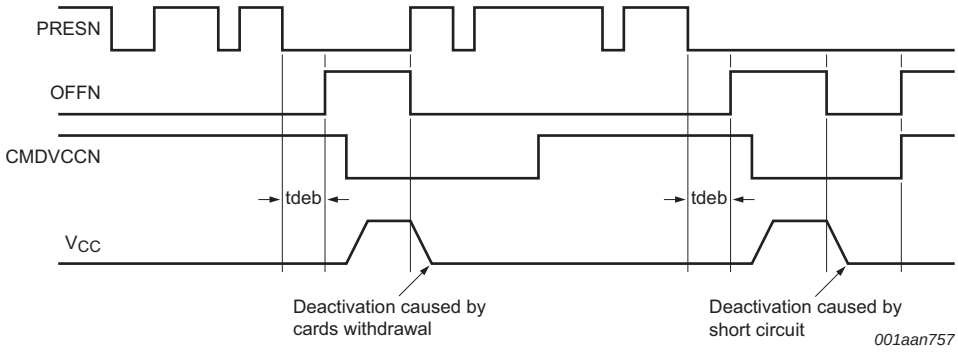


Fig 11. Behavior of OFFN, CMDVCCN, PRESN and V_{CC}

9. Limiting values

All card contacts are protected against a short-circuit with any other card contact.

Stress beyond the limiting values can damage the device permanently. The values are stress ratings only and functional operation of the device under these conditions is not implied.

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDP}	power supply voltage			–0.3	6	V
$V_{DD(INTF)}$	interface supply voltage			–0.3	4.1	V
V_{IH}	HIGH-level input voltage	CS, PRESN, $\overline{\text{CMDVCC}}$N, CLKDIV2, CLKDIV1, EN_1.8VN, EN_5V/3VN, RSTIN, OFFN, PORADJ, XTAL1, I/OUC, AUX1UC, AUX2UC, VDDP, VDD(INTF)		–0.3	4.1	V
		I/O, RST, AUX1, AUX2 and CLK		–0.3	5.75	V
T_{amb}	ambient temperature			–25	+85	°C
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature				+125	°C
P_{tot}	total power dissipation				0.45	W
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) on card pins I/O, RST, V_{CC}, AUX1, CLK, AUX2, PRESN within typical application		–10	+10	kV
		Human Body Model (HBM) on all other pins		–2	+2	kV
		Machine Model (MM) on all pins		–200	+200	V
		Field Charged Device Model (FCDM) on all pins		–500	+500	V

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Package name	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	HVQFN32	thermal resistance from junction to ambient	in free air with 4 thermal vias on PCB		55	K/W
			in free air without thermal vias on PCB		63	K/W

11. Characteristics

Table 7. Characteristics of IC

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{XTAL} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{DDP}	power supply voltage		2.7	3.3	5.5	V
$V_{DD(INTF)}$	interface supply voltage		1.6	3.3	3.6	V
I_{DDP}	power supply current	deep Shutdown mode; f_{XTAL} = stopped	-	0.1	3	µA
		Shutdown mode; f_{XTAL} = stopped	-	300	500	µA
		active mode; CLK = f_{XTAL}/2; V_{CC} = +5 V; no load	-	-	5	mA
		active mode; CLK = f_{XTAL}/2; V_{CC} = +5 V; I_{CC} = 65 mA	-	-	220	mA
		active mode; CLK = f_{XTAL}/2; V_{CC} = +3 V; I_{CC} = 65 mA	-	-	160	mA
		active mode; CLK = f_{XTAL}/2; V_{CC} = +1.8 V; I_{CC} = 35 mA	-	-	120	mA
$I_{DD(INTF)}$	interface supply current	deep Shutdown mode f_{XTAL} = stopped; present card	-	-	1	µA
		Shutdown mode f_{XTAL} = stopped; present card	-	-	1	µA
$V_{th(VREG)}$	threshold voltage on pin V_{REG}	internal voltage regulator falling	1.38	1.45	1.52	V
$V_{hys(VREG)}$	hysteresis voltage on pin V_{REG}		90	100	110	mV
$V_{th(VDDP)}$	threshold voltage on pin V_{DDP}	pin VDDP falling	2.15	2.25	2.35	V
$V_{hys(VDDP)}$	hysteresis voltage on pin V_{DDP}		90	100	110	mV
t_w	pulse width		3.0	6.5	8.9	ms
$V_{th(L)(PORADJ)}$	LOW-level threshold voltage on pin PORADJ	external resistors on PORADJ	0.81	0.85	0.89	V
$V_{hys(PORADJ)}$	hysteresis voltage on pin PORADJ		30	60	90	mV
I_L	leakage current	pin PORADJ	-1	-	+1	µA
VREG						
V_o	output voltage		1.62	1.80	1.98	V
t_r	rise time	exit of deep Shutdown mode	-	-	200	µs

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{XTAL} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VUP (DC-to-DC converter)						
V_{OH}	HIGH-level output voltage	VDDP=3.3V, VCC = 5 V, ICC < 65 mA DC	5.10	5.60	7.00	V
		VDDP=3.3V, VCC = 3 V, ICC < 65 mA DC	3.50	3.95	5.00	V
		VDDP=3.3V, VCC = 1.8 V, ICC < 35 mA DC	5.10	5.60	7.00	V
		VDDP=5V, VCC = 5 V, ICC < 65 mA DC	5.10	5.80	7.00	V
		VDDP=5V, VCC = 3 V, ICC < 65 mA DC	-	5.00	-	V
		VDDP=5V, VCC = 1.8 V, ICC < 35 mA DC	5.10	5.80	7.00	V
SAP (DC-to-DC converter)						
V_{OH}	HIGH-level output voltage	VDDP=3.3V, VCC = 5 V, ICC < 65 mA DC	-	-	8.20	V
		VDDP=3.3V, VCC = 3 V, ICC < 65 mA DC	-	-	6.00	V
		VDDP=3.3V, VCC = 1.8 V, ICC < 35 mA DC	-	-	8.20	V
		VDDP=5V, VCC = 5 V, ICC < 65 mA DC	-	-	8.20	V
		VDDP=5V, VCC = 3 V, ICC < 65 mA DC	-	5.00	-	V
		VDDP=5V, VCC = 1.8 V, ICC < 35 mA DC	-	-	8.20	V
DC-to-DC converter capacitors						
C_{SAPSAM}	DC/DC converter capacitance	connected between SAP and SAM (330 nF [4]) with VDDP=3.3v	231	-	429	nF
		connected between SAP and SAM (100 nF [4]) with VDDP=5v	70	-	130	nF
C_{SBPSBM}	DC/DC converter capacitance	connected between SBP and SBM (330 nF [4]) with VDDP=3.3v	231	-	429	nF
		connected between SBP and SBM (100 nF [4]) with VDDP=5v	70	-	130	nF
C_{VUP}	DC/DC converter capacitance	connected on VUP(1uF [4])	700	-	1300	nF
Card supply voltage (V_{CC})[1]						
C_{dec}	decoupling capacitance	connected on V_{CC} (220 nF + 220 nF 10 %)	396	-	484	nF
V_o	output voltage	inactive mode; no load	-0.1	-	+0.1	V
		inactive mode; Io = 1 mA	-0.1	-	+0.3	V

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{XTAL} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_o	output current	inactive mode at grounded pin VCC	-	-	−1	mA
V_{CC}	supply voltage	active mode; 5 V card; ICC < 65 mA DC	4.75	5.0	5.25	V
		active mode; 3 V card; ICC < 65 mA DC	2.85	3.05	3.15	V
		active mode; 1.8 V card; ICC < 35 mA DC	1.71	1.83	1.89	V
		active mode; current pulses of 40 nA/s with ICC < 200 mA, t < 400 ns; 5 V card	4.65	5.0	5.25	V
		active mode; current pulses of 40 nA/s with ICC < 200 mA, t < 400 ns; 3 V card	2.76	-	3.20	V
		active mode; current pulses of 15 nA/s with ICC < 200 mA, t < 400 ns; 1.8 V card	1.66	-	1.94	V
$V_{ripple(p-p)}$	peak-to-peak ripple voltage	from 20 kHz to 200 MHz	-	-	350	mV
I_{CC}	supply current	VCC = 0 V to 5 V, 3 V	-	-	65	mA
		VCC = 0 V to 1.8 V	-	-	35	mA
SR	slew rate	5 V card	0.055	0.18	0.8	V/µs
		3 V card	0.040	0.18	0.8	V/µs
		1.8 V card	0.025	0.18	0.8	V/µs
Crystal oscillator (XTAL1 and XTAL2)						
C_{ext}	external capacitance	connected on pins XTAL1/XTAL2 (depending on specification of crystal or resonator used)	-	-	33	pF
f_{xtal}	crystal frequency		2	-	27	MHz
$f_{xtal(XTAL1)}$	crystal frequency on pin XTAL1	with 56 pF serial capacitor	0	-	27	MHz
V_{IL}	LOW-level input voltage		-0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage		0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$+ 0.3	V
$t_{r(i)}$	input rise time	f_{CLK} = f_{XTAL1} = 20 MHz on external clock	-	-	4	ns
		f_{CLK} = f_{XTAL1} = 10 MHz on external clock	-	-	8	ns
		f_{CLK} = f_{XTAL1} = 5 MHz on external clock	-	-	16	ns

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{XTAL} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{f(i)}$	input fall time	f_{CLK} = f_{XTAL1} = 20 MHz on external clock	-	-	4	ns
		f_{CLK} = f_{XTAL1} = 10 MHz on external clock	-	-	8	ns
		f_{CLK} = f_{XTAL1} = 5 MHz on external clock	-	-	16	ns
Data lines (pins I/O, I/OUC, AUX1, AUX2, AUXIUC, AUX2UC)						
t_d	delay time	falling edge on pins I/O and I/OUC or I/OUC and I/O	-	-	200	ns
$t_{w(pu)}$	pull-up pulse width		200		400	ns
f_{max}	maximum frequency	on data lines	-	-	1	MHz
C_i	input capacitance	on data lines	-	-	10	pF
Data lines to the card (pins I/O, AUX1, AUX2); (Integrated 10 kΩ pull-up resistor connected to V_{CC})						
V_o	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; Io= 1 mA	0	-	0.3	V
I_o	output current	inactive mode at grounded pin I/O	-	-	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA - C1 version	0	-	0.3	V
		I_{OL} = 1 mA - C2 version	0	-	0.15 V_{CC}	V
		$I_{OL} \geq$ 15 mA	V_{CC} - 0.4	-	V_{CC}	V
V_{OH}	HIGH-level output voltage	No DC load	0.9 V_{CC}	-	V_{CC} + 0.1	V
		$I_{OH} \geq$ -15 mA	0	-	0.4	V
		C1 version				
		I_{OH} < -40 µA 5 V or 3 V	0.75 V_{CC}		V_{CC} + 0.1	V
		I_{OH} < -20 µA 1.8 V	0.75 V_{CC}		V_{CC} + 0.1	V
		C2 version				
		I_{OH} < -40 µA 5 V or 3 V	0.8 V_{CC}		V_{CC} + 0.1	V
		I_{OH} < -20 µA 1.8 V	1.28		V_{CC} + 0.1	V
V_{IL}	LOW-level input voltage	C1 version	–0.3	-	+0.8	V
		C2 version	-0.3		0.2 V_{CC}	
V_{IH}	HIGH-level input voltage	C1 Version				
		VCC = +5 V	0.6 V_{CC}	-	V_{CC} + 0.3	V
		VCC = +3 V or 1.8 V	0.7 V_{CC}	-	V_{CC} + 0.3	V
		C2 Version				
		VCC = +5 V or 3V	0.6 V_{CC}	-	V_{CC} + 0.3	V
		VCC =1.8 V	1.4	-	V_{CC} + 0.3	V
V_{hys}	hysteresis voltage	on I/O	30	75	120	mV
I_{IL}	LOW-level input current	on I/O; VIL = 0	-	-	600	µA
I_{LH}	HIGH-level leakage current	on I/O; V_{IH} = V_{CC}	-	-	10	µA
$t_{r(i)}$	input rise time	from V_{IL} max to V_{IH} min	-	-	1.2	µs

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{XTAL} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{f(i)}$	input fall time	from V_{IL} max to V_{IH} min	-	-	1.2	µs
$t_{r(o)}$	output rise time	C_L < = 80 pF; 10 % to 90 % from 0 to V_{CC}	-	-	0.1	µs
$t_{f(o)}$	output fall time	C_L < = 80 pF; 10 % to 90 % from 0 to V_{CC}	-	-	0.1	µs
R_{pu}	pull-up resistance	connected to VCC	8	10	12	kΩ
I_{pu}	pull-up current	V_{OH} = 0.9 V_{CC}, C = 80 pF	-8	-6	-4	mA
Data lines to the system; pins I/OµC, AUX1µC, AUX2µC (Integrated kΩ pull-up resistor to $V_{DD(INTF)}$)						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	-	0.3	V
V_{OH}	HIGH-level output voltage	No DC load	0.9 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.1	V
		$I_{OH} \leq$ 40 µA; $V_{DD(INTF)}$ >2 V	0.75 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$+ 0.1	V
		$I_{OH} \leq$ 20 µA; $V_{DD(INTF)}$ <2 V	0.75 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$+ 0.1	V
V_{IL}	LOW-level input voltage		–0.3	-	0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{hys}	hysteresis voltage	on I/Ouc	0.05 $V_{DD(INTF)}$	-	0.25 $V_{DD(INTF)}$	V
I_{LH}	HIGH-level leakage current	V_{IH} = $V_{DD(INTF)}$			10	µA
I_{IL}	LOW-level input current	V_{IL} = 0			600	µA
R_{pu}	pull-up resistance	connected to VDD(INTF)	8	10	12	kΩ
$t_{r(i)}$	input rise time	from V_{IL} max to V_{IH} min	-	-	1.2	µs
$t_{f(i)}$	input fall time	from V_{IL} max to V_{IH} min	-	-	1.2	µs
$t_{r(o)}$	output rise time	$C_L \leq$ 30 pF; 10 % to 90 % from 0 to $V_{DD(INTF)}$	-	-	0.1	µs
$t_{f(o)}$	output fall time	$C_L \leq$ 30 pF; 10 % to 90 % from 0 to $V_{DD(INTF)}$	-	-	0.1	µs
I_{pu}	pull-up current	V_{OH} = 0.9 V_{DD}, C = 30 pF	-1	-	-	mA
Internal oscillator						
$f_{osc(int)}$	internal oscillator frequency	inactive state: osc(int)_Low	230	315	430	kHz
		active state: osc(int)_High	2.0	2.5	3.0	MHz
Reset output to the card (RST)						
V_o	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; Io= 1 mA	0	-	0.3	V
I_o	output current	inactive mode at grounded pin RST	-	-	–1	mA
t_d	delay time	between RSTIN and RST, RST enabled	-	-	200	ns
V_{OL}	LOW-level output voltage	I_{OL}= 200 µA, VCC = +5 V	0	-	0.3	V
		I_{OL}= 200 µA, VCC = +3 V or 1.8 V	0	-	0.2	V
		I_{OL} = 20 mA (current limit)	V_{CC} - 0.4	-	V_{CC}	V

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{XTAL} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = -200 µA	0.9 V_{CC}	-	V_{CC}	V
		I_{OH} = -20 mA (current limit)	0	-	0.4	V
t_r	rise time	C_L = 100 pF V_{CC} = +5 V and +3 V	-	-	0.1	µs
		C_L = 100 pF V_{CC} = +18 V	-	-	0.2	µs
t_f	fall time	C_L = 100 pF V_{CC} = +5 V and +3 V	-	-	0.1	µs
		C_L = 100 pF V_{CC} = +18 V	-	-	0.2	µs
Clock output to the card (CLK)						
V_o	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; I_o = 1 mA	0	-	0.3	V
I_o	output current	inactive mode at grounded pin CLK	-	-	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 70 mA (current limit)	V_{CC} - 0.4	-	V_{CC}	V
		C1 version				
		I_{OL} = 200 µA	0	-	0.3	V
		C2 Version				
		I_{OL} = 200 µA	0	-	0.15 V_{CC}	V
V_{OH}	HIGH-level output voltage	I_{OH} = -200 µA	0.9 V_{CC}	-	V_{CC}	V
		I_{OH} = -70 mA (current limit)	0	-	0.4	V
t_r	rise time	C_L = 30 pF [2]	-	-	16	ns
t_f	fall time	C_L = 30 pF [2]	-	-	16	ns
f_{CLK}	frequency on pin CLK	operational	0	-	20	MHz
	duty cycle	C_L = 30 pF [2]	45	-	55	%
SR	slew rate	rise and fall; C_L = 30 pF; VCC = +5 V	0.2	-	-	V/ns
		rise and fall; C_L = 30 pF; VCC = +3 V	0.12	-	-	V/ns
		rise and fall; C_L = 30 pF; VCC = +1.8 V	0.072	-	-	V/ns
Control inputs (pins CS, CMDVCCN, CLKDIV1, CLKDIV2, RSTIN, EN_5V/ 3VN, EN_1.8VN) [3]						
V_{IL}	LOW-level input voltage		–0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage		0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
V_{hys}	hysteresis voltage	on control input	0.05 $V_{DD(INTF)}$	-	0.25 $V_{DD(INTF)}$	V
I_{LL}	LOW-level leakage current	V_{IL} = 0	-	-	1	µA
I_{LH}	HIGH-level leakage current	V_{IH} = $V_{DD(INTF)}$	-	-	1	µA
Card presence input (PRESN); PRESN has an integrated pull down resistor [3]						
V_{IL}	LOW-level input voltage		–0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage		0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$+ 0.3	V

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{XTAL} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hys}	hysteresis voltage		0.05 $V_{DD(INTF)}$	-	0.10 $V_{DD(INTF)}$	V
I_{LL}	LOW-level leakage current	V_{IL} = 0	-	-	1	µA
I_{LH}	HIGH-level leakage current	V_{IH} = $V_{DD(INTF)}$	-	-	5	µA
OFFN output (pin OFFN is an NMOS drain with a kΩ pull-up resistor to $V_{DD(INTF)}$)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	-	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = -15 µA	0.75 $V_{DD(INTF)}$	-		V
R_{pu}	pull-up resistance		8	10	12	kΩ
Protections and limitations						
T_{sd}	shutdown temperature	at die	-	150	-	°C
I_{Olim}	output current limit	on pin I/O	-15	-	+15	mA
		on pin CLK	-70	-	+70	mA
		on pin RST	-20	-	+20	mA
		on pin VCC = 5 V or 1.8 V	90	125	160	mA
		on pin VCC = 3 V	90	160	260	mA
I_{sd}	shutdown current	on pin VCC = 5 V or 1.8 V	80	115	150	mA
		on pin VCC = 3 V	80	150	250	mA
Timing						
t_{act}	activation time	see Figure 8 on page 13	1847	-	3390	µs
t_{deact}	deactivation time	see Figure 9 on page 14	35	90	250	µs
t_{act}	activation time	time of the window for sending CLK to the card with XTAL1	1992	2690	3653	µs
		$t_{act(start)}$ = t3; see Figure 8 on page 13 $t_{act(end)}$ = t5; see Figure 8 on page 13	2055	2766	3749	µs
t_{deb}	debounce time	on pin PRESN	2.96	4.05	5.55	ms

[1] To meet these specifications, VCC is decoupled to CGND using two ceramic multilayer capacitors of low ESR with both capacitors having a value of 220 nF.

[2] The transition time and the duty factor definitions are shown in Figure 12 on page 25; d = t1/(t1+ t2)

[3] PRESN and CMDVCCN are active LOW; RSTIN is active HIGH; for CLKDIV1 and CLKDIV2 see Table 4.

[4] Capacitance should not vary more than +- 30% compared to nominal value, taking all parameters into account (temperature, process variation, biasing voltage, etc. Non exhaustive list)

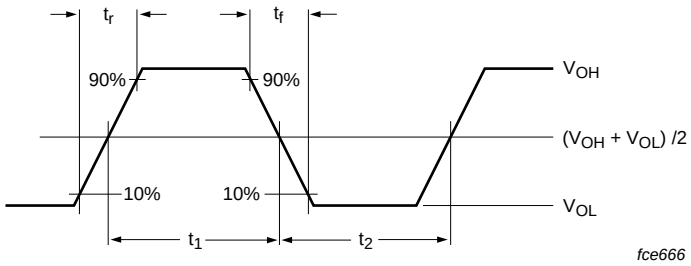
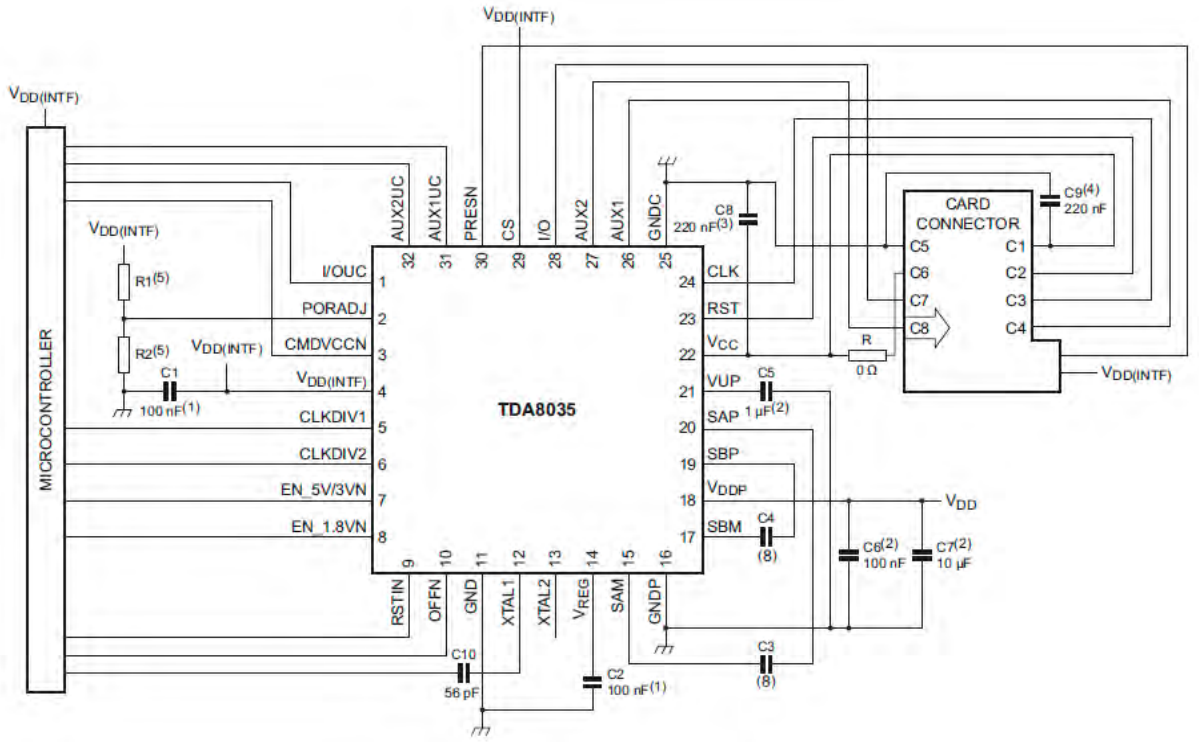


Fig 12. Definition of output and input transition times

12. Application information



(1) Place close to the protected pin with good (low resistive) and straight connection to the main ground

(2) Place close to the supply pin with good (low resistive) and straight connection to GNDP

(3) Place close to TDA8035´s VCC pin with good connection to GNDC

(4) Place close to card connector´s C1 (VCC) pin with good connection to GNDC

(5) Optional bridge. If not used, R1 must be O Ω and R2 absent (direct connection to $V_{DD(INTF)}$)

(6) GNDP and GNDC are connected to the main ground with a straight and low resistive connection

(7) The card connector represented here has a normally closed presence switch

(8) DC/DC converter capacitance value:

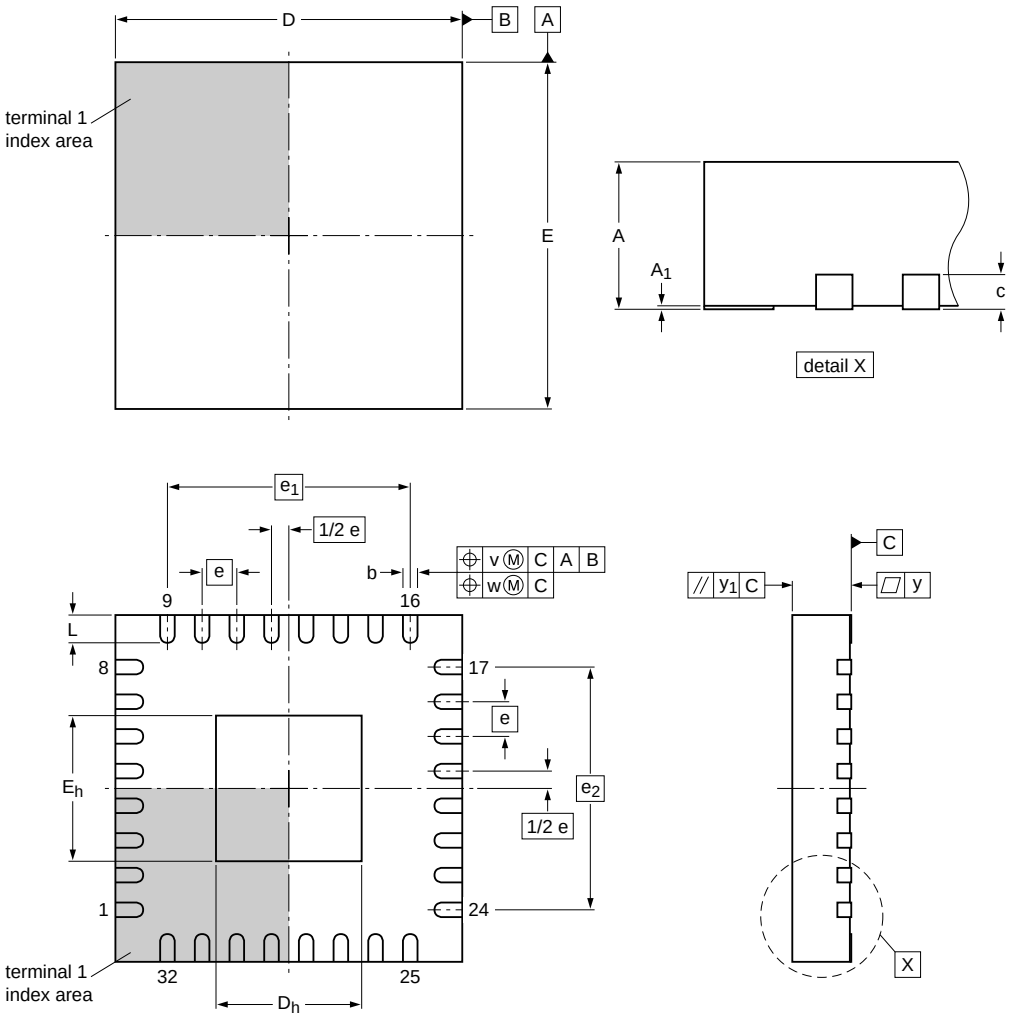
If VDDP=3.3v, C3=C4= 330nF & C5=1uF

If VDDP=5.0v, C3=C4= 100nF & C5=1uF

Fig 13. Application diagram

13. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-7**



Dimensions

Unit		A	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		5.1	2.2	5.1	2.2				0.5				
mm	nom	0.85	0.02	0.21	0.2	5.0	2.1	5.0	2.1	0.5	3.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.9	2.0	4.9	2.0				0.3				

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot617-7_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-7		- - -	- - -			~~10-02-08~~ 10-02-09

Fig 14. Package outline SOT617-7

14. Soldering

For all "Surface mount reflow soldering" information for the SOT617 packaging, utilize the following NXP Semiconductors documentation link:
http://www.nxp.com/documents/application_note/AN10365.pdf

15. Abbreviations

Table 8. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge

16. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8035HN v. 3.1	20160630	Product data sheet	-	TDA8035HN v. 3.0
Modifications	• Addition of C2 Version - EMVCo 4.3 compliant • Table 7 “Characteristics of IC”; updated			
TDA8035HN v. 3.0	20140625	Product data sheet	-	TDA8035HN v. 2.1
Modifications:	• Section 5 “Ordering information”: type TDA8035HN/C1/S1 added • Descriptive title changed			
TDA8035HN v. 2.1	20121203	Product data sheet	-	TDA8035HN v. 2.0
Modifications:	• Table 3 “Pin description”: updated • Section 8.1 “Power supply”: updated • Table 7 “Characteristics of IC”: updated • Figure 13 “Application diagram”: Table note (7) added			
TDA8035HN v. 2.0	20111220	Product data sheet	-	TDA8035HN v. 1.1
Modifications:	• All text updated to NXP standards			
TDA8035HN v. 1.1	20110706	Product data sheet	-	TDA8035HN v. 1.0
Modifications:	• Table 7 “Characteristics of IC”: $V_{th(L)(PORADJ)}$ values updated			
TDA8035HN v. 1.0	20110419	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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19. Tables

20. Figures

21. Contents

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