GOODWORK

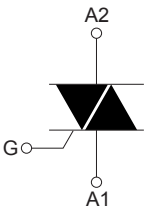
BTA12, BTB12, T1205
T1210, T1235, T1250

12 A Snubberless™, logic level and standard Triacs

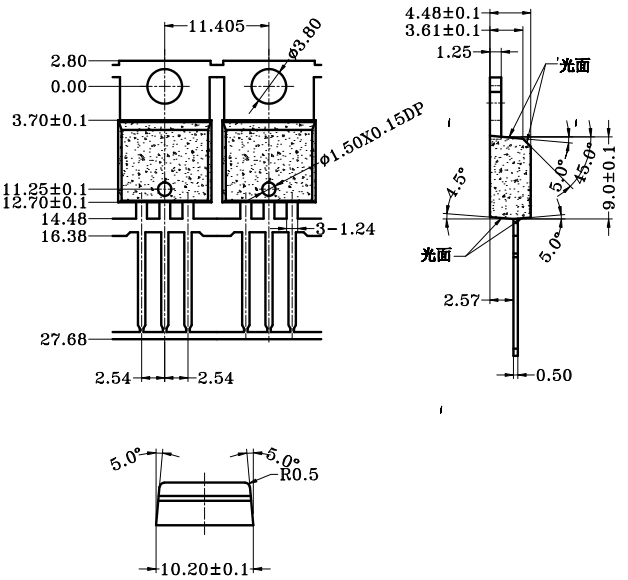
Features

Medium current Triac
Low thermal resistance with clip bonding
Low thermal resistance insulation ceramic for insulated BTA
High commutation (4Q) or very high commutation
(3Q, Snubberless™) capability

BTA series UL1557 certified (file ref: 81734)
Packages are RoHS (2002/95/EC) compliant
nsulated tab (BTA series, rated at 2500 V_{RMS})



TO-220



MAXIMUM RATINGS AND ELECTRICAL CHARA CTERISTICS

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise specified)

Symbol	Parameter			Value	Unit
V_{DRM}	Repetitive peak off-state voltage			600 / 800	V
V_{RRM}	Repetitive peak reverse voltage			600 / 800	V
$I_{T(RMS)}$	RMS on-state current (full sine wave)	TO-220AB, D²PAK	T_c = 105 °C	12	A
		TO-220AB Ins.	T_c = 90 °C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C)	f = 50 Hz	t = 20 ms	120	A
		f = 60 Hz	t_p = 16.7 ms	126	
I^2t	I^2t value for fusing		t_p = 10 ms	78	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT}, tr ≤ 100 ns	f = 120 Hz	T_j = 125 °C	50	A/µs
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25 °C	V_{DRM} / V_{RRM} + 100	V
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125 °C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125 °C	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +125	°C

Electrical characteristics (T_j = 25 °C, unless otherwise specified) - standard (4 quadrants)

Symbol	Parameter	Quadrant		Value		Unit
				C	B	
I_{GT} (1)	V_D = 12 V, R_L = 30 Ω	I - II - III	Max.	25	50	mA
		IV		50	100	
V_{GT}		All	Max.	1.3		V
V_{GD}	V_D = V_{DRM}, R_L = 33 kΩ, T_j = 125 °C	All	Min.	0.2		V
I_H (2)	I_T = 500 mA	I - II - III	Max.	25	50	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	Max.	40	50	mA
		II		80	100	
dV/dt (2)	V_D = 67 % V_{DRM} gate open, T_j = 125 °C		Min.	200	400	V/µs
(dV/dt)c (2)	(dI/dt)c = 5.3 A/ms, T_j = 125 °C		Min.	5	10	V/µs

1. *Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.*
2. *For both polarities of A2 referenced to A1*

Electrical characteristics (T_j = 25 °C, unless otherwise specified - Snubberless and logic level (3 quadrants)

Symbol	Parameter	Quadrant		T1205 BTB12-TW BTA12-TW	T1210 BTB12-SW BTA12-SW	T1235 BTB12-CW BTA12-CW	T1250 BTB12-BW BTA12-BW	Unit
I_{GT} (1)	V_D = 12 V, R_L = 30 Ω	I - II - III	Max.	5	10	35	50	mA
V_{GT}		I - II - III	Max.	1.3				V
V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ, T_j = 125 °C	I - II - III	Min.	0.2				V
I_H (2)	I_T = 100 mA	I - II - III	Max.	10	15	35	50	mA
I_L (2)	I_G = 1.2 x I_{GT}	I - III	Max.	10	25	50	70	mA
		II	Max.	15	30	60	80	
dV/dt (2)	V_D = 67% V_{DRM}, gate open, T_j = 125 °C		Max.	20	40	500	1000	V/µs
(dI/dt)c (2)	(dV/dt)c = 0.1 V/µs, T_j = 125 °C		Min.	3.5	6.5			A/ms
	(dV/dt)c = 10 V/µs, T_j = 125 °C		Min.	1.0	2.9			
	Without snubber, T_j = 125 °C		Min.			6.5	12	

1. *Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.*
2. *For both polarities of A2 referenced to A1*

Static electrical characteristics

Symbol	Test conditions			Value	Unit
V_{TM} (1)	I_{TM} = 17 A, t_p = 380 µs	T_j = 25 °C	Max.	1.55	V
V_{TO}(1)	threshold on-state voltage	T_j = 125 °C	Max.	0.85	V
R_D(1)	Dynamic resistance	T_j = 125 °C	Max.	35	mΩ
I_{DRM} I_{RRM}	V_{DRM} = V_{RRM}	T_j = 25 °C	Max.	5	µA
		T_j = 125 °C	Max.	1	mA

1. For both polarities of A2 referenced to A1

Thermal resistance

Symbol	Parameter				Value	Unit
$R_{th(j-c)}$	Max. junction to case thermal resistance (AC)		D^2PAK / TO-220AB	Max.	1.4	°C/W
			TO-220AB insulated	Max.	2.3	
$R_{th(j-a)}$	Junction to ambient	S = 2 cm² (1)	D²PAK	Typ.	45	°C/W
	Junction to ambient		TO-220AB / TO-220AB insulated	Typ.	60	

1. S = Copper surface under tab.

RATING AND CHARACTERISTIC CURVES (BTA12,BTB12,T1205,T1210,T1235,T1250)

Figure 1. Maximum power dissipation versus on-state RMS current (full cycle)

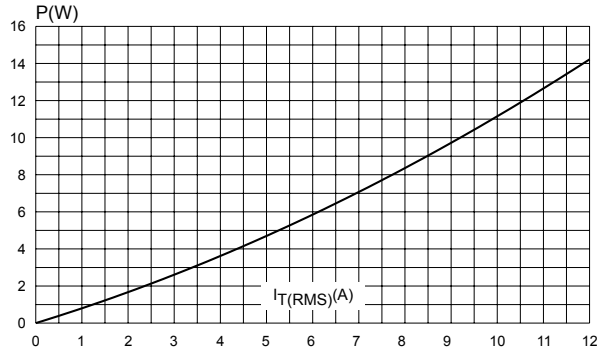


Figure 2. RMS on-state current versus case temperature (full cycle)

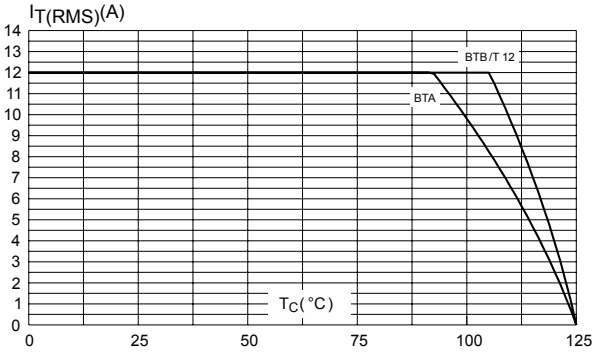


Figure 3. RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35 µm) (full cycle)

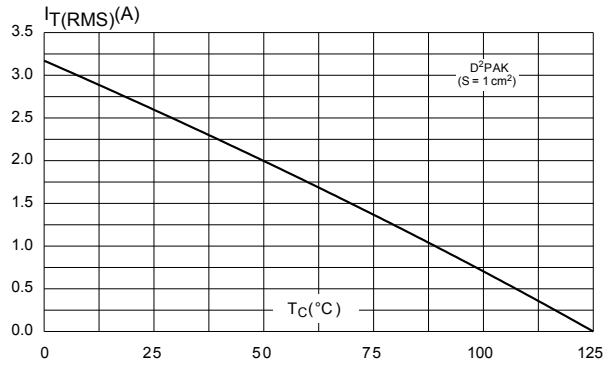


Figure 4. Relative variation of thermal impedance versus pulse duration

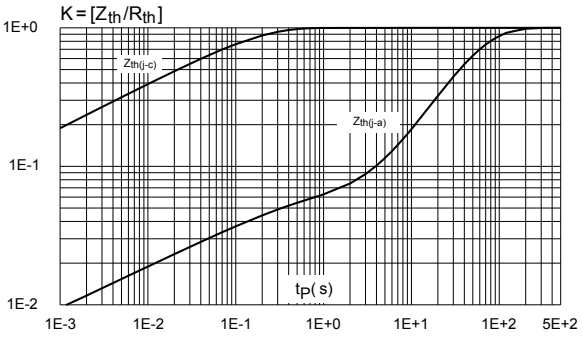


Figure 5. On-state characteristics (maximum values)

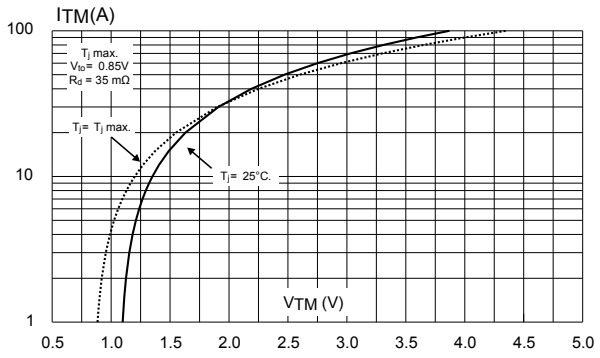


Figure 6. Surge peak on-state current versus number of cycles

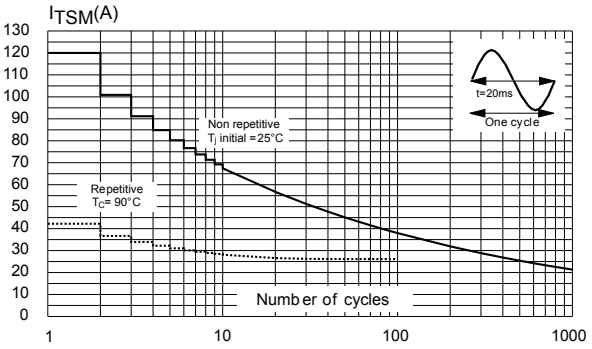


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse

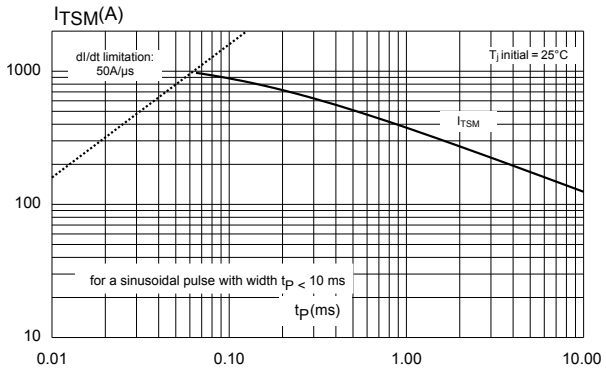


Figure 8. Relative variation of gate trigger current holding current and latching current versus junction temperature (typical values)

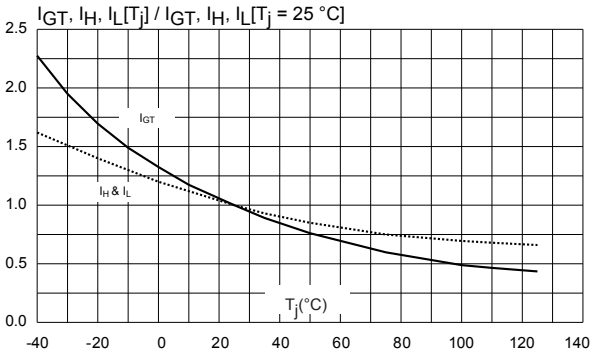


Figure 9. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

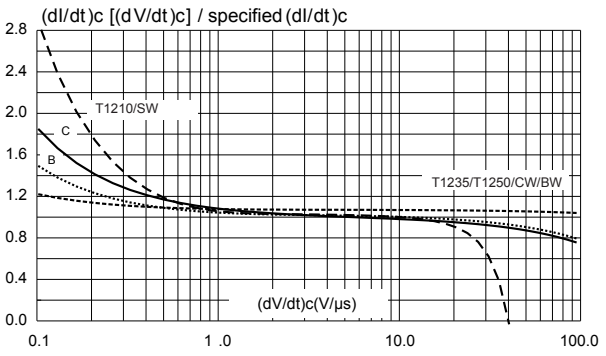


Figure 10. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)(TW)

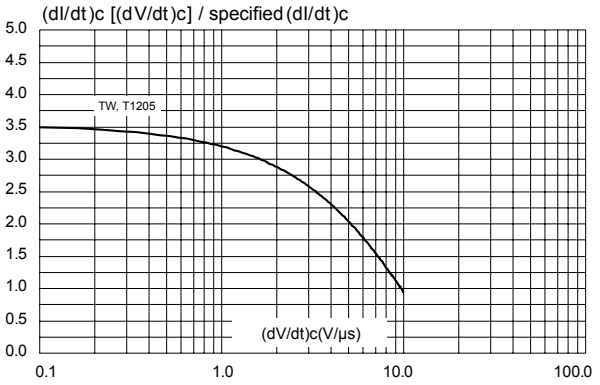


Figure 11. Relative variation of critical rate of decrease of main current versus junction temperature

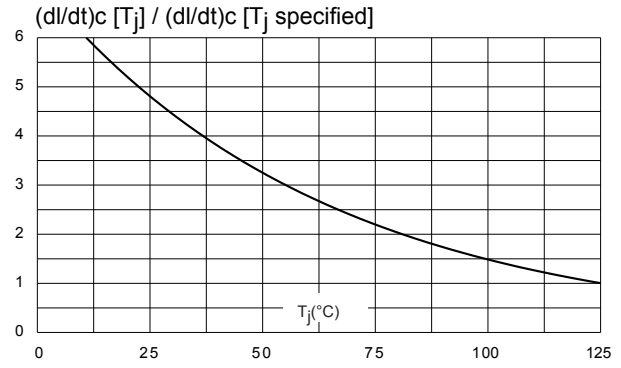


Figure 12. D²PAK thermal resistance junction to ambient versus copper surface under tab