TSW14DL3200 High-Speed LVDS Data Capture and Pattern Generator User's Guide

This user's guide describes the characteristics, operation, and use of the TSW14DL3200EVM high-speed data LVDS capture and pattern generator card. Throughout this user's guide, the abbreviation *EVM* and the term *evaluation module* are synonymous with the *TSW14DL3200EVM*, unless otherwise noted.

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1 Introduction

The TI TSW14DL3200 evaluation module (EVM) is a next-generation pattern generator and data capture card used to evaluate performances of the high-speed TI device family of high-speed low-voltage differential signaling (LVDS) analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). For an ADC, the TSW14DL3200 can be used to demonstrate datasheet performance specifications by capturing the sampled data over a wide LVDS interface when using a high-quality, low-jitter clock and a high-quality input frequency. Using Xilinx® IP cores, the TSW14DL3200 can be used to capture up to 48 pairs of high-speed LVDS signals or to provide up to 48 pairs of LVDS data. Together with the accompanying high-speed data converter pro graphic user interface (GUI), the TSW14DL3200EVM is a complete system that captures and evaluates data samples from ADC EVMs and generates and sends desired test patterns to DAC EVMs.

2 Functionality

The TSW14DL3200EVM has two industry-standard FMC connectors that interfaces directly with new TI high-speed LVDS ADC and DAC EVMs. When used with an ADC EVM, high-speed serial data are captured and formatted by an Xilinx Ultra-Scale® XCKU060 field-programmable gate array (FPGA). The data is then stored into internal FPGA memory, enabling the TSW14DL3200 to store up to 1M 16-bit data samples. To acquire data on a host PC, the FPGA transmits the data on a high-speed, 16-bit parallel interface. An onboard high-speed USB 3.0 to parallel converter bridges the FPGA interface to the host PC and GUI.

In pattern generator mode, the TSW14DL3200 generates desired test patterns up to 1M 16-bit samples for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14DL3200. The FPGA stores the data received into internal memory. The data from memory is then read by the FPGA and transmitted to a DAC EVM across the FMC interface connector. The board contains a 100-MHz oscillator used as a reference clock for the USB3.0 controller and a 125-MHz oscillator for the Xilinx Vivado HSSIO IPs. Figure 1 depicts the TI TSW14DL3200 evaluation module.

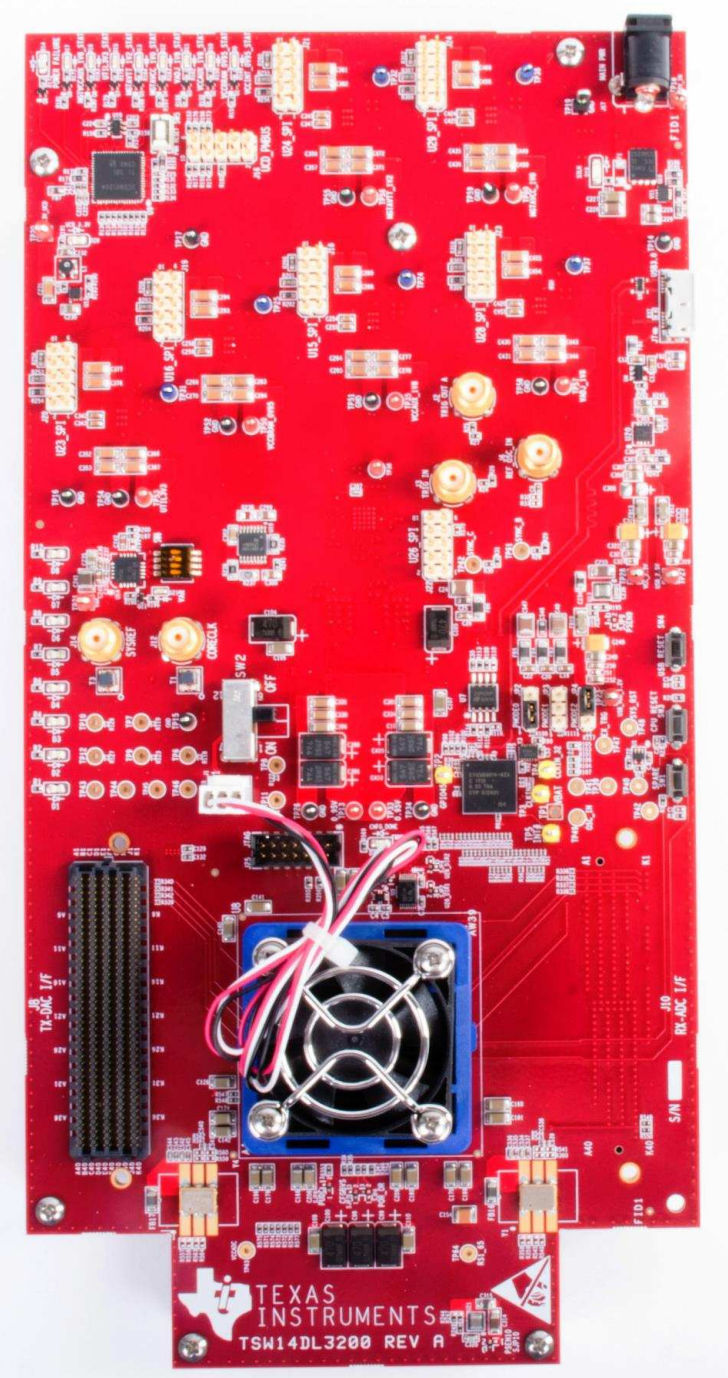

Figure 1. TSW14DL3200EVM

The major features of the TSW14DL3200 are:

- Serial LVDS speeds up to 1.6 Gbps
- 48 routed receive LVDS pairs
- 48 routed transmit LVDS pairs
- 1M of 16-bit samples of onboard memory
- Onboard UCD90120A for power sequencing and monitoring
- Onboard Cypress™ CYUSB301X USB 3.0 device for JTAG and parallel interface to the FPGA

- Reference clocking for transceivers available through FMC port or SMAs
- Supported by TI HSDC PRO software
- FPGA firmware developed with Vivado® 2017.1
  - IP core with support for:
    - USB interface
    - I/O delay

Figure 2 shows a block diagram of the TSW14DL3200EVM.

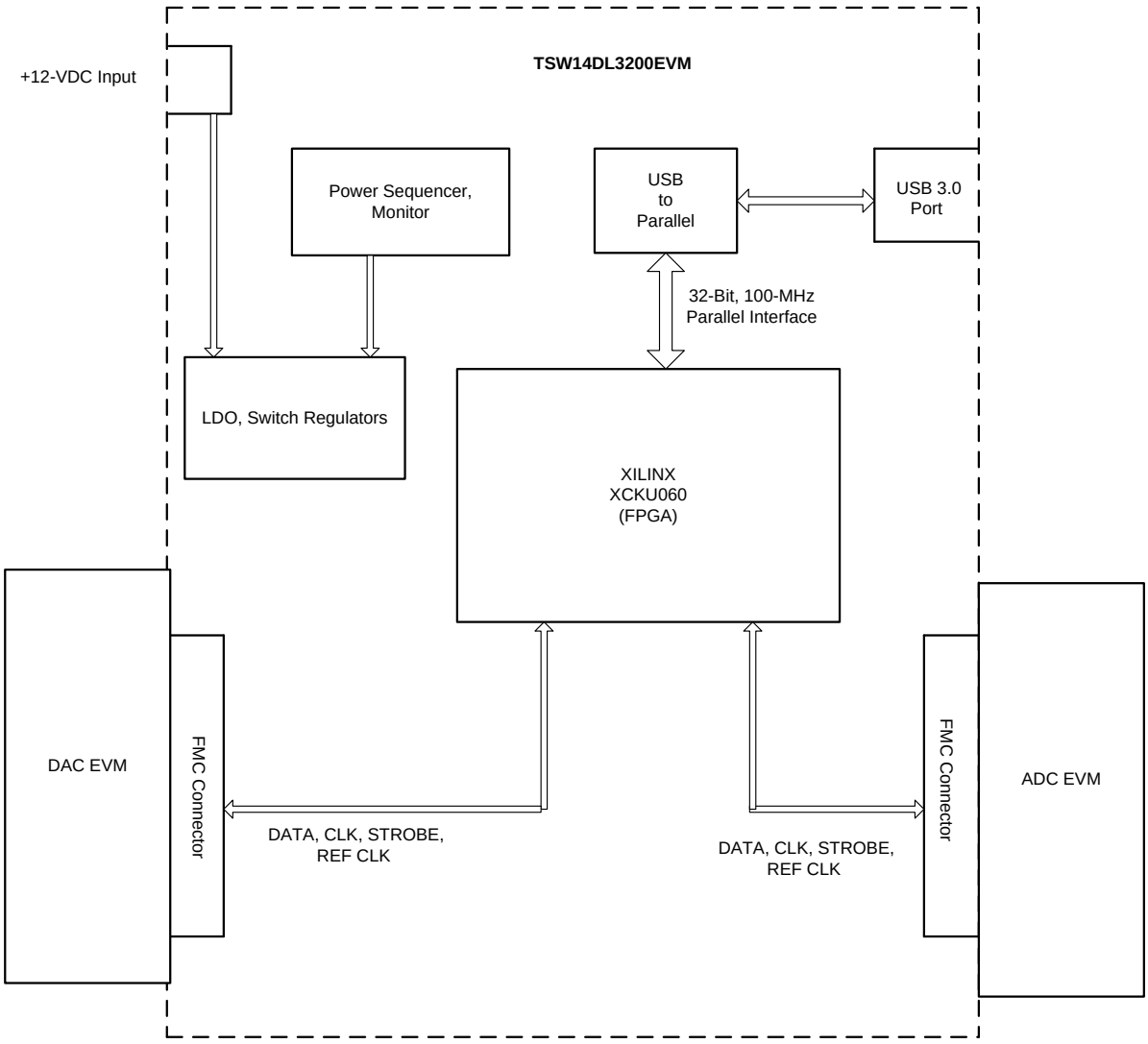

Figure 2. TSW14DL3200EVM Block Diagram

2.1 ADC EVM Data Capture

New TI high-speed ADCs and DACs have high-speed, wide-bus serial data interface. These devices are generally available on an EVM that connects directly to the TSW14DL3200EVM. The common connector between the EVMs and the TSW14DL3200EVM is a Samtec™ high-speed, high-density FMC connector (SEAF-40-05.0-S-10-2-A-K) suitable for high-speed differential pairs up to 28 Gbps. At present, the interface between the EVMs and the TSW14DL3200EVM has defined connections for 48 transmit LVDS pairs, 48 receive LVDS pairs, eight single-ended CMOS signals, four TX clocks and strobes, four RX clocks and strobes, and two LVDS FPGA clocks. The board has five spare SMA interfaces to the FPGA, a pushbutton switch, several spare test points routed to the FPGA, and eight status LEDs.

The data format for the ADCs and DACs is a 48-bit parallel format. The firmware in the FPGA on the TSW14DL3200 only supports either a TI ADC or DAC at one time.

The GUI loads the FPGA with the appropriate firmware based on the ADC or DAC device selected in the device drop-down window. Each ADC device that appears in this window has an associated initialization file (.ini) . This .ini file contains information, such as maximum sample rate, number of channels, number of bits, and other parameters. This information is loaded into the FPGA registers after the user clicks on the capture button. After the parameters are loaded, valid data is then captured into the FPGA internal memory. See the *High-Speed Data Capture Pro GUI Software User's Guide* and the ADC EVM User's Guide for more information.

The TSW14DL3200 device can capture up to 1M 16-bit samples at a maximum data rate of 1.6 Gbps that are stored inside the internal memory. To acquire data on a host PC, the FPGA reads the data from memory and transmits parallel data to the onboard high-speed parallel-to-USB converter.

2.2 DAC EVM Pattern Generator

In pattern generator mode, the TSW14DL3200EVM generates desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14DL3200. The FPGA stores the data received into the internal memory. The data from the memory is then read by the FPGA, then transmitted to a DAC EVM. The TSW14DL3200 can generate patterns up to 1M 16-bit samples at a data rate up to 1.6 Gbps.

The GUI comes with several existing test patterns that can be download immediately. The GUI also has a pattern generation tool that allows the user to generate a custom pattern, then download that pattern to the memory. See the *High-Speed Data Capture Pro Software User's Guide* for more information. Like the ADC capture mode, the DAC pattern generator mode uses .ini files to load predetermined interface information to the FPGA.

3 Hardware Configuration

This section describes the various portions of the TSW14DL3200EVM hardware.

3.1 Power Connections

The TSW14DL3200EVM hardware is designed to operate from a single-supply voltage of 12 V DC. The power input is controlled by the on and off switch, SW2. Make sure this switch is in the off position before inserting the provided power cable. Insert the connector end of the power cable into J17 of the EVM. Connect the positive red wire end of the power cable to the 12 V DC output of a power supply rated for at least 3 A. Connect the negative black wire to the return or GND of the power supply. The board can also be powered up by providing 12 V DC to the red test point, TP18, and the return to any black GND test point. As an example, the TSW14DL3200 draws approximately 0.4 A at power-up and 0.6 A steady state current when capturing 48 lanes of data from an ADC12DL3200EVM at a data rate of 1.6 Gpbs.

NOTE: The typical power-supply range for the TSW14DL3200EVM is between 10 V to 14 V with a power consumption of approximately 7.2 W. TI recommends that at least a 3-A rated supply be provided to the TSW14DL3200EVM because of the current consumption increase when data are being captured by HSDC Pro.

3.2 Switches, Jumpers, and LEDs

3.2.1 Switches and Pushbuttons

The TSW14DL3200 contains several switches and pushbuttons that enable certain functions on the board. Table 1 describes these switches.

Table 1. Switch Description of the TSW14DL3200 Device

Component	Description
SW1	Spare pushbutton that is connected to a spare FPGA input
SW2	Board main power switch
SW3 (CPU reset)	FPGA hardware reset
SW4	USB reset
SW5 (UCD reset)	Power monitor U9 reset
SW6	Dip switch to set VAR adjustable step-down output voltage. Default is 1.8 V (switches 1, 3, and 4 are off, 2 is on).

3.2.2 Jumpers

The TSW14DL3200 contains several jumpers (JP) that enable certain functions on the board. Table 2 describes these jumpers.

Table 2. Jumper Description of the TSW14DL3200 Device

Component	Description	Default
JP2	Programming mode for USB controller U8A	1 to 2
JP3	Programming mode for USB controller U8A	Open
JP4	Programming mode for USB controller U8A	2 to 3

3.3 LEDs

3.3.1 Power and Configuration LEDs

Several LEDs are on the TSW14DL3200EVM to indicate the presence of power and the state of the FPGA. Table 3 describes these LEDs.

Table 3. Power and Configuration LED Description of the TSW14DL3200 Device

Component	Description
D22	On after FPGA completes configuration
D9	On if VCCINT_0.95V_STAT are within specification
D10	On if VCCBRAM_0.95V_STAT are within specification
D11	On if USB_1.2V_STAT are within specification
D12	On if VADJ_1.8V_STAT are within specification
D13	On if MGTAVCC_1.0V_STAT are within specification
D14	On if power monitor device indicates that a power net is out of tolerance
D15	On if MGTAVTT_1.2V_STAT are within specification
D16	On if UTIL3.3V_STAT are within specification
D17	On if MGTVCCAUX_1.8V_STAT are within specification
D19	On if a 12-V board power is present
D20	On if 3.3 V is being provided for the power-supply sequencer
D21	On if VAR power is present

3.3.2 Status LEDs

Eight status LEDs on the TSW14DL3200EVM indicate the status of the FPGA and LVDs interface:

D1 – In ADC mode, indicates presence of rx_sync. In DAC mode, indicates the status of the onboard_mmcm_locked signal.

D2 – In ADC mode, indicates the status of rx_rst_done. In DAC mode, indicates the status of the dacclk_mmcm_locked signal.

D3 – In DAC mode, indicates the status of the tx_rst_done signal.

D4 – In DAC mode, indicates the status of the generate signal.

D5 – In DAC mode, indicates data are valid.

D6 – Not used

D7 – Not used

D8 – Not used

3.3.3 Connectors

3.3.3.1 SMA Connectors

The TSW14DL3200 has five SMA connectors. Table 4 defines these connectors.

Table 4. Connector Description of the TSW14DL3200 Device

Component	Connector	Description
J3	TRIG_IN	Adjustable level CMOS trigger input. Default level is 1.8 V.
J2	TRIG_OUT_A	Adjustable level CMOS trigger output. Default level is 1.8 V.
J6	REF_OSC	Adjustable level CMOS oscillator input. Default level is 1.8 V.
J12	CORE_CLK	Spare CORE CLK input
J14	SYSREF1	Spare SYSREF input

3.3.3.2 FPGA Mezzanine Card (FMC) Connector

The TSW14DL3200EVM has one connector to allow for the direct plug in of TI serial interface ADC EVMs and one for the DAC EVMs. FMC connector J10 provides the interface between the TSW14DL3200EVM and the ADC EVM under test. FMC connector J8 provides the interface between the TSW12DL3200EVM and the DAC EVM under test. These 400-pin Samtec high-speed, high-density connectors (part number SEAF-40-05.0-S-10-A-K) are suitable for high-speed differential pairs up to 28 Gbps.

In addition to the LVDS differential signals, several CMOS single-ended signals are connected between the FMC and FPGA. Table 5 describes the connector pinout.

Table 5. FMC Connector J10 Description of the TSW14DL3200 Device: Receive Data

FMC Signal Name	FMC Pin	Description
LRX0_P, LRX0_N	A11 and A10	LVDS receiver data from the ADC
LRX1_P, LRX1_N	A8 and A7	LVDS receiver data from the ADC
LRX2_P, LRX2_N	A4 and A5	LVDS receiver data from the ADC
LRX3_P, LRX3_N	A1 and A2	LVDS receiver data from the ADC
LRX4_P, LRX4_N	C7 and C8	LVDS receiver data from the ADC
LRX5_P, LRX5_N	C5 and C4	LVDS receiver data from the ADC
LRX6_P, LRX6_N	C11 and C10	LVDS receiver data from the ADC
LRX7_P, LRX7_N	C20 and C19	LVDS receiver data from the ADC
LRX8_P, LRX8_N	C17 and C16	LVDS receiver data from the ADC
LRX9_P, LRX9_N	A14 and A13	LVDS receiver data from the ADC
LRX10_P, LRX10_N	C14 and C13	LVDS receiver data from the ADC
LRX11_P, LRX11_N	C1 and C2	LVDS receiver data from the ADC
LRX12_P, LRX12_N	B21 and B22	LVDS receiver data from the ADC
LRX13_P, LRX13_N	B25 and B24	LVDS receiver data from the ADC
LRX14_P, LRX14_N	B27 and B28	LVDS receiver data from the ADC
LRX15_P, LRX15_N	B31 and B30	LVDS receiver data from the ADC
LRX16_P, LRX16_N	B34 and B33	LVDS receiver data from the ADC
LRX17_P, LRX17_N	D21 and D22	LVDS receiver data from the ADC
LRX18_P, LRX18_N	D24 and D25	LVDS receiver data from the ADC
LRX19_P, LRX19_N	D27 and D28	LVDS receiver data from the ADC
LRX20_P, LRX20_N	K8 and K7	LVDS receiver data from the ADC
LRX21_P, LRX21_N	D34 and D33	LVDS receiver data from the ADC
LRX22_P, LRX22_N	D37 and D36	LVDS receiver data from the ADC
LRX23_P, LRX23_N	K17 and K16	LVDS receiver data from the ADC
LRX24_P, LRX24_N	E1 and E2	LVDS receiver data from the ADC
LRX25_P, LRX25_N	E4 and E5	LVDS receiver data from the ADC
LRX26_P, LRX26_N	E8 and E7	LVDS receiver data from the ADC
LRX27_P, LRX27_N	E11 and E10	LVDS receiver data from the ADC
LRX28_P, LRX28_N	E13 and E14	LVDS receiver data from the ADC
LRX29_P, LRX29_N	K1 and K2	LVDS receiver data from the ADC
LRX30_P, LRX30_N	G4 and G5	LVDS receiver data from the ADC
LRX31_P, LRX31_N	G7 and G8	LVDS receiver data from the ADC
LRX32_P, LRX32_N	G11 and G10	LVDS receiver data from the ADC
LRX33_P, LRX33_N	G14 and G13	LVDS receiver data from the ADC
LRX34_P, LRX34_N	G17 and G16	LVDS receiver data from the ADC
LRX35_P, LRX35_N	G20 and G19	LVDS receiver data from the ADC
LRX36_P, LRX36_N	F21 and F22	LVDS receiver data from the ADC
LRX37_P, LRX37_N	F24 and F25	LVDS receiver data from the ADC
LRX38_P, LRX38_N	F28 and F27	LVDS receiver data from the ADC

Table 5. FMC Connector J10 Description of the TSW14DL3200 Device: Receive Data (continued)

FMC Signal Name	FMC Pin	Description
LRX39_P, LRX39_N	F31 and F30	LVDS receiver data from the ADC
LRX40_P, LRX40_N	F34 and F33	LVDS receiver data from the ADC
LRX41_P, LRX41_N	H21 and H22	LVDS receiver data from the ADC
LRX42_P, LRX42_N	H24 and H25	LVDS receiver data from the ADC
LRX43_P, LRX43_N	H28 and H27	LVDS receiver data from the ADC
LRX44_P, LRX44_N	H31 and H30	LVDS receiver data from the ADC
LRX45_P, LRX45_N	H34 and H33	LVDS receiver data from the ADC
LRX46_P, LRX46_N	H36 and H37	LVDS receiver data from the ADC
LRX47_P, LRX47_N	H39 and H40	LVDS receiver data from the ADC
RX_STROBE0_P, RX_STROBE0_N	A16 and A17	Synchronization strobe for LVDS Bus A
RX_STROBE1_P, RX_STROBE1_N	E19 and E20	Synchronization strobe for LVDS Bus B
RX_STROBE2_P, RX_STROBE2_N	E16 and E17	Synchronization strobe for LVDS Bus C
RX_STROBE3_P, RX_STROBE3_N	F37 and F36	Synchronization strobe for LVDS Bus D
RX_CLK0_P, RX_CLK0_N	K11 and K10	DDR data clock for LVDS Bus A
RX_CLK1_P, RX_CLK1_N	K14 and K13	DDR data clock for LVDS Bus B
RX_CLK2_P, RX_CLK2_N	K20 and K19	DDR data clock for LVDS Bus C
RX_CLK3_P, RX_CLK3_N	K25 and K24	DDR data clock for LVDS Bus D
CLK_ADC_REF_P, CLK_ADC_REF_N	K38 and K39	Clock for FPGA
RX_RESERVE0	J1	Spare signal
RX_RESERVE1	J2	Spare signal
RX_RESERVE2	J3	Spare signal
RX_RESERVE3	J4	Spare signal

Table 6 describes the connector pinout.

Table 6. FMC Connector J8 Description of the TSW14DL3200 Device: Transmit Data

FMC Signal Name	FMC Pin	Description
LTX0_P, LTX0_N	A11 and A10	LVDS transmit data to the DAC
LTX1_P, LTX1_N	A8 and A7	LVDS transmit data to the DAC
LTX2_P, LTX2_N	A4 and A5	LVDS transmit data to the DAC
LTX3_P, LTX3_N	A1 and A2	LVDS transmit data to the DAC
LTX4_P, LTX4_N	C8 and C7	LVDS transmit data to the DAC
LTX5_P, LTX5_N	C4 and C5	LVDS transmit data to the DAC
LTX6_P, LTX6_N	C10 and C11	LVDS transmit data to the DAC
LTX7_P, LTX7_N	C20 and C19	LVDS transmit data to the DAC
LTX8_P, LTX8_N	C17 and C16	LVDS transmit data to the DAC
LTX9_P, LTX9_N	A14 and A13	LVDS transmit data to the DAC
LTX10_P, LTX10_N	C14 and C13	LVDS transmit data to the DAC
LTX11_P, LTX11_N	C1 and C2	LVDS transmit data to the DAC
LTX12_P, LTX12_N	B21 and B22	LVDS transmit data to the DAC
LTX13_P, LTX13_N	B24 and B25	LVDS transmit data to the DAC
LTX14_P, LTX14_N	B28 and B29	LVDS transmit data to the DAC
LTX15_P, LTX15_N	B31 and B30	LVDS transmit data to the DAC
LTX16_P, LTX16_N	B34 and B33	LVDS transmit data to the DAC

Table 6. FMC Connector J8 Description of the TSW14DL3200 Device: Transmit Data (continued)

FMC Signal Name	FMC Pin	Description
LTX17_P, LTX17_N	D22 and D21	LVDS transmit data to the DAC
LTX18_P, LTX18_N	D25 and D24	LVDS transmit data to the DAC
LTX19_P, LTX19_N	D28 and D27	LVDS transmit data to the DAC
LTX20_P, LTX20_N	K8 and K7	LVDS transmit data to the DAC
LTX21_P, LTX21_N	D34 and D33	LVDS transmit data to the DAC
LTX22_P, LTX22_N	D37 and D36	LVDS transmit data to the DAC
LTX23_P, LTX23_N	K17 and K16	LVDS transmit data to the DAC
LTX24_P, LTX24_N	E1 and E2	LVDS transmit data to the DAC
LTX25_P, LTX25_N	E4 and E5	LVDS transmit data to the DAC
LTX26_P, LTX26_N	E8 and E7	LVDS transmit data to the DAC
LTX27_P, LTX27_N	E11 and E10	LVDS transmit data to the DAC
LTX28_P, LTX28_N	E13 and E14	LVDS transmit data to the DAC
LTX29_P, LTX29_N	K1 and K2	LVDS transmit data to the DAC
LTX30_P, LTX30_N	G4 and G5	LVDS transmit data to the DAC
LTX31_P, LTX31_N	G7 and G8	LVDS transmit data to the DAC
LTX32_P, LTX32_N	G11 and G10	LVDS transmit data to the DAC
LTX33_P, LTX33_N	G14 and G13	LVDS transmit data to the DAC
LTX34_P, LTX34_N	G17 and G16	LVDS transmit data to the DAC
LTX35_P, LTX35_N	G20 and G19	LVDS transmit data to the DAC
LTX36_P, LTX36_N	F21 and F22	LVDS transmit data to the DAC
LTX37_P, LTX37_N	F24 and F25	LVDS transmit data to the DAC
LTX38_P, LTX38_N	F28 and F27	LVDS transmit data to the DAC
LTX39_P, LTX39_N	F31 and F30	LVDS transmit data to the DAC
LTX40_P, LTX40_N	F34 and F33	LVDS transmit data to the DAC
LTX41_P, LTX41_N	H21 and H22	LVDS transmit data to the DAC
LTX42_P, LTX42_N	H24 and H25	LVDS transmit data to the DAC
LTX43_P, LTX43_N	H28 and H27	LVDS transmit data to the DAC
LTX44_P, LTX44_N	H31 and H30	LVDS transmit data to the DAC
LTX45_P, LTX45_N	H34 and H33	LVDS transmit data to the DAC
LTX46_P, LTX46_N	H36 and H37	LVDS transmit data to the DAC
LTX47_P, LTX47_N	H39 and H40	LVDS transmit data to the DAC
TX_STROBE0_P, TX_STROBE0_N	A16 and A17	Synchronization strobe for LVDS bus A
TX_STROBE1_P, TX_STROBE1_N	E19 and E20	Synchronization strobe for LVDS bus B
TX_STROBE2_P, TX_STROBE2_N	E16 and E17	Synchronization strobe for LVDS bus C
TX_STROBE3_P, TX_STROBE3_N	F37 and F36	Synchronization strobe for LVDS bus D
TX_CLK0_P, TX_CLK0_N	K11 and K10	Data clock for LVDS bus A
TX_CLK1_P, TX_CLK1_N	K14 and K13	Data clock for LVDS bus B
TX_CLK2_P, TX_CLK2_N	K20 and K19	Data clock for LVDS bus C
TX_CLK3_P, TX_CLK3_N	K25 and K24	Data clock for LVDS bus D
CLK_DAC_REF_P, CLK_DAC_REF_N	K38 and K39	Clock for FPGA
TX_RESERVE0	J1	Spare signal
TX_RESERVE1	J2	Spare signal
TX_RESERVE2	J3	Spare signal
TX_RESERVE3	J4	Spare signal

3.3.3.3 JTAG Connectors

The TSW14DL3200EVM includes nine industry-standard JTAG connectors; one that connects to the JTAG ports of the FPGA, seven that connects to the JTAG pins of the step-down converters, and one that connects to the programming pins of the power monitor and sequencer device. Jumpers on the TSW14DL3200EVM allow for the FPGA to be programmed from JTAG connector J25 or the USB interface. JTAG connectors J16, J18, J19, and J20 to J24 are for troubleshooting only. The board default setup is with the FPGA JTAG pins connected to JTAG connector J25. The FPGA can be programmed using this connector if the M0–M3 inputs are set to the proper logic levels. These inputs are set by resistors R348, R349, and R350. Consult the Xilinx XCKU060 data sheet for more information regarding JTAG programming. The FPGA also has the parallel programming inputs connected to the USB 3.0 controller. With JP2–JP4 in the default positions, the FPGA can be programmed by the HSDC Pro software GUI. Every time the TSW14DL3200EVM is powered-down, the FPGA configuration is removed. The user must program the FPGA through the GUI every time the board is powered-up. The Cypress USB3.0 controller device is programmed at power-up using the factory preprogrammed flash device U7. JTAG connector J16 is used to program the TI UCD90120A power monitor and sequencer device. This device is preprogrammed at the factory and this interface is only to be used for troubleshooting.

3.3.3.4 USB I/O Connection

Control of the TSW14DL3200EVM is through the USB 3.0 connector J7. This control provides the interface between the HSDC Pro GUI running on a PC using the Microsoft® Windows® operating system and the FPGA. For the computer, the drivers needed to access the USB port are included on the HSDC Pro GUI installation software that can be downloaded from the web. The drivers are automatically installed during the installation process. On the TSW14DL3200EVM, the USB port is used to identify the type and serial number of the EVM under test, load the desired FPGA configuration file, capture data from ADC EVMs, and send test pattern data to the DAC EVMs.

4 Software Start-Up

4.1 Installation Instructions

- Download the latest version (v4.9 or higher) of the HSDC Pro GUI to a local location on a host PC. This program can be found on www.ti.com by entering *high speed data converter pro GUI installer* in the search bar.
- Unzipping the software package generates a folder called *High Speed Data Converter Pro - Installer vx.xx.exe*, where x.xx is the version number. Run this program to start the installation.
- Make sure to disconnect all USB cables from any TSW14xxx boards before installing the software.
- Follow the onscreen instructions during installation.
- Click on the **Install** button. A new window opens. Click the **Next** button.
- Accept the license agreement. Click on the **Next** button to start the installation. After the installer has finished, click the **Next** button one last time.
- The installation is now complete. The GUI executable and associated files reside in the following directory:
  C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro.
- Power-up the TSW14DL3200 under test.
- To start the GUI, click on the file called *High Speed Data Converter Pro.exe*, located under *C:\Program Files\Texas Instruments\High Speed Data Converter Pro*.

NOTE: If an older version of the GUI has already been installed, make sure to uninstall the older version before loading a newer version. If the GUI detects that a newer version of the GUI is available online (DATACONVERTERPRO-SW), the GUI assists the user with downloading the latest version from the TI website. The GUI automatically interrogates the product website for latest version every seven days but the latest version check can also be manually invoked through use of the pulldown menu Help->Check for updates.

NOTE: When new TI high-speed data converter EVMs or interface modes become available that are not currently supported by the latest release of the HSDC Pro GUI, the HSDCProv_xpxx_Patch_setup executable, available on the TI website under the High Speed Data Converter Pro Software product folder (DATACONVERTERPRO-SW), allows the user to add these items to the GUI device list. After the patch is downloaded, follow the onscreen instructions to run the patch. The software displays the files to be added. After running the patch, open HSDC Pro and the new parts and modes appear in the ADC and DAC device drop-down selection box. The patch is always specific to a core GUI version and does not work for a GUI version for which the patch was not explicitly created.

4.2 USB Interface and Drivers

- Connect a USB 3.0 cable between J7 of the TSW14DL3200EVM and a host PC.
- Connect an ADC EVM to be tested with the TSW14DL3200EVM.
- Connect the provided power cable between the EVM and a 12-VDC source. LED D19 now turns green.
- Set SW2 to on. LEDs D22, D9-D13, D15-D17, and D19-D21, as shown in Figure 3, all turn blue now.

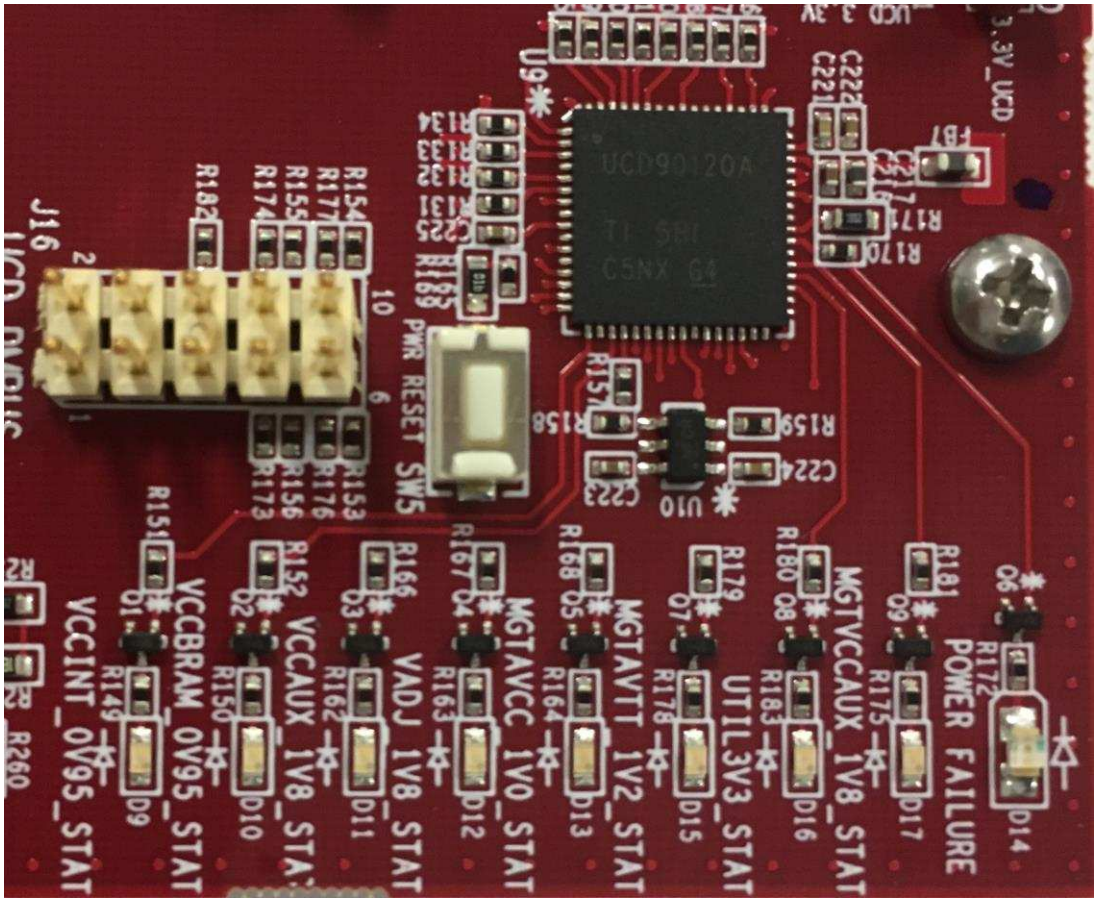

Figure 3. Power Indicator LEDs

NOTE: Power-up and configure the ADC EVM. This step is required to provide data to the TSW14DL3200EVM, which is needed for I/O delay calibration, and occurs immediately after the firmware is downloaded.

Click on the High-Speed Data Converter Pro icon that was created on the desktop panel, or go to *C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro* and double click on the executable called *High Speed Data Converter Pro.exe* to start the GUI.

The GUI first attempts to connect to the EVM USB interface. If the GUI identifies a valid board serial number, as shown in Figure 4, a pop-up opens displaying this value. The user can connect several TSW14DL3200EVMs to one host PC, but the GUI can only connect to one EVM at a time. When multiple boards are connected to the PC, the pop-up displays all of the serial numbers found. The user then selects which board to associate the GUI with.

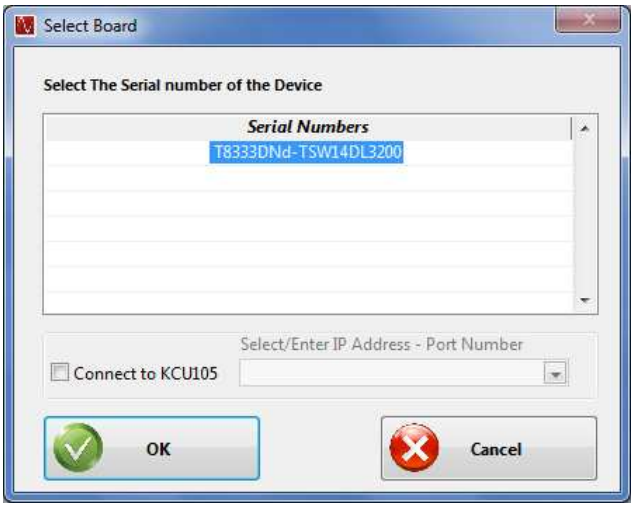

Figure 4. TSW14DL3200EVM Serial Number

Click **OK** to connect the GUI to the board. The top level GUI, as shown in Figure 5, then opens.

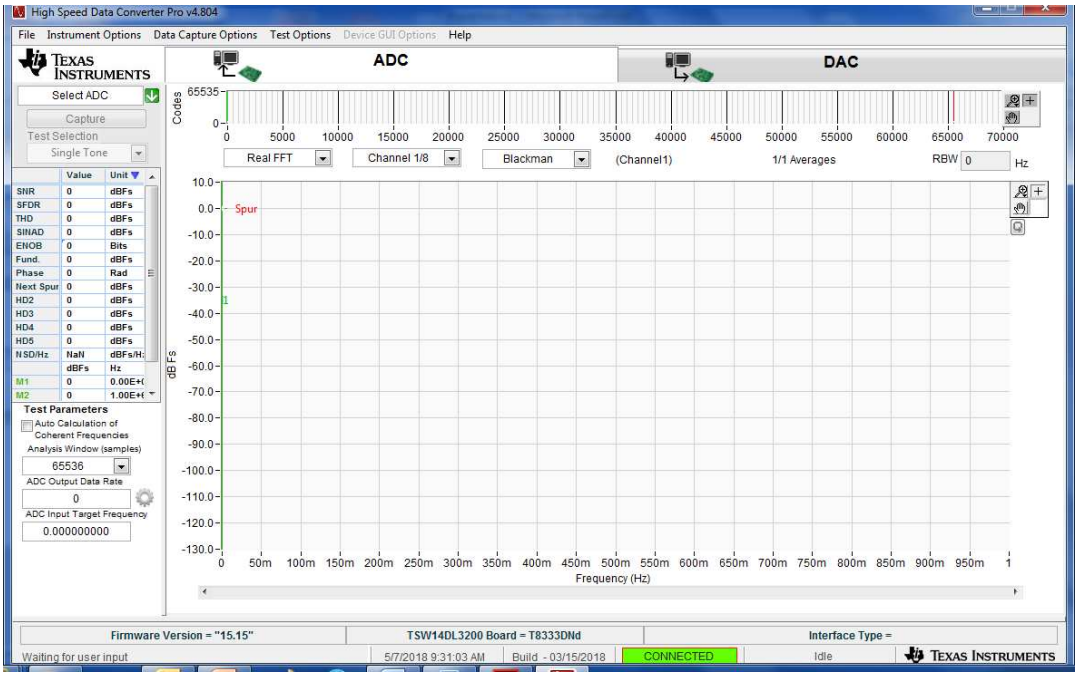

Figure 5. High-Speed Data Converter Pro GUI Top Level

A new pop-up opens with the message *No firmware. Please select a device to load firmware into the board*. Click on **OK**.

If the message *No Board Connected* opens, double check the USB cable connections and that power switch SW2 is in the on position. Remove the USB cable from the board then re-install. Click on the *Instrument Option* tab at the top left of the GUI and select *Connect to the Board*. If this process still does not correct the issue, check the status of the host USB port.

When the software is installed and the USB cable is connected to the TSW14DL3200EVM and the PC, the TSW14DL3200 USB 3.0 converter must be located in the Hardware Device Manager under the universal serial bus controllers as shown in Figure 6, labeled as *Cypress FX3 USB Streamer Example Device*. When the USB 3.0 cable is removed, this driver is no longer visible in the device manager. If the drivers are present in the device manager window and the software still does not connect, remove the USB 3.0 cable from the board then reconnect. Attempt to connect to the board. If the problem still exists, cycle power to the board and repeat the prior steps.

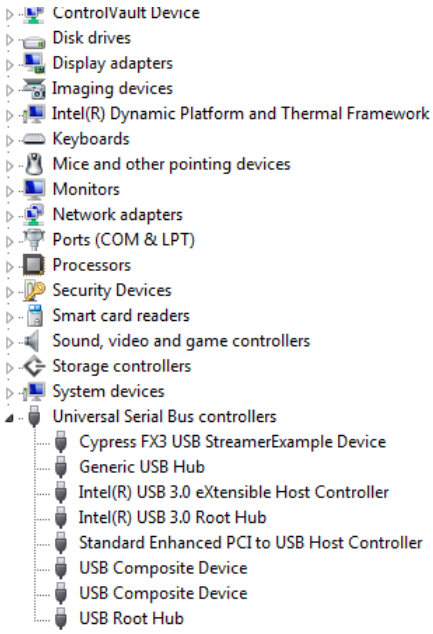

Figure 6. Hardware Device Manager

5 Downloading Firmware

The TSW14DL3200EVM has a Xilinx XCKU060 device that requires firmware to be downloaded every time power is cycled to operate. The firmware files needed are special .bin formatted files that are provided with the software package. The files used by the GUI currently reside in the directory called *C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14DL3200 Details\Firmware*.

To load a firmware after the GUI has established connection, click the *Select ADC* window in the top left of the GUI and select the device to evaluate, as shown in Figure 7 (for example, ADC12DL3200_LDEMUX_1_DES_EN_0).

Figure 7. Select ADC Firmware to be Loaded

The GUI prompts the user to update the firmware for the ADC. Click **Yes**. The GUI displays the message *Downloading Firmware, Please Wait*. The software now loads the firmware from the PC to the FPGA, a process that takes approximately 3 seconds. When completed, the GUI reports an interface type in the lower right corner and LED D2 turns green. Enter an ADC output data rate in the GUI and click on the **Capture** button. When data are captured LED D1 turns on. Figure 8 shows the status LEDs after both the firmware has been loaded and data are captured,

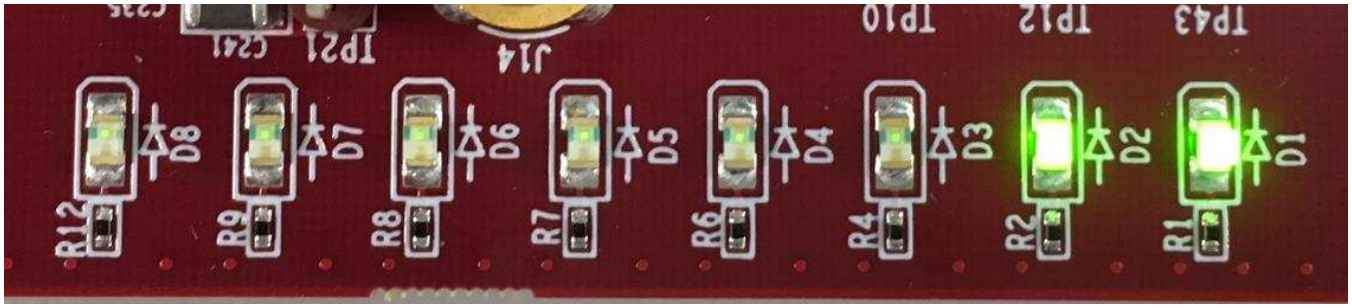

Figure 8. Status LEDs

For more information regarding the use of the TSW14DL3200EVM with a TI ADC or DAC wide LVDS interface EVM, consult the *High-Speed Data Converter Pro GUI User's Guide* and the individual EVM User's Guide, available on www.ti.com.

If the message appears as shown in Figure 9, verify that all jumpers are in the default position and all power status LEDs are illuminated. If certain jumpers are not installed in the proper location, the USB 3.0 controller does not boot from flash memory. If any power status LED is off, there may be a problem with a power supply on the board, which can prevent the firmware from downloading. Unplug and re-install the USB connector and try to connect to the board. If this connection fails, cycle the power switch to re-initialize the power-up sequencer to try to correct this problem.

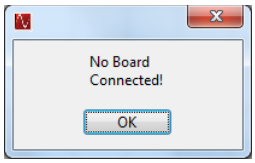

Figure 9. Download Firmware Error Message

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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