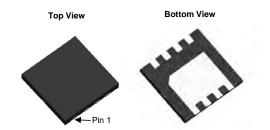


BSZ040N04LS G-VB Datasheet N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^f	Q _g (Typ.)		
40	0.0045 at V _{GS} = 10 V	40 ^g	9.8 nC		
40	0.0062 at V _{GS} = 4.5 V	40 ^g	9.0110		

DFN 3x3 EP



FEATURES

- Trench Power MOSFET
- 100 % R_q and UIS Tested
- Capable of Operating with 5 V Gate Drive

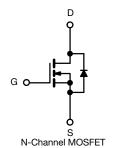


APPLICATIONS

- Synchronous Rectification
- Synchronous Buck Converters
- **ORing**
- Load Switching
- Motor Drive Switch

Top View





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	40	V		
Gate-Source Voltage		V _{GS}	± 20	V	
	T _C = 25 °C		40 ^g		
Continuous Drain Current (T = 150 °C)	T _C = 70 °C	1 .	40 ^g		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	- I _D	19.3 ^{a, b}		
	T _A = 70 °C	1	15.5 ^{a, b}	Α	
Pulsed Drain Current (t = 100 μs)		I _{DM}	100	^	
Continuous Source-Drain Diode Current	T _C = 25 °C	- I _S	40 ^g		
Continuous Source-Drain Diode Current	T _A = 25 °C		3.1 ^{a, b}		
Single Pulse Avalanche Current L = 0.1 mH		I _{AS}	20		
Single Pulse Avalanche Energy		E _{AS}	20	mJ	
	T _C = 25 °C		52		
Maximum Power Dissipation	T _C = 70 °C	1 .	33	w	
Maximum Power Dissipation	T _A = 25 °C	- P _D	3.7 ^{a, b}	VV	
	T _A = 70 °C	1	2.4 ^{a, b}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Tempera		260			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, e}	t ≤ 10 s	R _{thJA}	26	33	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.9	2.4	C/ VV	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s. c. The DFN 3 x 3 EP is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components. e. Maximum under steady state conditions is 81 °C/W.
- f. Based on T_C = 25 °C.g. Package limited.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A}$	40			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		56		>//06
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 6		mV/°
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1.1		2.2	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zoro Cata Valtaga Drain Current	_	V _{DS} = 40 V, V _{GS} = 0 V			1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α
Drain Course On Ctata Basistanas ^a	Б	V _{GS} = 10 V, I _D = 20 A		0.0045		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		0.0062		Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		65		S
Dynamic ^b						
Input Capacitance	C _{iss}			1330		pF
Output Capacitance	C _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1200		
Reverse Transfer Capacitance	C _{rss}			66		
Total Octo Observe		$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		21.3	32	nC
Total Gate Charge				9.8	15	
Gate-Source Charge	Q_{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		3.2		
Gate-Drain Charge	Q _{gd}			2.5		
Output Charge	Q _{oss}	V _{DS} = 20 V, V _{GS} = 0 V		32	48	
Gate Resistance	R_{g}	f = 1 MHz	0.2	0.9	1.5	Ω
Turn-On Delay Time	t _{d(on)}			22	44	
Rise Time	t _r	$V_{DD} = 20 \text{ V}, R_{I} = 2 \Omega$		65	120	1
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		24	45	
Fall Time	t _f			9	18	
Turn-On Delay Time	t _{d(on)}			11	22	ns
Rise Time	t _r	V_{DD} = 20 V, R_L = 2 Ω		11	22	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	44	
Fall Time	t _f			9	18	
Drain-Source Body Diode Characteristic						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			40	
Pulse Diode Forward Current ($t = 100 \mu s$)	I _{SM}				100	A
Body Diode Voltage	V _{SD}	I _S = 4 A, V _{GS} = 0 V		0.75	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			31	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			17	34	nC
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		13		
Reverse Recovery Rise Time	t _b			18		ns

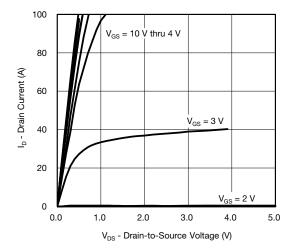
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

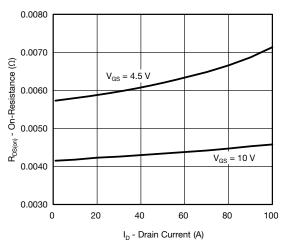
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



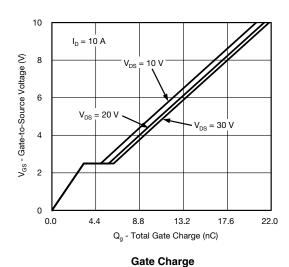
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

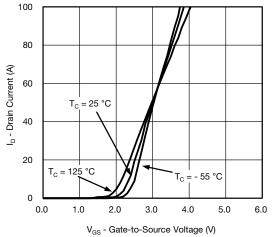


Output Characteristics

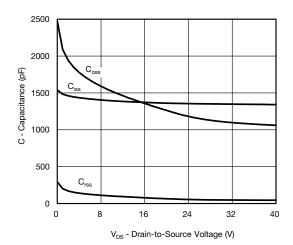


On-Resistance vs. Drain Current and Gate Voltage

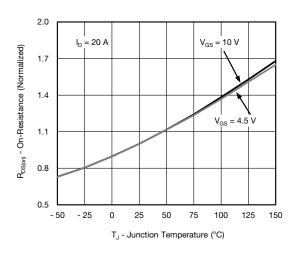




Transfer Characteristics



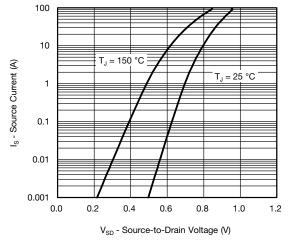
Capacitance



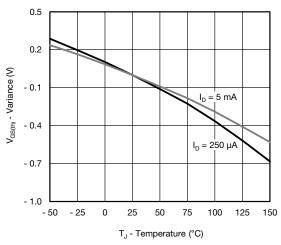
On-Resistance vs. Junction Temperature



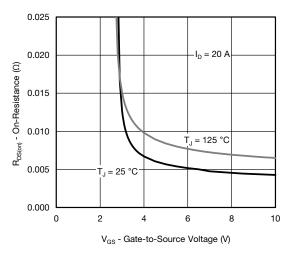
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



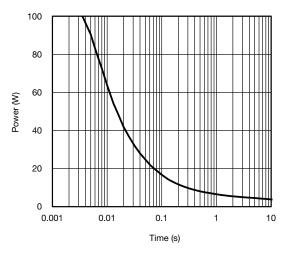
Source-Drain Diode Forward Voltage



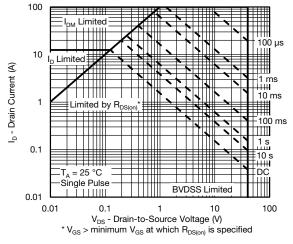
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



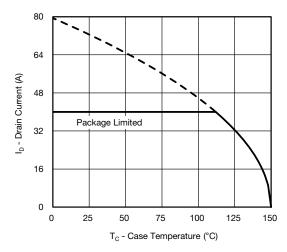
Single Pulse Power, Junction-to-Ambient



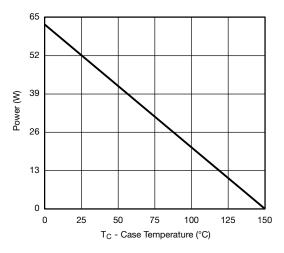
Safe Operating Area, Junction-to-Ambient



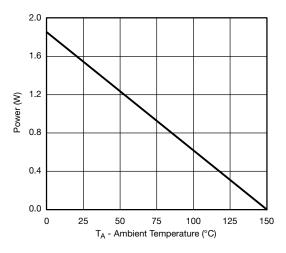
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*







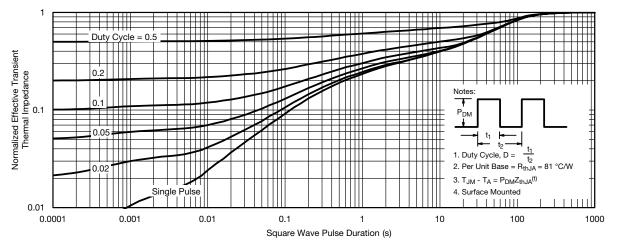
Power, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

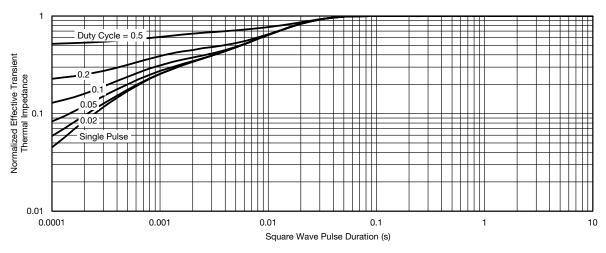
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

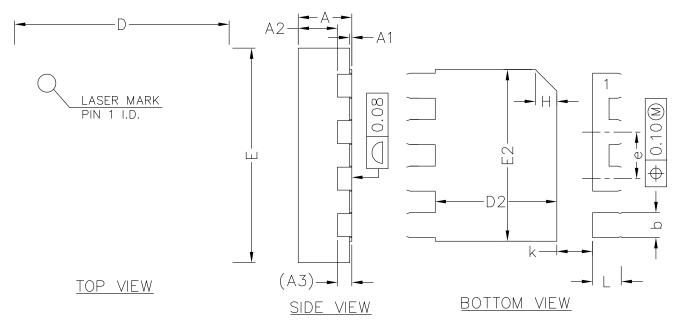


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case







COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX		
А	0.70	0.75	0.80		
A1	0.00	0.02	0.05		
A2	0.50	0.55	0.60		
А3	0.20REF				
Ь	0.30	0.35	0.40		
D	2.90	3.00	3.10		
Ε	2.90	3.00	3.10		
D2	1.60	1.70	1.80		
E2	2.30	2.40	2.50		
е	0.55	0.65	0.75		
K	0.40	0.50	0.60		
L	0.35	0.40	0.45		



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